Al-Ta_2O_5-GaN SEMICONDUCTOR DEVICE STRUCTURE

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$Al\text{-}Ta_2O_5\text{-}GaN$
SEMICONDUCTOR DEVICE STRUCTURE

by

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LIST OF SYMBOLS

α	Absorption coefficient
A	Cross-sectional area of gate in MOS structure
c	Speed of light in free space
č	Capture cross section
C	Total capacitance
C_{ADJ}	Series resistance compensated parallel model capacitance
C_{FB}	Flat band capacitance
C_{min}	Minimum capacitance
C_{ox}	Oxide capacitance
C_s	Semiconductor depletion layer capacitance
D	Dielectric displacement
D_{it}	Interface trap density
D_{it}^{m}	Mid-gap interface trap density
D_n	Electron diffusivity
D_{total}	Total interface trap density
$Đ_{total}$	Total transmission coefficient
ε_d	Dynamic dielectric constant
ε_o	Vacuum permittivity
ε_r	Relative permittivity
ε_s	Semiconductor permittivity
E	Electric field strength
E_c	Bottom of conduction band
E_F	Fermi level
E_g	Energy band gap
E_i	Intrinsic Fermi level
E_o	Minimum energy where an electron must have to reach vacuum level
E_{OT}	Equivalent oxide thickness
E_{ox}	Electric field in oxide

E_s	Electric field in semiconductor
E_v	Top of valance band
f	Frequency
G	Conductance
G_{ADJ}	Series resistance compensated conductance
h	Plank's constant
ħ	Reduced Plank's constant
I	Current
J	Current density
J_{child}	Child's law current density
J_{DT}	Direct tunneling current density
J_{FAT}	Field-assited tunneling current density
J_{FN}	Fowler-Nordheim tunneling current density
J_g	Post-stress current density
J_o	Pre-stress current density
J_{Ohm}	Ohm's current density
J_{PF}	Poole-Frenkel emission current density
J_{SE}	Schottky emission current density
J_{TAT}	Trap-assited tunneling current density
J_{TFL}	Trap-filled limited current density
$\Delta J/J_o$	Defect density created by constant voltage stress
k	Extinction coefficient
k_B	Boltzmann constant
k_{ox}	Dielectric constant of oxide
κ	Wave vector in a medium with wavelength λ
κ_o	Wave vector in free space with wavelength λ_o
κ_{ox}	Wave vector in oxide
m_o	Electron rest mass
m_n	Electron effective mass
m_p	Hole effective mass

m_{ox}^{*}	Effective mass of electron in oxide
n	Concentration of free electrons
ň	Reflective index
n_{bulk}	Electron concentration in the bulk of non-degenerate semiconductor
n_i	Intrinsic carrier concentration
n_n	Electron concentration in n-type semiconductor
n_o	Density of thermal generated free carriers
n_s	Electron concentration at semiconductor surface
Ň	Flux of metal electrons
N_A	Acceptor impurity density
N_D	Donor impurity density
N_f	Fixed oxide charges density
N_T	Total trap density in oxide
p	Concentration of free holes
p_{bulk}	Hole concentration in the bulk of non-degenerate semiconductor
p_n	Hole concentration in n-type semiconductor
p_s	Hole concentration at semiconductor surface
ρ	Charge density per unit volume
ρ_s	Surface charge density per unit volume
þ	Resistivity
$þ_d$	Dynamic resistivity
P	Radiometric power
P_g	Defect generation rate
q	Electronic charge
$q\phi_m$	Work function of metal
$q\phi_s$	Work function of semiconductor
$q\phi_{ms}$	Work function difference between metal and semiconductor
$q\chi$	Electron affinity
$q\Psi_B$	Energy difference between Fermi level and intrinsic Fermi level
Q_f	Fixed oxide charges

Q_{inj}	Injected charges
Q_{it}	Interface trapped charges
Q_m	Mobile ionic charges
Q_M	Charges placed on gate
Q_{ot}	Oxide trapped charges
Q_{ox}	Positive sheet charges per unit area in oxide
Q_p	Charges in inversion layer
Q_s	Charges per unit area in semiconductor
Q_{sc}	Charges in depletion layer
r	Compensation factor
r_d	Dynamic resistance
R	Resistance
Ř	Reflectance
R_S	Series resistance
R_{Sh}	Sheet resistance
S_{Ohm}	Gradient of logarithm J-V plot in Ohm's conduction
t	Time
t_{ox}	Oxide thickness
τ_e	Electron transit time
T	Absolute temperature
T_c	Characteristic temperature related to trap distribution
μ_n	Electron mobility
v	Phase velocity of light wave
υ	Frequency of light wave
V	Voltage
V_{FB}	Flat band voltage
V_G	d.c. bias on gate
V_o	Potential across oxide
V_{on}	Crossover voltage where Ohm's law transits to Child's law
V_S	Stressing voltage

V_T	Gate threshold voltage at the onset of strong inversion
V_{TFL}	Threshold voltage of trap-filled limited process
ω	Angular frequency
W	Depletion layer width
W_m	Maximum width of depletion region
Z	Charge of center in Poole-Frenkel emission
σ	Electrical conductivity
σ_d	Dynamic conductivity
λ	Light wavelength in a medium
λ_o	Light wavelength in free space
λ_{Debye}	Extrinsic Debye length
φ_o	Triangular barrier height in Fowler-Nordheim tunneling
ϕ	Fluence
ϕ_B	Barrier height between semiconductor and oxide
ϕ_F	Electrostatic potential of semiconductor
ϕ_{ox}	Metal-oxide barrier
ϕ_{PF}	Barrier lowering associated with Coulomb potential in Poole-Frenkel emission
ϕ_t	Energy barrier separating traps from conduction band in Poole-Frenkel emission
$\Delta\phi$	Conduction band offset between oxide and oxide-semiconductor interface
Φ_o	Photon flux
$\Psi(x)$	Electrostatic potential inside semiconductor at a given point x
Ψ_B	Potential difference between Fermi level and intrinsic Fermi level
Ψ_s	Surface potential at $x = 0$
Ψ_s (inv)	Surface potential at strong inversion
θ	X-ray diffraction angle

LIST OF ABBREVIATIONS

a. c.	Alternating current
a. u.	Arbitrary unit
AFM	Atomic force microscope
Ag	Silver
Al	Aluminium
AlN	Aluminium nitride
Al_2O_3	Aluminium oxide
Ar	Argon
Au	Gold
BFOM	Baliga figure-of-merit
BHFFOM	Baliga high-frequency figure-of-merit
BOE	Buffer oxide etch
BSE	Back-scattered electron
C	Carbon
Ca	Calcium
CaO	Calcium oxide
Cd	Cadmium
CMOS	Complementary metal-oxide-semiconductor
Co	Cobalt
Cr	Chromium
Cu	Copper
C-V	Capacitance-voltage
CVS	Constant voltage stress
d.c.	Direct current
DFT	Density functional theory
DI	Deionized
DRAM	Dynamic random access memory
DUT	Device-under-test
ECR	Electron cyclotron resonance

EDX	Energy dispersive x-ray
ELOG	Epitaxial lateral overgrowth
FAT	Field-assited tunneling
FEG	Field emission gun
FESEM	Field emission scanning electron microscope
FIB	Focused ion beam
FN	Fowler-Nordheim
FOM	Figure-of-merit
FWHM	Full width at half maximum
G	Gate
GaAs	Gallium arsenide
$GaCl_3$	Gallium chloride
GaN	Gallium nitride
Ga_2O_3	Gallium oxide
GaP	Gallium phosphite
GPIB	General purpose interface bus
H	Hydrogen
HBT	Heterojunction bipolar transistor
HCl	Hydrochloric acid / hydrogen chloride
HEMT	High electron mobility transistor
HF	Hydrofluoric acid
HFET	Heterojunction field effect transistor
HNO_3	Nitric acid
H_2O	Water
H_3PO_4	Phosphoric acid
HVPE	Hydride vapor phase epitaxy
ICS	Interactive characterization software
InP	Indium phosphide
I-V	Current-voltage
JFOM	Johnson figure-of-merit

KFOM	Keyes figure-of-merit
LaB_6	Lanthanum hexaboride
LED	Light emitting diode
LEEBI	Low energy electron beam irradiation
Li	Lithium
LMIS	Liquid-metal ion sources
MBE	Molecular beam epitaxy
MCA	Multi channel analyzer
MESFET	Metal-semiconductor field effect transistor
Mg	Magnesium
MgO	Magnesium oxide
MISFET	Metal-insulator-semiconductor field effect transistor
MOCVD	Metal-organic chemical vapor deposition
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
NH_3	Ammonia
NH_4OH	Ammonium hydroxide
Ni	Nickel
OBIC	Optical beam induced current
PDA	Post-deposition annealing
PF	Poole-Frenkel
PMA	Post-metallization annealing
PSD	Position sensitive detector
Pt	Platinum
PVD	Physical vapor deposition
QB	Quasi-breakdown
RCA	Radio Corporation of America
RF	Radio-frequency
RHEED	Reflection high-energy electron diffraction
RMS	Root mean square

RPECVD	Remote plasma-enhanced chemical vapor deposition
SC	Standard cleaning
SCL	Space charge limited
Sc_2O_3	Scandium oxide
S-D	Source-drain
SE	Spectroscopic ellipsometry
SEI	Seebeck effect imaging
SEM	Scanning electron microscope
Si	Silicon
SiC	Silicon carbide
SILC	Stress-induced leakage current
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
SOG	Spin-on-glass
SPM	Scanning probe microscope
SR	Spectral reflectance
Ta_2O_5	Tantalum oxide
TAT	Trap-assited tunneling
TFL	Trap-filled limited
Ti	Titanium
TIVA	Thermally-induced voltage alteration
UV	Ultraviolet
XRD	X-ray diffraction
XRF	X-ray fluorescent
Zn	Zinc

STRUKTUR PERANTI SEMIKONDUKTOR
Al/Ta_2O_5/GaN

ABSTRAK

Peranti semikonduktor berasaskan GaN telah dikaji secara menyeluruh bagi penggunaan dalam kuasa dan suhu tinggi bagi menggantikan Si yang tidak dapat lagi memenuhi keperluan tersebut. Sifat seperti kebocoran arus yang rendah, ketumpatan cas oksida yang rendah, dan kapasitan yang tinggi amat diperlukan untuk peranti MOS berasaskan GaN berkualiti tinggi. Dalam pada itu, terdapat juga kecenderungan tinggi dalam membangunkan transistor MOS berasaskan GaN. Kajian pada awal tahun 2000-an menggunakan filem oksida GaN sebagai dielektrik di dalam struktur MOS. Pada hujung tahun 2000-an, MOS berasaskan GaN dengan dielektrik seperti Al_2O_3, MgO, Sc_2O_3, Si_3N_4, SiO_2, dan Ta_2O_5 telah dibangunkan.

Dalam penyelidikan ini, wafer komersial yang mengandungi GaN-atas-nilam digunakan sebagai semikonduktor. Penebat pintu dibina dengan memendapkan bahan oksida terpilih seperti SiO_2, Al_2O_3 dan Ta_2O_5 ke atas GaN menggunakan teknik percikan frekuensi-radio. Logam pintu pula dibina dengan menyejatkan aluminum ke atas penebat. Pencirian bagi penebat dilakukan menerusi AFM, XRD, XRF, SEM dan EDX. Selain itu, pengukuran C-V, I-V dan D_{it} dilakukan untuk menentukan ciri elektrik struktur MOS. Ciri asas struktur MOS dengan dielektrik SiO_2, Al_2O_3 dan Ta_2O_5 telah dikaji dan dibandingkan. Kajian ini disusuli dengan kes penyelidikan terhadap struktur MOS Al/Ta_2O_5/GaN yang merangkumi sepuhlindap selepas-pemendapan, sepuhlindap selepas-pelogaman, tegasan suhu substrat, tegasan voltan malar, dan tegasan sinaran cahaya.

Penyelidikan ini telah membuktikan bahawa struktur MOS yang difabrikasi dengan Ta_2O_5 bernilai k tinggi mempunyai prestasi yang paling baik dari segi ketumpatan cas oksida yang rendah, ketumpatan perangkap antaramuka yang rendah, kapasitan yang tinggi, kekonduksian dinamik yang tinggi, kestabilan dalam operasi suhu tinggi, serta ketahanan dalam keadaan tegasan voltan malar. Ciri-ciri peranti yang diperoleh daripada penyelidikan ini adalah lebih baik jika dibandingkan dengan sesetengah data daripada literatur.

$Al/Ta_2O_5/GaN$
SEMICONDUCTOR DEVICE STRUCTURE

ABSTRACT

GaN-based semiconductor devices have been extensively investigated for used in high power and high temperature device applications in order to replace Si which is no longer capable to fulfill these ever-increasing demands. The characteristics of low leakage current, low oxide charge density, and high oxide capacitance would be necessary for device-quality GaN-based MOS devices. Along this, there is a great interest in development of GaN-based MOS transistors. The foremost work in early 2000s used a thermally oxidized GaN film as the gate dielectric in MOS structure. In late 2000s, GaN-based MOS with other dielectrics such as Al_2O_3, MgO, Sc_2O_3, Si_3N_4, SiO_2, and Ta_2O_5 were developed.

In the present work, commercial GaN-on-sapphire wafer was used as the semiconductor. The gate insulator was obtained by depositing selected oxide materials of SiO_2, Al_2O_3, and Ta_2O_5 onto GaN using RF-sputtering technique. The gate metal was built by evaporating aluminium onto the insulator. The deposited insulators were characterized using AFM, XRD, XRF, SEM, and EDX. On the other hand, C-V, I-V, and D_{it} measurements were carried out to determine the electrical characteristics of the MOS structures. The fundamental properties of MOS structures with SiO_2, Al_2O_3, and Ta_2O_5 gate dielectrics were studied and compared. Then, case studies of post-deposition annealing, post-metallization annealing, substrate temperature stress, constant voltage stress, and light radiation stress were investigated on the $Al/Ta_2O_5/GaN$ MOS structure.

The research results revealed that MOS structure with high-k dielectric of Ta_2O_5 possessed the best performance in term of lower oxide charge density, lower interface trap density, higher storage capacitance, higher dynamic conductivity, stability in high temperature operation, and durability in constant voltage stress. These characteristics were even better than the ones reported in some existing literatures.

CHAPTER 1

Literature Reviews

1.1 Introduction

MOS (Metal-Oxide-Semiconductor) is the heart of MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) which forms the basic building block of charge-coupled device as storage capacitor in integrated circuits and memories. The first MOSFET was invented by Kahng and Atalla in 1960 using a thermally oxidized silicon (Si) substrate. The silicon dioxide (SiO_2) thickness was 100 nm with gate length of 20 µm. Two keyholes were made on this device for drain and source contacts, while aluminium (Al) was evaporated onto the top elongated area for gate contact. Although today's device has been scaled down into deep submicron regime, Si is still dominating about 90% of the semiconductor devices market [1]. Marching into 21st century, semiconductor industry is seeing greater demand on higher power, high temperature, high voltage, improved spectra purity, and increased bandwidth, especially in the wireless communication technology. Nevertheless, Si is no longer capable to fulfill these ever-increasing demands. Of all design factors, power consumption is the most critical issue as it influences the device reliability significantly. To address this problem, researchers are currently focusing on new semiconductor materials used in power transistor and gallium nitride (GaN) has emerged as the true contender [2].

1.2 Overview of GaN

1.2.1 Crystal Structure

GaN is a hard and mechanically stable material with large heat capacity. It is a binary group III-group V direct band gap semiconductor of wurtzite crystal structure (Figure 1.1 & Figure 1.2). Each of the Ga atom and the N atom is tetrahedrally coordinated and each forms a sublattice which is hexagonal close-pack. The atomic positions are the same as in lonsdaleite (hexagonal diamond). The wurtzite structure is non-centrosymmetric (lacks inversion symmetry), thus it has properties such as piezoelectricity and pyroelectricity, which are not found in the centrosymmetric crystal [3].

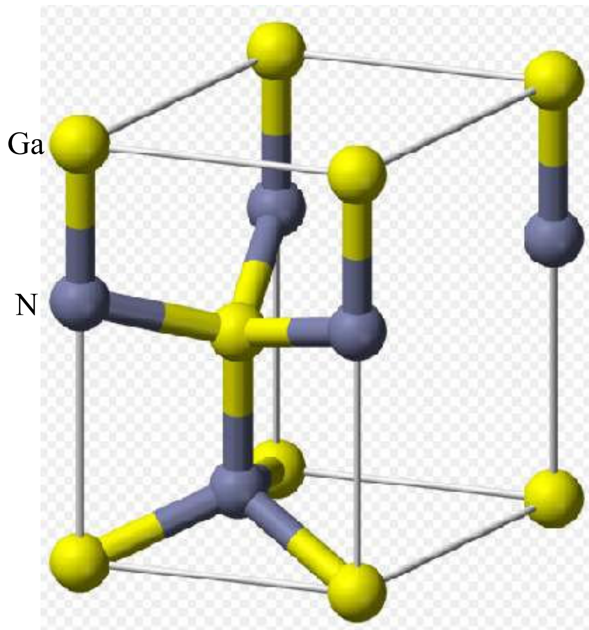


Figure 1.1 Wurtzite unit cell [3]

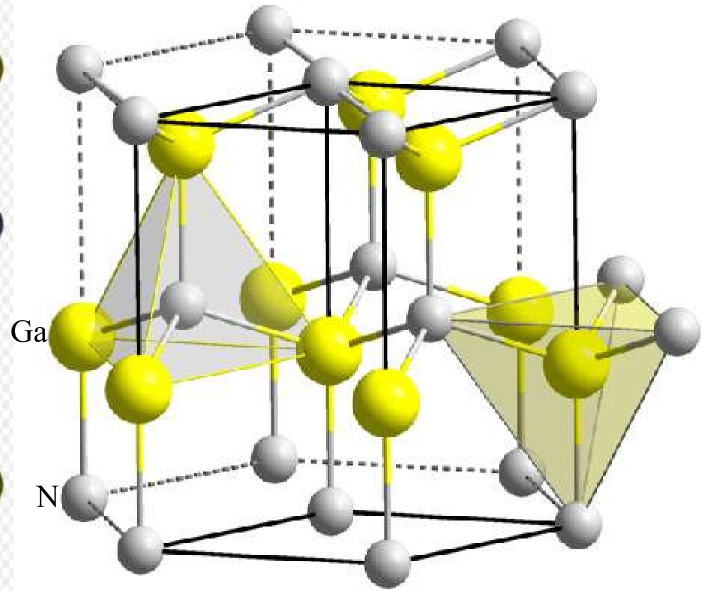


Figure 1.2 Wurtzite structure [3]

1.2.2 History

In 1932, GaN was synthesized in powder form. In 1938, GaN was synthesized in small needles. In 1969, GaN was first grown on a sapphire substrate using hydride vapor phase epitaxy (HVPE). In 1971, GaN was grown epitaxially via metal-organic chemical vapor deposition (MOCVD) and by molecular beam epitaxy (MBE) in 1974. However, lattice mismatch led to poor quality of epitaxial layer until early 1980s. These early epilayers were always unintentionally doped n-type ($n \geq 1x10^{17}$ cm^{-3}), resulting from growth defects or impurities inadvertently introduced during the growth. In 1983, Yoshida et al. improved the epilayer quality by using a two-step growth method, where a thin AlN buffer layer was grown on the sapphire substrate. He managed to confine most mismatch-induced dislocations to a thin AlN/GaN interfacial region rather than throughout the GaN epilayer. In 1989, Amano et al. developed p-type GaN using low energy electron beam irradiation (LEEBI) of Mg-doped GaN. The energy provided by the electron beam depassivated the Mg acceptors by breaking the Mg—H bonds formed during MOCVD growth. Today's GaN epilayers are grown on either β-Al_2O_3 sapphire or 6H-SiC substrate. The differences between the two are shown in Table 1.1 [4].

Table 1.1 Comparison of properties between β-Al_2O_3 sapphire and 6H-SiC substrate [4]

Property	β-Al_2O_3 Sapphire	6H-SiC Substrates
Cost	Cheaper	Expensive
Lattice mismatch to GaN	13%	3.5%
Thermal conductivity	Lower	10x higher
Threading dislocation concentration	$2x10^9$ cm^{-2}	$5x10^8$ cm^{-2}

1.2.3 Synthesis

MOCVD, MBE, HVPE, and ELOG are four common techniques used for the growth of GaN. MOCVD is more popular for group III-nitride growth with an optimum growth temperature of 1050 °C and growth rate of 2 μm/hr for GaN. MBE process uses NH_3 as the nitrogen source at growth temperature of 900-1000 °C and growth rate of 1 μm/hour. HVPE has growth rate of 10 μm/hour and it provides lower dislocation density free-standing thick GaN layers after the substrate has been removed. During ELOG (epitaxial lateral overgrowth) of GaN, thin strips of SiO_2 are patterned on a GaN buffer layer. GaN growth continues selectively on the GaN buffer layer then laterally over the SiO_2 strips. When the SiO_2 mask has been overgrown, the GaN over the SiO_2 has a much lower dislocation density [4].

1.2.4 Applications

GaN has been widely used in optoelectronic devices such as light emitting diode, laser diode, and solar cell for years. GaN can be doped with transition metal like manganese to form spintronics material (magnetic semiconductor). Nanotube of GaN is applied in nanoscale electronic and biochemical sensing application [3]. Nowadays, a wide variety of electronic devices are fabricated using GaN, including heterojunction bipolar transistors (HBTs), heterojunction field effect transistors (HFETs), and high electron mobility transistors (HEMTs). Recently, many researches are focusing on designing the state-of-the-art of microwave power transistors for wireless communication and GaN is emerging as the front runner compared to other semiconductor materials. This is owing to its unique material and electronic properties (Table 1.2) [4].

1.2.5 Physical and Electrical Properties

GaN is a very hard but mechanically stable material with large heat capacity. The comparisons between GaN with other semiconductor materials are given in Table 1.2 [4].

Table 1.2 The properties of various semiconductor materials [4]

Property	**C**	**GaAs**	**GaN**	**InP**	**Si**	**4H-SiC**
Band gap at 300 K (eV)	5.47 (I)	1.424 (D)	3.44 (D)	1.344 (D)	1.12 (I)	3.26 (I)
Dielectric constant	5.57 (dc)	13.2 (dc) 10.9 (∞)	8.9 (dc) 5.35 (∞)	12.4 (dc) 9.66 (∞)	11.7 (dc)	9.6 (dc) 6.7 (∞)
Thermal expansion ($x10^{-6}$ K.Δa/a)	0.08	6.86	5.59	4.5	2.56	4.2
Lattice constant (Å)	3.567	5.653	3.189 (a) 5.185 (c)	5.869	5.431	3.073 (a) 10.05 (c)
m_n/m_o	0.2	0.063	0.22	0.077	1.18	-
m_p/m_o	0.25	0.53	0.8	0.64	0.81	-
Bulk mobility (cm^2/Vs) **Electron** **Hole**	 2200 1600	 8500 400	 900 150	 4600 150	 1450 500	 1140 50
Saturation velocity ($x10^7$ cm/s)	2.7	1.0	2.5	-	1.0	2.0
Breakdown field (MV/cm)	10	0.4	5	-	0.3	3
Thermal conductivity (W/cmK)	22	0.46	1.3	0.68	1.5	4.9
Melting point (K)	3826	1238	Sublimes $T > 1300$	1070	1412	Sublimes $T > 1827$

GaN has band gap energy of 3.4 eV at room temperature, enabling GaN-based device to be having peak internal electric field about 5 times higher than that of Si or GaAs-based devices. This in turn renders higher breakdown voltage, which is necessary for high power handling and high efficiency achievement. GaN has high electron velocity which can minimize the internal device delay. GaN device offers higher impedance, higher bandwidth, and easier input matching. GaN does possess superior linearity (the converse of distortion) that helps to avoid excessive spillover between adjacent channels in power amplifier, thus enable achievement of higher amplifier efficiency. Efficiency is referred to the ability of transistor and amplifier to convert electrical power into output power. On the other hand, GaN exhibits maximum output power density as high as 4 times than that of GaAs. This allows smaller chip to handle the same amount of power. In other words, more chips can be fabricated on a wafer, leading to reduction of cost per chip. Alternatively, the same size device can handle higher power, leading to lower cost per watt of power and thus lower system cost [2].

1.2.6 Figure of Merit (FOM)

Figure of Merit (FOM) is utilized to evaluate the device performance for different applications. There are four common FOMs, where larger FOM represents better device performance. The Johnson FOM (JFOM) considers the breakdown voltage and saturated electron drift velocity in high-frequency handling capability. The Keyes FOM (KFOM) emphasizes materials for high speed digital integrated circuits. The Baliga FOM (BFOM) identifies which materials are best in minimizing conduction power losses in lower-frequency, high-power switching systems, whereas the Baliga high-frequency FOM (BHFFOM) indicates the best material for high-frequency power systems where switching losses due to charging and discharging of input capacitance dominates. These FOMs reveal that the critical field (i.e. dielectric strength), saturation velocity, mobility, energy band gap, thermal conductivity, and dielectric constant are the best predictors of device performance in extreme applications [2, 4]. GaN demonstrates the highest value for JFOM, BFOM, and BHFFOM, as shown in Table 1.3. At room temperature, the doping concentration of GaN is closed to the electron concentration due to the small activation energy of Si donor. The electron mobility is approximately 312 cm^2/Vs at 300 K [5].

Table 1.3 FOM for various semiconductor materials normalized to silicon [4]

	Si	InP	GaP	GaAs	GaN	6H-SiC	4H-SiC
JFOM	1.0	13	37	11	790	260	410
KFOM	1.0	0.72	0.73	0.45	1.8	5.1	5.1
BFOM	1.0	10	16	28	910	90	290
BHFFOM	1.0	6.6	3.8	16	100	13	34

1.3 Research Progress on GaN-Based MOS

The first GaN-based MOSFET with Ga_2O_3 as gate dielectric was reported by Ren et al. [6]. The use of insulator or oxide as the gate dielectric has advantages over metal. This includes lower gate leakage current, lower power consumption, and higher thermal stability [7]. GaN-based MOSFET is more superior than GaN-based MESFET in term of higher temperature performance. GaN-based MOSFET is widely used in electric utility industry, electric vehicle power electronics, as well as defense and space applications. Fabrication of high performance MOSFET on GaN would require good thermal stability, excellent interfacial electrical characteristics, and ease of process [8]. Besides Ga_2O_3, GaN-based MOS with other dielectrics such as Al_2O_3 [9, 10, 11, 12, 13], MgO [14, 15, 16], Sc_2O_3 [7, 16, 17, 18, 19], Si_3N_4 [20, 21], SiO_2 [20, 21, 22, 23, 24, 25, 26] and Ta_2O_5 [27] have also been reported. Literatures on MOS structures with selected dielectrics are discussed below.

1.3.1 Al/Ga_2O_3/GaN MOS

Hyunsoo Kim reported the characteristics of thermally oxidized GaN-based MOS. 1.1 µm thick p-type GaN was epitaxially grown on a sapphire substrate by metal organic chemical vapor deposition (MOCVD). p-type carrier concentration of 2.5×10^{17} cm^{-3} was obtained via van der Pauw measurement. The sample was cleaned in trichloroethylene, acetone, methanol, and deionized water, while the native oxide was removed through buffer oxide etch (BOE). Oxidation was performed in a quartz tube furnace at 850 °C for 12 hours to develop an 88 nm thick oxide. X-ray diffraction (XRD) found peaks at diffraction angles of 49.6° and 59.1°, which were corresponded to monoclinic β-Ga_2O_3 phases with diffraction planes of (206) and (306), respectively. The gate and substrate contacts were made by electron beam evaporation of Pt (60 nm) and Ni/Au (30 nm/80 nm), respectively. Thermal annealing was performed at 500 °C for 1

min in the flow of nitrogen gas. I-V measurement showed breakdown field of 3.85 $MVcm^{-1}$. C-V hysteresis was observed during high-frequency C-V measurement due to oxide charge trap. The oxide charge density N_f was determined as 6.77 $x10^{11}$ cm^{-2} [6]. The disadvantages of Ga_2O_3 were found to be a small band gap of 5.3 eV and a large lattice mismatch of 20% to GaN [14].

1.3.2 Al/MgO/GaN MOS

MgO has advantages over Ga_2O_3 as it possesses a larger band gap of 8 eV and a smaller lattice mismatch of 6.5% to GaN. Study was performed by J. Kim et al. [14] using MOCVD grown n-GaN on sapphire (0001). The sample was subjected to wet chemical etch of HCl:H_2O for 3 min and then rinsed with DI water. The sample was next exposed to UV ozone for 25 min, followed by dipping in BOE for 5 min and the final DI rinse. MgO was grown on n-GaN using a Mg elemental source and a Wavemat MPDR 610 electron cyclotron resonance (ECR) plasma source (2.54 GHz) with 200 W forward power at $1x10^{-4}$ Torr of oxygen pressure. Evaporation of Mg was from an effusion cell operating at 1130 – 1170 °C. The substrate was indium mounted to molybdenum blocks and was loaded into a RIBER 2300 MBE system equipped with reflection high energy electron diffraction (RHEED) system. The substrate surface was polycrystalline according to the RHEED patterns, while a streaky (1x3) pattern was formed upon heating to 700 °C. During fabrication, AZ-1045 and H_3PO_4 were applied in mask etching and oxide removal to expose the underlying GaN for metal deposition. Ohmic contact to GaN was made via Ti/Al/Pt/Au deposition, followed by Pt/Au-based gate deposition. Electrical analysis was carried out using the HP 4284 precision LCR meter. I-V measurement indicated a forward breakdown field of 1.2 MV/cm. C-V measurement done at 1 MHz frequency and 100 mV/s sweep rate revealed a deep depletion behavior at negative bias with no sign of hysteresis. On the other hand, an interface state density of $4x10^{11}$ $eV^{-1}cm^{-2}$ at 0.3 eV below E_c was acquired through Terman method. It rose to $6x10^{11}$ $eV^{-1}cm^{-2}$ at 300 °C [14].

1.3.3 Al/Sc_2O_3/GaN MOS

Sc_2O_3 has a bixbyite crystal structure with 9.2% lattice mismatch to GaN. It possesses dielectric constant of 14 and band gap of 6.3 eV. Sc_2O_3 is effective in mitigating current collapse in AlGaN/HEMT devices via surface traps passivation which can reduce the output power. J.

Kim et al. [7] grew 1 μm thick Mg doped GaN (with hole density of $2x10^{17}$ cm^{-3} at 25 °C) over an undoped GaN buffer on an Al_2O_3 substrate through MOCVD. By using RF plasma activated MBE, Sc_2O_3 of 400 Å thick was then deposited at 650 °C. Oxide outside the gate was etched-off by inductively coupled plasma, while n^+ S/D regions were formed via multiple energy/dose Si^+ implantation (70 keV, $2x10^{13}$ cm^{-2}, 95 keV, $2x10^{13}$ cm^{-2}, and 380 keV, $1.8x10^{13}$ cm^{-2}), followed by annealing at 950 °C. p-ohmic (Ni/Au), n-ohmic (Ti/Al/Pt/Au), and gate metal (Pt/Au) were deposited via e-beam and then patterned by lift-off. Charge pumping method was utilized to measure the total surface charge density that was $3x10^{12}$ cm^{-2}. C-V measurement was performed at 150 kHz and inversion behavior was demonstrated by the n^+ regions in the gated diodes. Sc_2O_3 produced more stable passivation on GaN surface than MgO [7, 17].

1.3.4 Al/Si_3N_4/GaN MOS

GaN-based MOS with silicon nitride (Si_3N_4) gate dielectric was reported by S. Arulkumaran et al. [20]. The GaN surface was subjected to NH_4OH treatment, followed with N_2 plasma treatment prior to Si_3N_4 deposition using PECVD. The author observed an improved Si_3N_4/GaN interface with a clear deep depletion. After chemical treatment, Si_3N_4/GaN structure indeed demonstrated lower interface trap density D_{it} than SiO_2/GaN structure. The breakdown field of Si_3N_4/GaN structure was greater than 5.7 MV/cm even at 350 °C.

1.3.5 Al/SiO_2/GaN MOS

Al/SiO_2/GaN MOS was fabricated by Casey et al. [28] using a remote plasma enhanced chemical vapor deposition (RPECVD) of SiO_2 at 300 °C on a solvent cleaned GaN surface. The measured C-V curve at 10 kHz agreed with the calculated C-V curve and there was no hysteresis. On the other hand, the capacitance in deep depletion obtained during photo-assisted C-V analysis increased from 54 pF to 90 pF, which was larger than the expected value of 60 pF when an inversion layer was formed, and a large hysteresis was observed.

Surface treatments of GaN prior to insulator deposition were investigated by Nakasaki at el. [28]. The surface Fermi level of interfaces with native oxide was strongly pinned due high D_{it}. It was found that NH_4OH solution can effectively reduce natural oxides and interface states. Further reduction of D_{it} was realized by NH_4OH treatment followed by N_2 plasma treatment.

Some studies observed that the Fermi level was unpinned in the SiO_2/GaN interfaces regardless of how the GaN surface was prepared prior to the oxide deposition, while some other works reported that the Fermi level was still pinned in these SiO_2/GaN interfaces if the GaN surface was not properly prepared. The pyroelectric polarization of GaN was measured from the positive flat band voltage shift versus temperature of GaN MOS, in which SiO_2 was deposited by low pressure CVD at 900 °C. A pyroelectric charge coefficient was calculated as 3.7 x 10^9 q/cm^2-K. This pyroelectric effect of increasing negative charge at the GaN surface caused "current slump" in GaN metal-semiconductor field effect transistor (MESFET) and should be considered for high-temperature operation of GaN MISFET [28].

1.3.6 Al/Ta_2O_5/GaN MOS

Tantalum pentoxide (Ta_2O_5) was grown on the n-GaN epilayer by L. W. Tu et al. [27] using the RF magnetron sputtering. He obtained fixed oxide charge density of 4.1 x 10^{12} cm^{-2} calculated from the flat band voltage shift and a hysteresis of 2 V attributed to mobile charges of 2.1 x 10^{12} cm^{-2} in the oxide. He observed a flatten-out after –8 V which indicated the onset of strong inversion due to high dielectric constant of 20 that had never been reported at such a low voltage.

1.4 Research Issues on GaN-Based MOS

In 1965, Gordon E. Moore predicted that the number of transistors per chip would be doubled-up every two-year. This led to higher integration and functionality, but resulted in scaling-down of device dimensions - feature size, gate length, and oxide thickness. The revolution of the design parameters is depicted in the 2003 International Technology Roadmap for Semiconductors (ITRS), which covers a wide range of silicon-based semiconductors and III-V compound semiconductors products and technologies (Figure 1.3 & Table 1.4) [29]. According to this roadmap, the thickness of SiO_2 is shrinking down over the years and this would result in various reliability issues. The oxide thickness is therefore appeared as one of the target of study in this project. It will be proven that by replacing SiO_2 with high-k dielectric material, the oxide thickness can be preserved while maintaining high device quality.

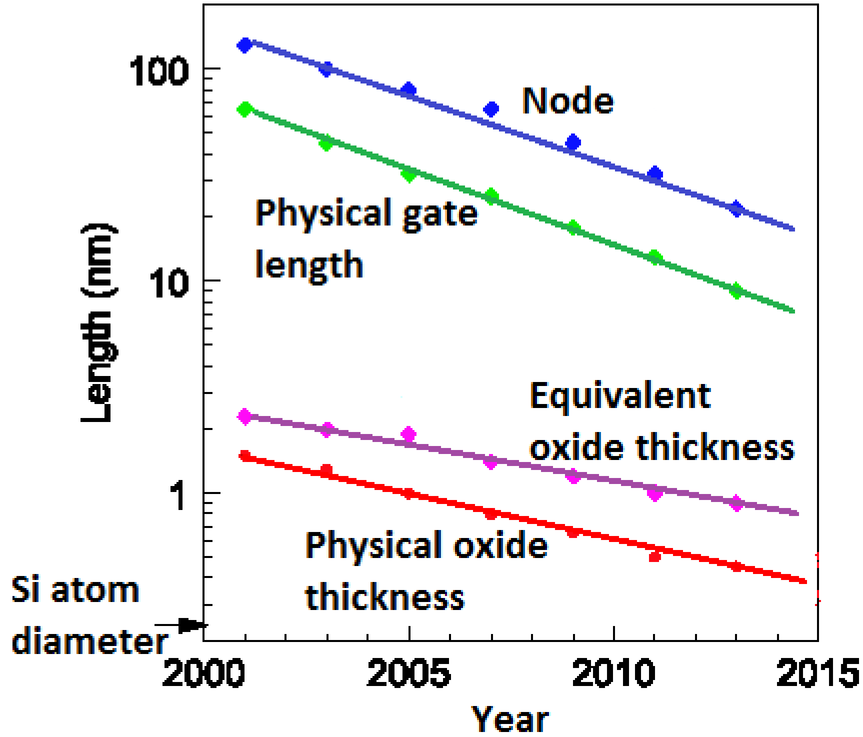


Figure 1.3 The scaling of feature size, gate length, and oxide thickness from year 2000 to year 2015 according to 2003 Semiconductors Roadmap [29].

Table 1.4 Summary of 2003 Semiconductors Roadmap, showing revolution of node, gate length, equivalent oxide thickness of high power (CPU) and low standby power devices (mobile), as well as gate oxide and gate electrode materials [29].

<table>
<tr><th>Year</th><th>2001</th><th>2003</th><th>2005</th><th>2007</th><th>2009</th><th>2012</th><th>2016</th><th>2018</th></tr>
<tr><td>Node</td><td>130</td><td>100</td><td>80</td><td>65</td><td>45</td><td>32</td><td>22</td><td>18</td></tr>
<tr><td>ASIC ½ pitch</td><td>150</td><td>107</td><td>80</td><td>65</td><td>45</td><td>32</td><td>25</td><td>18</td></tr>
<tr><td>Physical gate length</td><td>65</td><td>45</td><td>32</td><td>25</td><td>20</td><td>13</td><td>9</td><td>7</td></tr>
<tr><td>T_{ox} hi power</td><td>1.5</td><td>1.3</td><td>1.1</td><td>0.9</td><td>0.8</td><td>0.6</td><td>0.5</td><td>0.5</td></tr>
<tr><td>T_{ox} lo power</td><td></td><td>2.2</td><td>2.1</td><td>1.6</td><td>1.4</td><td>1.1</td><td>1.0</td><td>0.9</td></tr>
<tr><td>Gate oxide</td><td colspan="3">Oxynitride</td><td colspan="3">HfO_x, Si, N</td><td colspan="2">$LaAlO_3$</td></tr>
<tr><td>Gate metal</td><td colspan="3">Poly Si</td><td colspan="5">Metal gate, e.g. $TaSiN_x$</td></tr>
</table>

SiO_2 has been used as gate dielectric for decades owing to its unique chemical and physical properties as well as its ease of process and integration. The benefits of SiO_2 are thermodynamic stability, native oxide of silicon, stable Si-SiO_2 interface, and low trap density. SiO_2 has large band gap energy of 8-9 eV and it is a good insulator. Besides that, the large barrier height of 3.1 eV and 4.5 eV for holes and electrons, respectively, keeps carriers in the channel [30].

As the transistor size decreases, the thickness of SiO_2 decreases as well in order to increase the gate capacitance and thereby drive current and device performance. Nevertheless, tunneling effect would cause leakage current to rise significantly when the SiO_2 thickness is reduced below 2 nm, resulting in increased power consumption, low breakdown voltage associated with high pinholes density, and deteriorated device reliability. By replacing SiO_2 with high-k material, use of thicker film is allowed without the concomitant leakage while maintaining the same capacitance density. This is extremely important for dynamic random access memory (DRAM) as information is stored as charge in capacitor which is periodically refreshed. The capacitor must be able to retain the charge prior to refresh and the leakage current density must be $< 10^{-7}$ A/cm^2. Thus, SiO_2 should be replaced by high-k materials in order to allow continuous scaling [31].

On the other hand, although III-V semiconductor materials and high-k dielectric materials have been proposed to replace Si and SiO_2 for future generation CMOS technology, high defect density between III-V semiconductor and high-k dielectric is still a major problem yet to be resolved. One solution is to move the channel away from high-k dielectric in buried channel MOSFET structures with barrier layers and some promising research results have been obtained [32].

It was reported that the toughest issue encountered on high-k dielectric is the low-k interfacial dielectric layer that dominates the dielectric constant and prohibit high-k dielectric to be scaled-down below 0.5 nm. Other challenging issues associated with high-k dielectric include threshold and flat band voltage shifts, low mobility, as well as Fermi pinning at the metal-dielectric interface [33].

1.5 Introduction to Oxides

The continuous scaling down of transistor dimension has pushed the gate oxide thickness below 5 nm. This causes drastic increase of leakage current which may impede the device performance [34]. The use of high-k gate dielectric is one of the strategies implemented to allow further miniaturization of microelectronic devices. The required conditions of a new oxide are six-fold [29]:

1. The oxide must have a high enough k that it can be used for a reasonable number of years of scaling.
2. Since the oxide is in direct contact with the semiconductor, so it must be thermodynamically stable with it.
3. The oxide must be kinetically stable and be compatible with processing of 1000 °C for 5s.
4. The oxide must act as an insulator by having band offsets with semiconductor of over 5 eV to minimize carrier injection into its bands.
5. The oxide must form a good electrical interface with semiconductor.
6. The oxide must have few bulk electrically active defects.

There is a trade-off between dielectric constant and band gap condition, where dielectric constant is inversely proportional to band gap (Figure 1.4). In this project, high-k dielectrics of Al_2O_3 and Ta_2O_5 were used to construct GaN-based MOS structures and their results were compared to that of SiO_2. Although Al_2O_3 has the disadvantage of slightly low-k, but it has high band gap as the advantage. In contrast, Ta_2O_5 meets the first condition by having high-k but it has low band gap.

The second condition requires the new oxide to be thermodynamically stable with the underlying semiconductor so that it would not react with the semiconductor to form additional oxide which may negate the effect of using the new oxide. SiO_2 and Al_2O_3 fulfill this second condition but Ta_2O_5 does not. When Ta_2O_5 is annealed at high temperature above 500 °C, a thin layer of Ga_2O_3 may form at the Ta_2O_5-GaN interface. This interfacial Ga_2O_3 layer is good in the sense that it may reduce the dielectric polarization effect, molecular bond distortion, and soft optical phonon scattering, which can lead to higher channel carrier mobility and lower gate leakage current [35]. However, this MOS structure is no longer representing the property of

Al/Ta_2O_5/GaN. Conversely, it is a MOS structure with different characteristic due to the stacked gate dielectrics of Ta_2O_5 and Ga_2O_5. Therefore, annealing temperature must be kept below 500 °C to maintain the thermodynamic stability between Ta_2O_5 and GaN.

The third condition requires the compatibility with existing process conditions. For instance, if an amorphous oxide is selected, the oxide must be remained amorphous when annealed up to 1000 °C for 5s. Al_2O_3 is a reasonably good glass former behind SiO_2, while Ta_2O_5 is moderately good glass former. The amorphous structure of Ta_2O_5 will be transformed into crystalline structure at 500 °C and above, so the operating temperature must be kept below 500 °C to maintain Ta_2O_5 at amorphous stage [36].

According to the fourth condition, the potential barrier at each band must be more than 5 eV so that conduction by the Schottky emission of electrons or holes into the oxide bands can be prevented. This restricts the use of oxide with band gap lower than 5 eV. In this context, Al_2O_3 (8.8 eV) meets this requirement but Ta_2O_5 (4.4 eV) does not. Therefore, Ta_2O_5 could be facing the risk of carrier injection into the oxide bands.

In conjunction with the fifth condition, the oxide must be able to develop high electrical quality with the underlying semiconductor in term of roughness as well as interface defects. Extra defects are associated with oxide grain boundaries. High quality interface can be achieved by either using an epitaxially grown crystalline oxide or an amorphous oxide.

Unlike SiO_2 which has relatively lower concentration of defects, high-k oxides are normally not the material with a low intrinsic defect concentration as their bonding cannot relax easily. High-k oxides can suit the sixth condition via proper processing control and annealing.

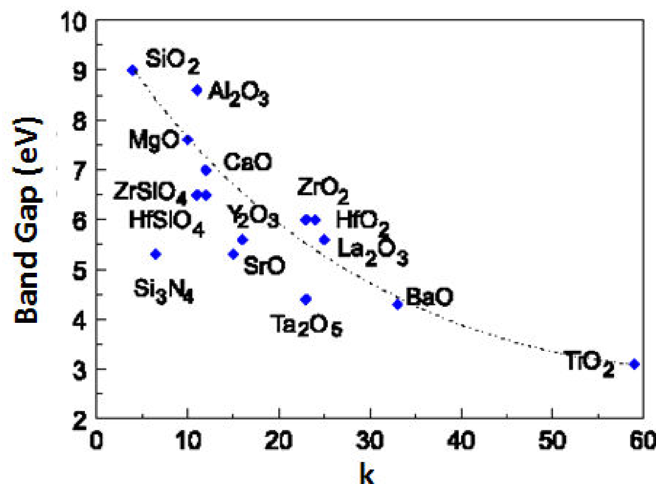


Figure 1.4 Band gap versus dielectric constant for various insulators [29]

In this work, SiO_2, Al_2O_3, and Ta_2O_5 were used to construct gate dielectrics in MOS structures. The basic properties of these oxides are briefly described below.

Silicon dioxide (SiO_2), also known as silica or silox, is the oxide of silicon. Ball-and-stick model for the crystal structure of α-quartz SiO_2 is depicted in Figure 1.5. The Si atom owns a tetrahedral coordination with 4 oxygen atoms surrounding a central Si atom. The central tetrahedron shares all 4 of its corner O atoms, the 2 face-centered tetrahedra share 2 of their corner O atoms, and the 4 edge-centered tetrahedra share just one of their O atoms with other SiO_4 tetrahedra. This leaves a net average of 12 out of 24 total vertices for that portion of the 7 SiO_4 tetrahedra that are considered to be a part of the unit cell for silica [37]. Silica is found naturally in sand or quartz, as well as in the cell walls of diatoms. Silica is manufactured in several forms, including glass (fused silica), synthetic amorphous silica, and silica gel [38]. SiO_2 is a stable native oxide that can be grown thermally on the surface of Si [39]. Alternatively, SiO_2 can be deposited on the surface of other semiconductors.

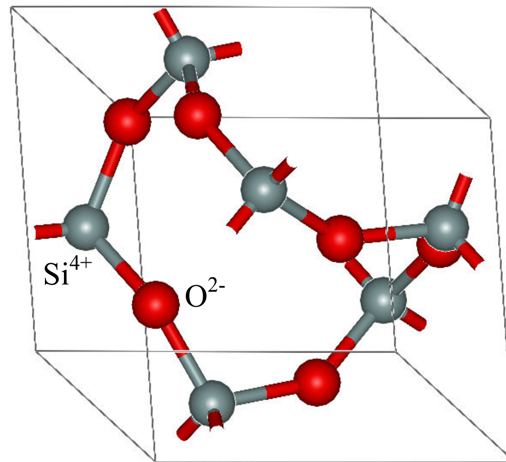


Figure 1.5 Ball-and-stick model for the crystal structure of α-quartz SiO_2 [37]

Aluminium oxide (Al_2O_3) is also referred to as alumina, aloxite, or sapphire. It is an amphoteric oxide of aluminium. The most common form of alumina is corundum (α-Al_2O_3). Ball-and-stick model for the crystal structure of α-Al_2O_3 is illustrated in Figure 1.6. Corundum possesses a trigonal Bravais lattice with a space group of R-3c. The primitive cell contains two formula units of aluminium oxide. The oxygen ions nearly form a hexagonal close-packed structure with aluminium ions filling two-thirds of the octahedral interstices. Alumina also exists

in other phases such as eta, chi, gamma, delta and theta aluminas. Each has a unique crystal structure and properties. The so-called β-alumina proved to be $NaAl_{11}O_{17}$ [40]. Al_2O_3 has high alternating current (a.c.) dielectric strength and high thermal conductivity that made it famous in power electronic applications, especially in the manufacture of electronic device substrate. For instance, high and low capacity IGBT modules are insulated by Al_2O_3. F. Talbi et al. [41] studied the direct current (d.c.) conduction of Al_2O_3 under high electric field and found a low trap density of 2 x 10^{11} cm^{-3}. The advantages of Al_2O_3 are large band gap (8.7 eV), high field strength, good chemical and thermal stabilities, resistant to ionic transport as well as compact and amorphous matrix under the conditions of interest [42].

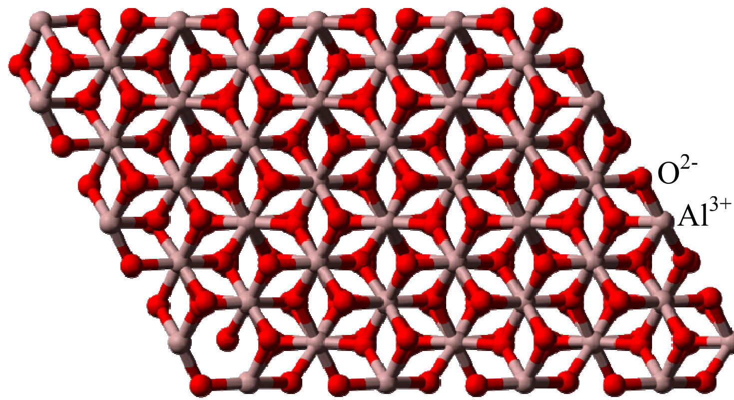


Figure 1.6 Ball-and-stick model for the crystal structure of α-Al_2O_3 [37]

Tantalum pentoxide (Ta_2O_5), also known as tantalum (V) oxide, is a material with high refractive index and low absorption. It has orthorhombic and hexagonal phases. At low temperature, it exists as β-Ta_2O_5, while it is α-Ta_2O_5 at high temperature. The transition between these two phases occurs slowly at 1360 °C and is reversible. The structures of both forms consist of chains built from octahedral and pentagonal bipyramidal polyhedra sharing opposite vertices. These chains are further joined by sharing edges to yield the 3-dimension structure [43, 44, 45]. Ball-and-stick model for the crystal structure of Ta_2O_5 is shown in Figure 1.7. Ta_2O_5 is a key high-k dielectric material used to make DRAM capacitor. This is owing to its high dielectric constant (37), high breakdown field (4.5 MV/cm), low leakage current ($<10^{-8}$ A/cm^2 at 1 MV/cm), and good step coverage [46]. Ta_2O_5 has attracted much attention for memory applications, especially in nanoscale DRAM. This is attributed to its charge storage capability, which is a few times higher than other oxides [47].

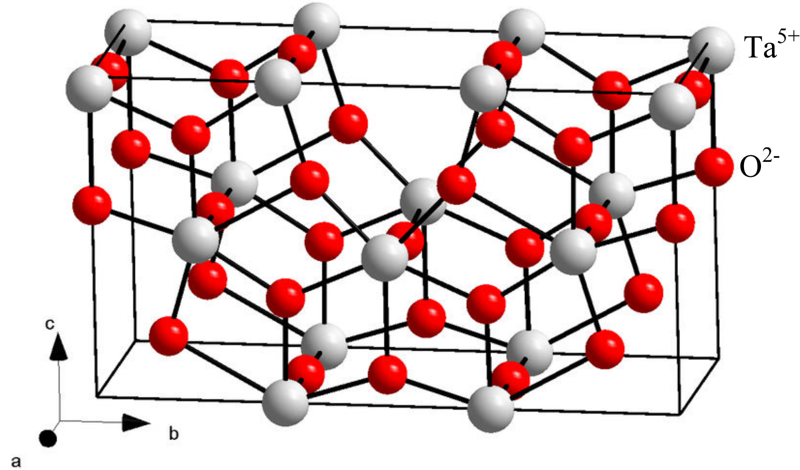


Figure 1.7 Ball-and-stick model for the crystal structure of Ta_2O_5 [48]

1.6 Problem Statement

The device miniaturization trend has caused carrier tunneling and current leakage which need to be avoided in MOS-based devices. It has been proposed the need to replace the conventional gate dielectric of SiO_2 with high-k dielectric of Ta_2O_5 so that use of thicker film is allowed without the concomitant leakage while maintaining the same capacitance density [48]. Furthermore, thicker film enables continuous scaling for a number of years which is in line to the Moore's Law. However, some researchers reported that high-k dielectric has limitation of high defect concentration and unrelaxed bonding, which may result in poor MOS characteristic [29]. If this is happened to be true, then the performance of the MOS structure will encounter degradation in the field, especially at applications dealing with high temperature and electrical biasing. On the other hand, literature about MOS structure with high-k gate dielectric of Ta_2O_5 grown on compound semiconductor of GaN is very limited. Most of the previous works were on Si-based MOS. Lack of such research works provides a motivation for us to study GaN-based MOS with Ta_2O_5 and to prove that the Al/Ta_2O_5/GaN MOS structure has better performance compared to MOS structures with other dielectrics such as SiO_2 and Al_2O_3.

1.7 Objective and Scope of Works

In earlier part of the present work, a comparative study was conducted among SiO_2, Al_2O_3, and Ta_2O_5 to extract the excellent properties of Ta_2O_5 compared to other dielectrics, such as higher oxide capacitance, lower fixed oxide charge density, lower interface trap density, etc. In the real field application, ability of a device to withstand environmental effects such as temperature, electric bias, and radiation would determine the functionality and life time of the device. This appears to be a driving force and source of motivation for us to perform comprehensive case studies in the later part of the work to determine the robustness of the $Al/Ta_2O_5/GaN$ MOS structure when subjected to the above environmental stresses. The objective of each case study is described as below:

- Effect of post-deposition annealing (PDA): To study the effect of PDA temperature on the grain structure of Ta_2O_5 and to determine the ideal range of annealing temperature for the $Al/Ta_2O_5/GaN$ MOS structure in order to maintain Ta_2O_5 at amorphous stage
- Effect of post-metallization annealing (PMA): To study the effect of PMA on the $Al/Ta_2O_5/GaN$ MOS structure and to investigate the mechanism of thermal-induced damage
- Effect of substrate temperature: To study the effect of substrate temperature on the $Al/Ta_2O_5/GaN$ MOS structure and to prove that it is robust against temperature stress
- Effect of constant voltage stress (CVS): To study the effect of CVS on the $Al/Ta_2O_5/GaN$ MOS structure and to prove that it is robust against electrical stress
- Effect of visible light radiation: To study the effect of the radiation on the $Al/Ta_2O_5/GaN$ MOS structure and to prove that it is robust against radiation

1.8 Arrangement of the Thesis

Chapter 1 discusses the properties of GaN, SiO_2, Al_2O_3, and Ta_2O_5, which are the materials of semiconductor and oxides used in the present work. Literature review on GaN-based MOS with various dielectrics is provided, together with the research progress and research issue over the last few years. In addition, problem statement, objectives, and scope of works related to GaN-based MOS are also given.

Chapter 2 presents the fundamentals of MOS, where the basic theories and concepts of MOS are discussed in details. A lot of useful equations are listed, which will be applied in the analysis of the experimental works in Chapter 4 and Chapter 5. Current transport mechanisms through the gate dielectric are introduced as well. Besides that, brief introductions on temperature stress, electrical stress, and radiation stress are given in the last section of this chapter.

Chapter 3 covers the discussion on experimental procedures. There are three main categories. The first category is the fabrication process, including RCA cleaning, dielectric sputtering, metal evaporation, and thermal annealing. The second category is physical analysis using a variety of tools such as AFM, XRD, XRF, FESEM, EDX, and FIB. The third category is electrical analysis which is consisting of four-point probing, TIVA fault isolation, C-V and I-V measurements.

Chapter 4 presents the comparative study among three different MOS structures, namely Al/SiO_2/GaN, Al/Al_2O_3/GaN, and Al/Ta_2O_5/GaN. The fundamental characteristics of each MOS structure are evaluated using the concepts and formulas provided in Chapter 2. This chapter will prove that Al/Ta_2O_5/GaN is the best MOS structure. Moreover, important parameters that demonstrate the advantages of Al/Ta_2O_5/GaN are highlighted.

Chapter 5 is the core chapter that is focused on the Al/Ta_2O_5/GaN MOS structure. A few case studies are performed to understand the MOS behavior under the influence of external factors like annealing temperature, substrate temperature, electrical stress, and visible light radiation. In each section, comprehensive research results and in-depth technical discussions are presented.

Chapter 6 is the conclusion chapter that summarizes all the research findings. Future plan for improvement purpose is also included.

CHAPTER 2

Fundamentals of MOS

2.1 Introduction

Metal-Oxide-Semiconductor (MOS) is a two-terminal device comprises of an oxide sandwiched between a metal and a semiconductor. A conventional MOS is usually made of aluminium (Al) (or heavily doped polycrystalline silicon) - silicon dioxide (SiO_2) – silicon (Si). The first terminal is a field plate called gate connected to the oxide where electrical bias is normally applied. The second terminal is also a metallic layer which provides electrical contact to the semiconductor backside and is normally grounded (Figure 2.1) [1].

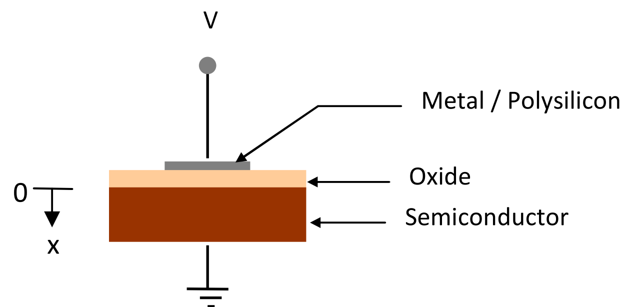


Figure 2.1 Cross-sectional view of a MOS structure

2.2 Explicit Properties of an Ideal MOS

A total of eight assumptions are made for an ideal MOS [1]:

1) The metallic gate is sufficiently thick so that it can behave as an equipotential region under alternating current (a.c.) and direct current (d.c.) biasing conditions.
2) The oxide is a perfect insulator with infinite resistivity such that no carriers transport through the oxide under all static biasing conditions.
3) The semiconductor is uniformly doped.
4) The semiconductor is sufficiently thick so that a field-free regime (known as silicon bulk) is encountered before reaching the backside contact under any applied gate bias.
5) The contact between the semiconductor and the backside metallic plate is Ohmic.
6) Charges only present in the semiconductor and on the metal surface adjacent to the oxide at any biasing condition.

7) The MOS structure is one dimensional structure with all variables taken to be a function only of the x-coordinate (Figure 2.1).
8) The work function difference between metal and semiconductor ($q\phi_{ms}$) is zero at zero bias. In other words, the energy bands are flat when there is no applied voltage (flat-band condition). The meaning of each symbol in equation (2-1) is explained in Figure. 2.2.

$$q\phi_{ms} = q\phi_m - q\phi_s = q\phi_m - (q\chi + E_g/2 - q\Psi_B) \quad (2\text{-}1)$$

2.3 Energy Band Diagram at Zero Bias

The formation of the MOS energy band diagram first requires both metal and semiconductor to be brought together at a distance x_o apart from each other. Both are allowed to equilibrate so that their Fermi levels are aligned at the same energy. In addition, the vacuum levels of both the metal and the semiconductor must be in alignment as well because $\phi_m = \phi_s$. It is assumed that charge or electric field does not exist in the MOS system. Next, an insulator with thickness t_{ox} is inserted into the empty space between the metal and the semiconductor. This lowers the energy barrier between the two. Figure 2.2 illustrates the energy band diagram of an ideal n-type semiconductor MOS at zero bias, with the metal work function $q\phi_m$ equals the semiconductor work function $q\phi_s$. Work function is the energy difference between the Fermi level and the vacuum level. The vacuum level denotes the minimum energy (E_o) where an electron must have to completely free itself from the material. Electron affinity $q\chi$ is the energy difference between the conduction band edge and the vacuum level in the semiconductor, that is, the height of the surface energy barrier. On the other hand, $q\Psi_B$ is the energy difference between the Fermi level E_F and the intrinsic Fermi level E_i [1, 49].

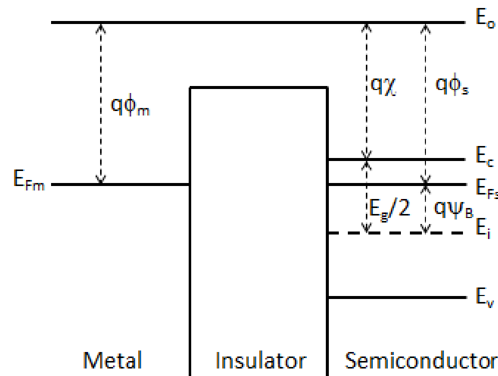


Figure 2.2 Energy band diagram of an ideal n-type MOS at $V_G = 0$ [1, 49]

2.4 Energy Band Diagram at Non-Zero Bias

Assume that V_G is the d.c. bias applied to the gate while the semiconductor backside is grounded. $V_G \neq 0$ causes potential drops and E_c (E_v) band bending interior to the MOS, where the energy bands in the semiconductor encounter an upward slope (increasing E going from the gate toward the backside contact) when $V_G > 0$ and a downward slope when $V_G < 0$. Nevertheless, the semiconductor Fermi level is unaffected by the bias and remains invariant as a function of position owing to zero current flow under all static biasing conditions. In contrast, there is no bending in the metal as it is an equipotential region. Furthermore, the conduction and valence energy bands in the oxide are linear functions of position because electric field in the oxide is a constant. The bias separates the Fermi energies of the metal and the semiconductor by an amount equal to qV_G.

$$E_F\text{ (metal)} - E_F\text{ (semiconductor)} = -qV_G \qquad (2\text{-}2)$$

When a positive bias ($V_G > 0$) is applied to the gate, positive charges Q_M are placed on the gate and equivalent amount of negative charged electrons Q_s will be drawn towards the oxide-semiconductor interface. E_F of the metal is lowered relative to E_F of the semiconductor. This induces positive sloping of energy bands in the oxide and the semiconductor. In other words, bands near the semiconductor surface are bent downward and cause an increase in the energy E_F - E_i. Since $n = n_i \exp[(E_F - E_i)/k_BT]$, the electron concentration at the oxide-semiconductor interface is enhanced and is greater than the majority carrier concentration in the bulk of the semiconductor. This condition is known as accumulation (Figure 2.3a). The accumulation capacitance is given by

$$C\text{ (accumulation)} \approx C_{ox} = k_{ox}\, \varepsilon_o\, A / t_{ox} \qquad (2\text{-}3)$$

When a small negative bias ($V_G < 0$) is applied to the gate, E_F of the metal is raised slightly relative to E_F of the semiconductor. This induces negative sloping of energy bands in the oxide and the semiconductor, where bands near the semiconductor surface are bent upward. $V_G < 0$ places negative charges $-Q_M$ on the gate. This repels electrons away from the oxide-semiconductor interface and exposes the positively charged donor sites $+Q_{sc}$. Since the majority carriers are depleted in the vicinity of the oxide-semiconductor interface such that its concentration is less than the background doping concentration, it is thus known as depletion (Figure 2.3b). The depletion capacitance is modeled by

$$C \text{ (depletion)} = C_{ox} C_s / (C_{ox} + C_s) \quad (2\text{-}4)$$

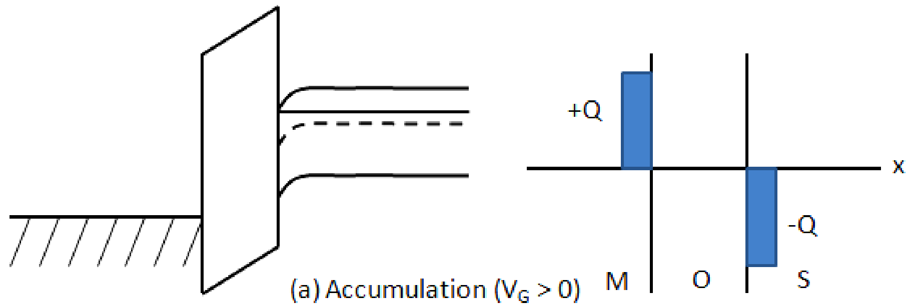
When a larger and larger negative bias ($V_G << 0$) is applied to the gate, the bands at the semiconductor surface will bend up more and more. The hole concentration at the surface (p_s) will increase from less than n_i when E_i (surface) < E_F, to n_i when E_i (surface) = E_F, to greater than n_i when E_i (surface) > E_F. Finally, p_s will increase to the point where

$$E_i \text{ (surface)} - E_i \text{ (bulk)} = 2 [E_F - E_i \text{ (bulk)}] \quad (2\text{-}5)$$

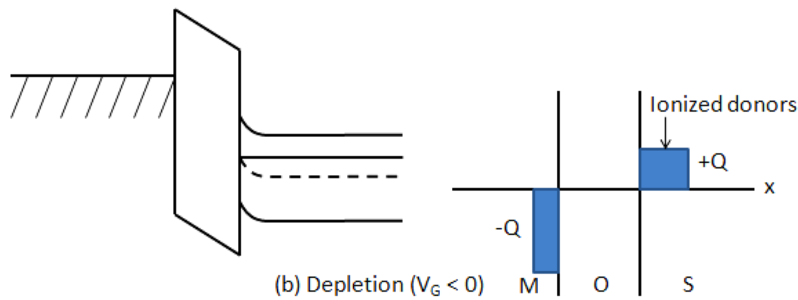
$$p_s = n_i e^{[E_i(\text{surface}) - E_F]/k_B T} = n_i e^{[E_F - E_i(\text{bulk})]/k_B T} = n_{bulk} = N_D \quad (2\text{-}6)$$

The surface is no longer depleted when $p_s = N_D$ at $V_G = V_T$. When the negative bias ($V_G < V_T$) further increases until p_s exceeds $n_{bulk} = N_D$, the surface character changes from n-type to p-type, where the minority carrier concentration at the surface is greater than the bulk majority carrier concentration. The surface is inverted and this condition is called inversion. During inversion, most of the additional positive charges in the semiconductor comprise of the charge in a narrow p-type inversion layer of width x_i. The typical x_i value is 1-10 nm and is always smaller than the surface depletion layer width. At strong inversion, the bands are bent upward far enough such that a small increase in band banding corresponds to a small increase in depletion layer width, but a large increase in the inversion layer charge. Under strong inversion, the layer width reaches a maximum value of W_m, while the charge per unit area in the semiconductor Q_s is the sum of the charge in the inversion layer Q_p and the charge in the depletion layer Q_{sc} [49].

$$Q_s = Q_p + Q_{sc} = Q_p + qN_DW_m \quad (2\text{-}7)$$



(a) Accumulation ($V_G > 0$)



(b) Depletion ($V_G < 0$)

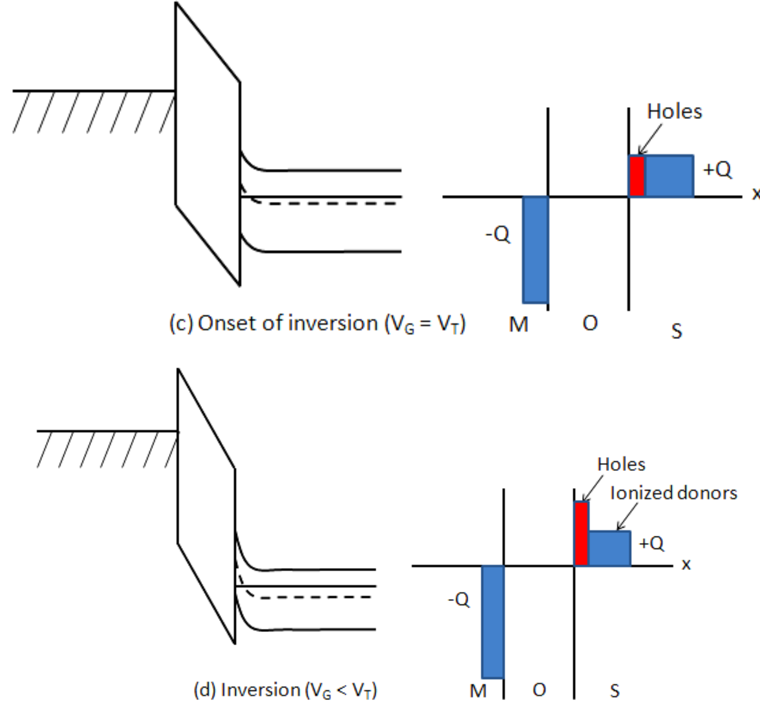


Figure 2.3 Energy band diagrams and charge distributions of an ideal n-type MOS at $V_G \neq 0$ [49]

2.5 Semiconductor Electrostatics

Charge in the vicinity of the metal-oxide interface resides only a few Angstroms into the metal and it can be assumed as a δ-function of charge at the metal-oxide interface. The magnitude of charge in the metal is equal to the sum of charges inside the semiconductor. Since there is no charge in the oxide, electric field is constant in the oxide and the potential is a linear function of position. Hence, the electrostatic of the MOS is representing by the electrostatic in the semiconductor and it can be analyzed by solving the Poisson's equation.

Given that $\Psi(x)$ is the electrostatic potential inside the semiconductor at a given point x, where x is the depth into the semiconductor measured from the oxide-semiconductor interface. Ψ is zero in the field-free region of the semiconductor bulk. Ψ_s is the surface potential at x = 0. Figure 2.4 illustrates a detailed band diagram at the surface of an n-type MOS [49].

$$\Psi(x) = 1/q\ [E_i(bulk) - E_i(x)] \quad (2\text{-}8)$$

$$\Psi_s = 1/q\ [E_i(bulk) - E_i(surface)] \quad (2\text{-}9)$$

$$\Psi_B = 1/q\ [E_i(bulk) - E_F] \quad (2\text{-}10)$$

For a non-degenerate semiconductor substrate, the hole concentration in the bulk, p_{bulk} and the electron concentration in the bulk, n_{bulk} are given by [49]

$$p_{bulk} = n_i \exp \{[E_i(bulk) - E_F] / k_BT\} = N_A, \text{ for } N_A >> N_D, \quad (2\text{-}11)$$

$$n_{bulk} = n_i \exp \{[E_F - E_i(bulk)] / k_BT\} = N_D, \text{ for } N_D >> N_A \quad (2\text{-}12)$$

By combining equations (2-10) to (2-12), we obtain

$$\Psi_B = (k_BT/q) \ln (N_A/n_i) \text{ for p-type semiconductor} \quad (2\text{-}13)$$

$$\Psi_B = -(k_BT/q) \ln (N_D/n_i) \text{ for n-type semiconductor} \quad (2\text{-}14)$$

where $\Psi_s < 0$ Accumulation of electrons (bands bend downward)

$\Psi_s = 0$ Flat-band condition

$0 < \Psi_s < 2\Psi_B$ Depletion of electrons (bands bend upward)

$\Psi_s = \Psi_B$ Mid gap with $p_s = p_n = n_i$

$\Psi_s > 2\Psi_B$ Inversion (bands bend upward)

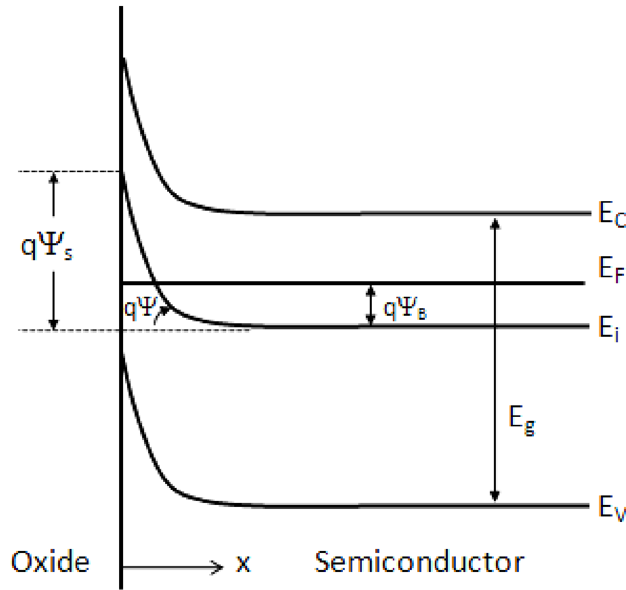


Figure 2.4 Energy band diagram at the surface of an n-type MOS [49]

The electron and hole concentrations can be expressed as a function of Ψ as follow [49]:

$$n_n = n_i \exp (q\Psi - q\Psi_B) / k_BT \quad (2\text{-}15)$$

$$p_n = n_i \exp (q\Psi_B - q\Psi) / k_BT \quad (2\text{-}16)$$

$$n_s = n_i \exp (q\Psi_s - q\Psi_B) / k_BT \quad (2\text{-}17)$$

$$p_s = n_i \exp (q\Psi_B - q\Psi_s) / k_BT \quad (2\text{-}18)$$