

**INVESTIGATION OF METAL-ORGANIC DECOMPOSED
(MOD) CERIUM OXIDE (CeO₂) GATE DEPOSITED ON
SILICON AND GALLIUM NITRIDE SUBSTRATES VIA SPIN-
ON COATING TECHNIQUE**

by

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**Thesis submitted in fulfillment of the requirements
for the Degree of Master of Science**

June 2010

ACKNOWLEDGEMENT

I would like to express my greatest gratitude to my supervisors, Assoc. Prof. Ir. Dr. Cheong Kuan Yew and Prof. Zainuriah Hassan, who had provided guidance and advice to me in terms of technical and theory when this research was being carried out. Besides that, I would also like to wish Dr. Zainovia Lockman for her worthy advices in solving the encountered difficulties during this research.

Furthermore, I felt grateful to the Dean of School of Materials and Mineral Resources Engineering, Prof. Dr. Ahmad Fauzi Mohd Noor, and all the academic, administrative, and technical staffs for their endless supports and assistances. Specially appreciation was given to Mr. Suhaimi, Mr. Rashid, Madam Fong, Mr. Azam, and Mr. Zaini as well as all the technical staffs of NOR lab of School of Physics (Mr. Azhar, Mr. Mohtar, Mr. Jamil, and Madam Ee) for their valuable technical supports and assistances.

I would like to thank my family members and friends for their endless encouragements and supports in making this research a reality. Last but not least, I greatly appreciated the financial support from Universiti Sains Malaysia Short Term grant (6035269), Universiti Sains Malaysia Research Universiti grant (8031012), and USM fellowship.

QUAH HOCK JIN

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LIST OF ABBREVIATION

AFM	: Atomic force microscopy
Ar	: Argon
CeO ₂	: Cerium oxide
Ce ₂ Si ₂ O ₇	: Cerium silicate
CSD	: Chemical solution deposition
FESEM	: Field emission scanning electron microscope
FG	: Forming gas
GaN	: Gallium nitride
ICCD	: International conference for diffraction data
IL	: Interfacial layer
LCR	: Inductance-capacitance-resistance
MOD	: Metal-organic decomposition
MOS	: Metal oxide semiconductor
O ₂	: Oxygen
Si	: Silicon
SiC	: Silicon carbide
SiO ₂	: Silicon dioxide
SPA	: Semiconductor parameter analyzer
XRD	: X-ray diffraction

LIST OF SYMBOLS

A_G	: Capacitor area (cm^2)
C_{ox}	: Oxide capacitance (pF)
D_{it}	: Interface trap density ($\text{eV}^{-1} \text{cm}^{-2}$)
E_B	: Electric breakdown field (MV cm^{-1})
I	: Current (A)
J	: Current density (A cm^{-2})
K	: Dielectric constant
θ	: Angle
ϕ_B	: Barrier height
q	: Charge (C)
Q_{eff}	: Effective oxide charge
V	: Voltage (V)
V_B	: Breakdown voltage (V)
STD	: Slow trap density (cm^{-2})
E_C	: Conduction band (eV)
E_F	: Fermi energy (eV)
E_V	: Valance band (eV)
ρ	: Oxide density (g cm^{-2})
D	: Crystallite size (nm)
β	: Full width at half maximum

LIST OF PUBLICATIONS

1. Quah, H. J., Cheong, K. Y., Hassan, Z., Lockman, Z., Janis, F. A. and Lim, W. F. (2010). Effect of Postdeposition Annealing in Argon Ambient on Metallorganic Decomposed CeO₂ Gate Spin Coated on Silicon. Journal of the Electrochemical Society, 157, pp. H6-H12. (Impact Factor: 2.437).
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3. Quah, H. J., Cheong, K. Y., Hassan, Z. and Lockman, Z. (2010). MOS Characteristics of Metal-Organic Decomposed CeO₂ Spin-Coated on GaN. Electrochemical and Solid-State Letters, 13, pp. H116-H118. (Impact Factor: 2.001).

**KAJIAN TENTANG LAPISAN FILEM OKSIDA SERIUM (CeO_2)
YANG DISEDIAKAN MELALUI TEKNIK PENGURAIAN
ORGANIK LOGAM (MOD) YANG DISALUTKAN KE ATAS
SUBSTRAT SILIKON DAN GALIUM NITRIDA MELALUI
TEKNIK SALUTAN PUTAR**

ABSTRAK

Prapenanda CeO_2 yang disediakan dengan teknik penguraian organik logam telah diserakkan ke atas wafer Si dan GaN berjenis n dengan ketebalan dalam lingkungan 45-90 nm. Larutan prapenanda disediakan dengan menggunakan serium (III) acetylacetonate hidrat, metanol, dan asid asetik sebagai bahan pemula. Kesan sepuhlindap telah dijalankan ke atas filem CeO_2 yang disalutkan pada wafer Si pada suhu-suhu yang berlainan (600, 800 dan 1000 °C) di bawah aliran gas argon. Penyejukan secara perlahan seterusnya dijalankan sehingga sampel disejukkan ke suhu bilik. Pelbagai atmosfera sepuhlindap seperti aliran gas argon, gas campuran (campuran H_2 dan N_2), dan gas oksigen, serta suhu sepuhlindap (400, 600, 800 dan 1000 °C) telah diaplikasikan untuk mengkaji kesan-kesan terhadap filem CeO_2 yang disalutkan ke atas wafer GaN. Analisis pembelauan sinar-X (XRD) telah berjaya mengesan CeO_2 , $\alpha\text{-Ce}_2\text{O}_3$, dan silikat serium ($\text{Ce}_2\text{Si}_2\text{O}_7$) dalam sistem CeO_2/Si . Di samping itu, kelakuan mirip epitaksi berorientasikan (200) telah dipaparkan oleh sampel yang disepuhli pada 600 °C. Dominasi satah (200) untuk filem ini kemudiannya menjadi semakin berkurangan dan diambil alih oleh satah (111) yang dominasinya meningkat apabila suhu sepuhlindap semakin meningkat. Keputusan XRD bagi filem CeO_2 yang disalutkan ke atas GaN menunjukkan kehadiran β -oksida gallium ($\beta\text{-Ga}_2\text{O}_3$) selain daripada CeO_2 . Pengukuran ellipsometri telah dijalankan untuk mengambil bacaan ketebalan dan indeks biasan untuk filem CeO_2 .

Pencirian bagi kapasitor logam-oksida-semikonduktor Al/CeO₂/Si dan Al/CeO₂/GaN telah dijalankan dengan menggunakan pengukuran arus-voltan (I-V) dan kapasitan-voltan (C-V). Kegagalan voltan yang paling tinggi telah diperoleh CeO₂/Si yang disepuhlandap pada suhu 1000 °C. Untuk CeO₂ yang disalutkan pada GaN, sampel yang disepuhlandap pada suhu 1000 °C dalam atmosfera argon dan oksigen mempunyai kegagalan medan elektrik yang tertinggi. Manakala bagi CeO₂/GaN yang disepuhlandap dalam atmosfera gas campuran pada suhu yang sama, kegagalan medan elektrikny adalah yang paling rendah. Ketumpatan perangkap antaramuka, ketumpatan cas oksida, ketumpatan perangkap lambat, dan ketinggian benteng, Φ_B bagi oksida-semikonduktor telah dikira dan dikaitkan dengan kegagalan medan elektrik lapisan filem yang dikaji. Penimbusan Fowler-Nordheim (FN) juga telah dikaji untuk sampel yang berkeupayaan untuk menampung medan elektrik yang tinggi.

INVESTIGATION OF METAL-ORGANIC DECOMPOSED (MOD) CERIUM OXIDE (CeO_2) GATE DEPOSITED ON SILICON AND GALLIUM NITRIDE SUBSTRATES VIA SPIN-ON COATING TECHNIQUE

ABSTRACT

Metal-organic decomposed (MOD) CeO_2 precursor has been spin coated on n-type Si and n-type GaN substrates with thickness in the range of 45-90 nm. This precursor has been prepared by cerium (III) acetylacetonate hydrate, methanol, and acetic acid as the starting materials. The effect of post-deposition annealing at different temperatures (600, 800 and 1000 °C) under the flow of argon gas has been performed on the MOD-derived CeO_2 films on Si. Slow cooling at 5 °C/min was then accomplished for samples to cool down to room temperature. Post-deposition annealing temperatures (400, 600, 800 and 1000 °C) at three different ambients [argon, forming gas (mixture of H_2 and N_2), and oxygen] have been employed to investigate the effect of these parameters on CeO_2 films spin-coated on GaN substrate. X-ray diffraction (XRD) has detected the presence of CeO_2 , $\alpha\text{-Ce}_2\text{O}_3$, and cerium silicate ($\text{Ce}_2\text{Si}_2\text{O}_7$) in CeO_2/Si system. Besides, epitaxial-like (200) oriented CeO_2 film has been produced in sample annealed at 600 °C and the dominance of this plane ceased with the increase of annealing temperature. While XRD characterization performed on CeO_2 film deposited on GaN revealed the presence of β -gallium oxide ($\beta\text{-Ga}_2\text{O}_3$) besides CeO_2 . Ellipsometry measurements have been carried out on the investigated samples to acquire the film thickness and refractive index. Metal-oxide-semiconductor characteristics of Al/ CeO_2 /Si and Al/ CeO_2 /GaN capacitors have been investigated based on current-voltage (I-V) and capacitance-voltage (C-V) measurements. It has been noticed that the highest dielectric

breakdown voltage has been obtained for 1000 °C annealed CeO₂ gate oxide deposited on Si substrate. Besides that, the highest dielectric breakdown field has also been observed for 1000 °C annealed CeO₂ gate oxide deposited on GaN substrate in argon and oxygen ambients. A contrary result has been obtained for CeO₂/GaN system annealed in forming gas ambient, wherein the sample annealed at 1000 °C has the lowest dielectric breakdown field. Semiconductor-oxide interface-trap density, effective oxide charge, slow trap density, and barrier height have been calculated and correlated with electric breakdown field of the investigated oxides. Fowler-Nordheim tunneling has been taken into consideration for samples that were able to sustain high electric field.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Substantial development in silicon technology and design of new device structures have yet conformed to the endless demand for higher current and voltage handling capacity. Eventually, the Si-based power devices have been pushed to their theoretical limits, meaning that they will not be able to handle the requirements needed in future power electronics, such as high switching frequency, high blocking voltage, high efficiency and reliability (Yu et al., 2008). Therefore, it is crucial to seek for other semiconducting materials providing the device performance can be further enhanced.

Alternative semiconductor materials have arisen in replacing Si with higher breakdown field and wider band gap. This can be accomplished by using wide band gap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) (Barcena et al., 2008; Calame et al., 2007). Unlike Si technology, devices based on wide band gap semiconductors are capable of operating under high temperature and hostile environments (Mohammad and Morkoc, 1996). However, SiC forms a formidable challenge to nitrides in demonstrating device performance for power amplification. In SiC materials, “micropipe” defects are commonly found, hampering its performance. Therefore, III-V nitride semiconductors, such as GaN, have become the wise choices to compete with SiC.

GaN is preferred due to its larger band gap (3.4 eV), large critical electric field (3 MV/cm), high electron mobility, as well as good thermal conductivity and stability (Chang et al., 2007; Zhou et al., 2008; Huang et al., 2006; Lee et al., 2006; Matocha et al., 2005; Lin and Lai, 2007). Thus, it has been regarded as a potential semiconductor material for high power devices, delivering the device performance of SiC but with considerably cheaper substrate. On the other hand, GaN provides direct band gap heterostructures, which allow carrier confinement and the placement of carriers at the interfaces. Besides, it forms good ohmic contacts imperatively for power devices (Mohammad and Morkoc, 1996). It is anticipated that ultimately GaN will turn out to be more promising than SiC for high power applications due to the advantages offered by GaN. However, further development in GaN has been obstructed due to the absence of native substrates with close lattice match to this material. This is due to the costly development of homoepitaxy of GaN on bulk GaN. In order to achieve the potential performance, alternative substrates, such as sapphire, SiC, Si, ZnO, germanium, glass, LiGaO₂ and LiAlO₂, are used (Bishop et al., 2007; Caban et al., 2008; Calame et al., 2007; Craven et al., 2004; Tamura et al., 2008).

The novel properties provided by GaN have promised it to be used as the electronic substrate for high power and high temperature GaN-based metal-oxide-semiconductor (MOS) devices (Arulkumaran et al., 1998; Chang et al., 2008; Chang et al., 2007, Chow, 2006; Huang et al., 2006; Hwang and Lin, 2009; Kim et al., 2001; Lee et al., 2006; Liu et al., 2006; Matocha et al., 2003; Matocha et al., 2007; Nakano and Jimbo, 2002; Nakano and Jimbo, 2003; Shur, 1998; Wu et al., 2007; Zhou et al., 2008). In order to fabricate these devices, a high quality gate oxide

acting as an insulating layer for the gate to sustain a high transverse electric field is required (Cheong et al., 2008).

Metal-organic decomposition method is a wet chemical route, which can be used to prepare a precursor that will transform to an oxide film through heat treatment. It utilizes large carboxylate and strong chelating ligand to form a precursor solution. It is cost-effective in synthesizing electronic oxide thin films. This is owing to its capability of producing stable precursor with precise control of its composition by using both the water-insensitive carboxylate and chelating ligand without the involvement of complex chemical reaction. β -diketonate (acetylacetonate-type) compounds are the chelating ligands commonly used in MOD method (Bhuiyan et al., 2006; Morlens et al., 2003; Schwartz et al., 2004).

1.2 Problem Statement

Relatively low dielectric constant (k) material, such as SiO_2 has been employed as the gate oxide in GaN-based MOS devices (Arulkumaran et al., 1998; Huang et al., 2006; Hwang and Lin, 2009; Lee et al., 2008; Matocha et al., 2003; Matocha et al., 2007; Nakano and Jimbo, 2002; Niiyama et al., 2007). However, since the application is for high power, conventional SiO_2 is not suitable to be deposited on GaN. This is attributed to the low electric breakdown field of SiO_2 , which is insufficient to sustain high electric breakdown field of GaN (Cheong et al., 2008). In order to overcome this shortcoming, high- k materials, such as Ga_2O_3 (Fu and Kang, 2002; Kim et al., 2001; Lee et al., 2006; Lin et al., 2006; Nakano and Jimbo, 2003; Zhou et al., 2008), Ta_2O_5 (Tu et al., 2000), MgO (Chen et al., 2006; Craft et al., 2007; Kim et al., 2002), Al_2O_3 (Chang et al., 2008; Chang et al., 2009;

Ostermaier et al., 2008; Wu et al., 2007), Si_3N_4 (Arulkumaran et al., 1998), $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ (Chang et al., 2007; Lay et al., 2001; Lay et al., 2005; Ren et al., 1998), Gd_2O_3 (Chang et al., 2009; Gila et al., 2001; Lay et al., 2005), Sc_2O_3 (Allums et al., 2007; Gila et al., 2001; Liu et al., 2006), and HfO_2 (Chang et al., 2007; Shih et al., 2009), have been deposited on GaN substrate. With these materials, the beneficial usage of utilizing GaN as the substrate for high power application can be exploited.

Rare-earth cerium oxide (CeO_2), which is available in three phases, such as CeO_2 with cubic fluorite (CaF_2) structure as well as Ce_2O_3 with hexagonal and cubic structures, is also considered as a potential candidate of substituting SiO_2 (Adachi and Imanaka, 1998; Yamamoto et al., 2005). CeO_2 with cubic fluorite structure consists of eight equivalent O^{2-} anions surrounding each Ce^{4+} cation forming the corner of a cube, with each O^{2-} anion coordinated to four Ce^{4+} cations (Chen et al., 2007; Deshpande et al., 2005; Triguero et al., 1999). It is gaining interest as an alternative gate oxide due to its novel properties, including large band gap (~ 6 eV), high thermal and chemical stability, and high dielectric constant ($k = 15-26$), in which the k values depend on deposition techniques (Barnes et al., 2006; Fukuda et al., 1998; Kang et al., 2001; Inoue et al., 1999; Ta et al., 2008; Wang et al., 1999; Wang et al., 2004; Wei and Choy, 2005). In addition, phase transformation was reported to occur in pulsed-laser deposited CeO_2 on Si (Hirschauer et al., 1999; Wang et al., 1999) and molecular beam deposited CeO_2 on germanium (Ge) substrate (Brunco et al., 2007; Dimoulas et al., 2007). This is due to the ability of CeO_2 to continuously transform between the oxygen-rich CeO_2 and the oxygen-poor Ce_2O_3 depending on the oxygen concentration of the in-situ deposition heating and

post-deposition annealing ambient (Barnes et al., 2006; Brunco et al., 2007; Chen et al., 2007; Deshpande et al., 2005; Dimoulas et al., 2007; Hirschauer et al., 1999; Skorodumova et al., 2001; Tsunekawa et al., 2004; Wang et al., 2000; Yamamoto et al., 2005; Zhang et al., 2004). Wang et al. (1999) reported that pulsed-laser deposited CeO₂ film is partially transformed into metastable phase of amorphous Ce₂O₃ at an oxygen pressure lower than 2×10^{-5} Pa, while a reversed phase transformation may happen at an oxygen pressure of 5×10^{-3} Pa. A similar phase transformation has also been reported by Hirschauer et al. (1999) but at a higher oxygen pressure. This transformation is due to the tendency of CeO₂ to release oxygen to form oxygen vacancies, where the cerium valence state is reduced from +4 to a lower state (+3) (Chen et al., 2007; Yamamoto et al., 2005). The effect of having this metastable phase on MOS characteristics is not yet fully understood and not much work has been reported.

During post-deposition annealing, besides the formation of CeO₂, an interfacial layer between the CeO₂ and the semiconductor may also be formed. This formation relies on the annealing ambient. It has been reported previously that a layer of SiO₂ interface was formed in the DC sputtered (Yoo et al., 2001) and metal-organic decomposed (Fukuda et al., 1998) CeO₂ deposited on Si when post-deposition annealing was performed in oxygen ambient. However, when post-deposition annealing was carried out in vacuum ambient for electron-beam evaporated CeO₂ on Si, a cerium silicate (Ce₂Si₂O₇) interfacial layer was formed (Barnes et al., 2006). The effect of this Ce₂Si₂O₇ layer on the MOS characteristics has not been reported. Apart of these, the formation of interfacial layer was also reported in CeO₂ deposited on Ge substrate (Brunco et al., 2007; Dimoulas et al.,

2007; Rahman et al., 2008). In reducing ambient, which is in the presence of forming gas (95 % N₂ + 5 % H₂), Ge-O-Ce interfacial layer had been formed in electron-beam evaporated CeO₂ on Ge (Dimoulas et al., 2007; Rahman et al., 2008). While, the formation of GeO_x interfacial layer was being observed in in-situ deposition heating of molecular beam deposited CeO₂ on Ge substrate under ultrahigh vacuum condition (Brunco et al., 2007; Dimoulas et al., 2007). It was proposed that the formation of interfacial layer (GeO_x or Ge-O-Ce) was due to the phase transformation of CeO₂ (Ce⁴⁺) to Ce₂O₃ (Ce³⁺) that would release oxygen and react with the Ge (Brunco et al., 2007; Dimoulas et al., 2007).

Interfacial layer formation has provided benefits in MOS applications. The beneficial effects of having interfacial layer on both CeO₂/Si and CeO₂/Ge MOS structures had been reported (Brunco et al., 2007; Dimoulas et al., 2007; Fukuda et al., 1998; Rahman et al., 2008; Yoo et al., 2001). The increment of interfacial layer thickness with increasing annealing temperature and time may further reduce the leakage current (Brunco et al., 2007; Fukuda et al., 1998; Yoo et al., 2001). These advantages had also been presented in HfO₂/Si or ZrO₂/Si MOS structures, where the presence of metal silicate would significantly reduce the effect of dielectric polarization. As a result, the metal silicate was less susceptible to breakage and leakage even though the effective k value had been reduced due to the reduction of molecular bonds distortion and soft optical phonon scattering. Thus, higher oxide breakdown field and higher channel carrier mobility with lower leakage current could be obtained (Ahn et al., 2004; Filipescu et al., 2004; Robertson, 2004; Schlom et al., 2008; Wilk et al., 2001; Wong et al., 2006).

In this work, metal-organic decomposition (MOD) technique has been used to prepare CeO₂ precursor. Subsequently, CeO₂ is deposited on Si and GaN via spin on coating technique and post-deposition annealing must be performed to solidify the film. Reports related to the annealing in oxygen ambient are very common. However, there is no report on the effects of argon (Ar) annealing on the MOD-derived CeO₂ film on Si (100) substrate. Therefore, the effects of post-deposition annealing temperature (600, 800, and 1000 °C) on the physical and electrical properties of CeO₂ films in Ar ambient have been systematically investigated throughout this study. In addition, the beneficial effect of having an interfacial layer in reducing the leakage current while enhancing the oxide breakdown field in CeO₂/Si and CeO₂/Ge systems has stimulated the interest to have a better understanding on the CeO₂/GaN interface, which has not been reported. As a result, the effects of post-deposition annealing temperatures (400, 600, 800, and 1000 °C) at 3 different ambients [inert (argon), reducing (forming gas), and oxidizing (oxygen)] on the physical and electrical characteristics of MOD-derived CeO₂ film deposited on GaN have been investigated.

1.3 Objectives of the Research

Objectives of the present study are as follow:

1. To study the effect of post-deposition annealing temperatures (600, 800, and 1000 °C) in Argon ambient on the MOD derived CeO₂ films deposited on Si substrate.
2. To study the effect of post-deposition annealing temperatures (400, 600, 800, and 1000 °C) in 3 different ambients [inert (argon), reducing (forming gas), and

oxidizing (oxygen)] on the MOD derived CeO₂ films deposited on GaN structure.

3. To study the effect of interfacial layer formed in between CeO₂ gate oxide deposited on Si and GaN substrates in improving the oxide breakdown field, while reducing the leakage current in CeO₂/Si and CeO₂/GaN systems.

1.4 Scope of the Research

In this work, cerium (III) acetylacetonate hydrate, methanol, and acetic acid have been utilized to derive CeO₂ precursor via MOD technique. Then, spin on coating technique has been used to deposit CeO₂ thin films on Si and GaN substrates. The effects of post-deposition annealing temperatures and ambients on the MOD-derived CeO₂ films spin coated on Si and GaN substrates have been performed. The compositions, structures, and morphologies of these samples are revealed by X-ray diffraction (XRD), field-emission scanning electron microscopy (FESEM), and atomic force microscope (AFM). In order to investigate the electrical characteristics of these samples, Al/CeO₂/GaN-based metal-oxide-semiconductor (MOS) structures are developed and characterized by using semiconductor parameter analyzer (SPA) and LCR meter.

1.5 Structure of the Thesis

This thesis is divided into five chapters. The background and problem statement, research objective, and the scope of the research are presented in the first chapter. Chapter two discusses on the literature review while the third chapter elucidates on the research methodology. Chapter four presents the result and

discussion on the outcome of this work. Finally, conclusion and suggestion for future research is discussed in the fifth chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 The Significance of GaN as a Substitutional Substrate for Silicon

In general, a semiconductor material that is ideal for high power application should have high breakdown voltage, mechanical stability, low parasitic capacitance and chemical inertness (Dikme et al, 2003; Shur, 1998). Therefore, a device would only be considered as high power when it is able to operate under high temperature with extremely low on-state resistance and withstand an extremely high power (Niiyama et al., 2007; Ikeda et al., 2004). The majority of power devices are dominated by Si for the time being. However, power electronics based on Si technology have extended the design on size, weight, and efficiency to its cutoff point due to heating (Niiyama et al., 2007). The limitation faced by current Si-based power devices is the operating temperature. The maximum temperature that can be sustained by Si-based power devices is 150 °C. Thus, attentions have been placed on using wide band gap semiconductors as the substrate for power electronics devices. Wide band gap semiconductors have the potential of achieving higher operating reliability at higher temperature and device density (Sepulveda, 2008).

Consequently, the usage of wide band gap semiconductors in high power device applications has evolved from the development of optoelectronics (Jain et al., 2000). The presence of high dislocation densities in GaN does not degrade the electrical properties of GaN (Liu and Edgar, 2002). This may imply that this material is suitable for power applications. The ability of GaN power devices to operate at high voltage will eradicate or lower the need for voltage conversion. As an illustration, when a system operates at 28 V, voltage step down from 28 V is

required for a low-voltage technology but voltage step down is not required by GaN power devices as it can operate at 28 V or higher voltage. The outcome of utilizing GaN power devices is that a higher efficiency can be extended by reducing power requirements and the cooling system can be simplified (Ozpineci and Tolbert, 2003). This evidences that GaN has the capability of outperforming silicon in this application.

2.1.1 Comparison between Si and GaN Properties

GaN is considered as a wide band gap semiconductor because its band gap is nearly three times of Si. Besides that, GaN possesses good thermal stability provided additional advantages for power device applications. Unlike Si, the high thermal conductivity of GaN has the capability to dissipate heat generated in the devices. N-type and p-type conductivity of GaN can be achieved due to the significant ionic chemical bonding and non-centrosymmetric structure (Liu and Edgar, 2002). For instance, the ability of GaN-based power devices to operate at 250 °C has suppressed the difficulties faced by Si-based power devices wherein the performance of Si-based power devices will degrade at temperature above 150 °C. With such a high operating temperature, it is accepted as true that the stability of GaN power devices are better than Si power devices (Niiyama et al., 2007). Table 2.1 compares the physical properties of Si and GaN at room temperature.

The excellent properties of GaN, such as high critical electric field and high saturation mobility surpass Si, as shown in Table 2.1 (Neudeck and Chen, 2002). As a result, the stability of power devices composed of GaN is better than Si power devices under high temperature conditions (Niiyama et al., 2007). For a power

semiconductor device operating at high current, higher switching frequency is required. This is because large instantaneous dynamic power dissipation will occur when a power semiconductor device is being switched on and off. By using power devices with higher frequencies, the dynamic power dissipation will be reduced (Neudeck and Chen, 2002). Therefore, GaN, which owns higher switching frequencies, are needed.

Table 2.1: Physical properties of Si and GaN at room temperature (Borges, 2001; Gillessen and Schairer, 1987; Jain et al., 2000; Ozpineci and Tolbert, 2003; Shur and Davis, 2004; Zhou et al., 2008).

Properties	Si	GaN
Band gap, E_g (eV)	1.12	3.45
Dielectric constant, ϵ	11.9	9
Electric breakdown field, E_c (kV/cm)	300	2000
Electron mobility, μ_n ($\text{cm}^2/\text{V-s}$)	1500	1250
Hole mobility, μ_p ($\text{cm}^2/\text{V-s}$)	600	850
Thermal conductivity, λ (W/cm.K)	1.5	1.3
Saturated electron drift velocity, V_{sat} ($\times 10^7$ cm/s)	1	22.2

2.1.2 Common Crystal Structure of GaN

Generally, heteroepitaxy is utilized in growing GaN films on a number of substrates, such as sapphire, SiC, Si, ZnO, germanium, glass, LiGaO₂ and LiAlO₂

(Barcena et al., 2008; Bishop et al., 2007; Caban et al., 2008; Craven et al., 2004; Tamura et al., 2008). However, lattice mismatch remains as the major concern in determining the suitability of the material as a substrate for GaN growth. In addition, the suitability of the material also relies on its crystal structure, composition, surface finish, reactivity, chemical, thermal, and electrical properties. Therefore, device performance depends on the substrate properties as the crystal orientation, polarity, polytype, surface morphology, strain, and the defect concentration of the GaN film are reliant on the employment of substrate material (Liu and Edgar, 2002).

Hence, an appropriate substrate is essential to lower the defect densities and obtain a better quality of GaN epitaxial layer for devices to operate at extreme voltage and current densities conditions. Sapphire is a single crystal aluminum oxide that has been a preferred substrate for most researchers in growing GaN despite of the large lattice (16 %) and thermal mismatch to GaN (Mohammad and Morkoc, 1996; Neudeck and Chen, 2002). This is due to the difficulties in discovering a lattice-matched substrate. Special concentration has been placed on sapphire substrates because of the wide availability of the substrates at large diameters with good quality, hexagonal symmetry, and minimal pre-growth cleaning requirements (Dikme et al., 2003). Other than that, sapphire substrates are able to sustain stability at high temperature (~ 1000 °C). The stability at high temperature is a vital requirement in epitaxial growth by vapor phase techniques (Ambacher, 1998; Mohammad and Morkoc, 1996; Shovlin et al., 2004).

It has been well-known that the type of substrate and its lattice orientation will affect the epitaxially grown crystal structure of GaN. In addition, the deposition

surface does not mean Ga-terminated. Nevertheless, it can be N-terminated if the surface is being covered up by nitrogen atoms. Therefore, N-faced can only be obtained by flipping the crystal. It is believed that the smooth side of bulk single crystal platelets can be grown through Ga-faced (0001) and the rougher surface is obtained via N-faced (000 $\bar{1}$). Experimental results showed that MBE grown GaN in the direction of (000 $\bar{1}$) on c-plane sapphire substrate would result in N-faced while Ga-faced film would be formed by using MOCVD through the deposition of GaN in the direction of (0001) on c-plane sapphire substrate. Figure 2.2 shows the polarities difference between Ga-faced and N-faced wurtzite GaN (Ambacher, 1998).

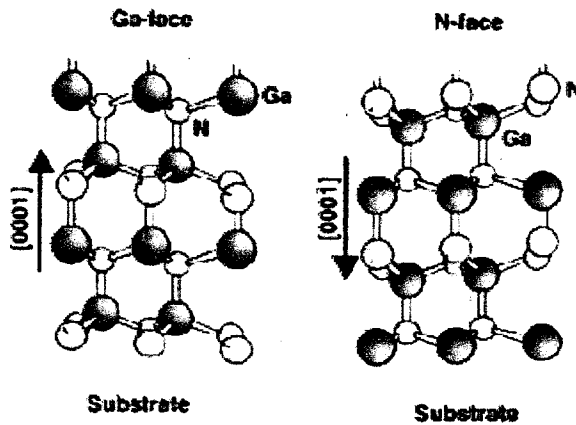


Figure 2.2: Polarities difference between Ga-faced and N-faced wurtzite GaN (Ambacher, 1998).

Recently, much attention has been devoted in growing GaN on (111) Si wafer, owing to the reason that Si wafer can be obtained at lower price and large diameter (Dikme et al., 2003; Shovlin et al., 2004; Sze, 1981). Moreover, the quality of Si wafer is higher than sapphire and SiC, provided that silicon offers good relative thermal conductivity, broad availability, consistency of supply and quality

(Shur and Davis, 2004). In spite of this, the growth of GaN on Si substrate is rather difficult due to the variation in lattice constant (17 %) and thermal-expansion coefficient (Mehandru et al., 2003; Sze, 1981; Tamura et al., 2008; Zhang et al., 2007). This increasing lattice mismatch requires dislocation to release strain. But, the wurtzite III-nitrides are lack of low-energy slip systems compared to zinc-blended semiconductors. As a result, they are unable to nucleate and glide dislocations to relieve the in-plane biaxial tension. Thus, cracking is the most effective way to release the tensile stress (Jain et al., 2000). By applying the advantages that Si offers, the quality of the GaN film can be adapted by using a buffer layer, which is grown on the Si substrate. This can alleviate the lattice mismatch and tensile stress. Same application can be applied onto GaN deposited on sapphire.

2.1.3 Buffer Layer as Stress Relaxation in GaN Thin Film

It has been established that growing GaN thin film on silicon and sapphire substrate will lead to cracking in GaN thin film (Ishikawa et al., 1998; Kim, 2007). In the case of GaN film grown on sapphire substrate, the sample will be subjected to compressive stress due to the thermal expansion coefficient of GaN, which is smaller than sapphire. For GaN film grown on silicon substrate, tensile stress will be induced on the sample due to the difference in the thermal expansion coefficient (Tamura et al., 2008). The introduction of tensile and compressive stresses on the samples will initiate cracks when the grown layer thickness exceeds a critical value (Ishikawa et al., 1998). Since neither of these substrates is lattice matched with GaN, buffer layers of AlN or low-temperature (LT)-GaN have been used to obtain a crack free surface and subsequently a high quality layer of GaN (Lee et al., 2008).

AlN buffer layer has been deposited on both Si and sapphire substrates prior to the growth of GaN in order to grow a high crystalline quality and smooth surface of GaN layer (Amano et al., 1998; Kim, 2007). This is due to the small lattice mismatch (2.3 %) and thermal expansion coefficient mismatch between GaN and AlN buffer layer. It is believed that amorphous AlN has the capability of increasing the breakdown field sustainable in the materials. The use of crystalline AlN will result in a lower breakdown field and a lower forward gate voltage due to dislocations and other defects. Therefore, the electrical behavior of the AlN/GaN structures can be improved by reducing the crystallinity of the material (Jin et al., 2004; Luo et al., 2008). This can be achieved by reducing the growth temperature. Besides AlN buffer layer, LT-GaN buffer layer has been also used for GaN grown on sapphire and Si substrates. The crystal quality of GaN layer grown on sapphire substrate is enhanced when LT-GaN buffer layer is being utilized (Lee et al., 2008). However, meltback etching of Si occurred when LT-GaN buffer layer is deposited on Si substrate, (Kim, 2007). This will cause the quality of thin films to decline. Another vital role in reducing crack density is by varying the thickness of buffer layer. It has been stated by other researchers that, by increasing the thickness, a smoother surface can be produced and the crack density can be reduced (Kim, 2007; Luo et al., 2008).

2.2 Development of Metal-Oxide-Semiconductor (MOS) Based Power Device

GaN is an excellent candidate to use in power components based on a number of device configurations, such as metal-semiconductor field effect transistors (MESFET), heterojunction field effect transistors (HFET), thyristors and

heterojunction bipolar transistor (HBTs) previously. Later research has been devoted on GaN for the use in metal oxide semiconductor field effect transistor (MOSFET) configuration. Despite the fact that GaN-based power devices outperform Si-based power devices, the performance and reliability of GaN-based power devices face limitation due to relatively high leakage current (Ye et al., 2005; Zhou et al., 2008). As the leakage current increases, the noise figure escalates and the trimming down of breakdown voltage will ensue (Ye et al., 2005). Other than that, GaN built from MESFET structure has several drawbacks that need to be rectified, such as low power added efficiencies and nonlinearity. These drawbacks take place because of high parasitic resistance. High contact resistivities and high sheet resistances between the source contact and the gate are the root of high parasitic resistance (Ren and Zolper, 2003).

As a result, this drawback can be overcome by introducing metal-oxide-semiconductor (MOS)-based power device (Figure 2.3) (Zhou et al., 2008). The ability of MOSFET structure to remain insensitive to temperature during operation provides an advantage over the heterojunction type transistor. Another advantage supplied by MOSFET is that the structure can be fabricated by n-type or p-type material under the gate. Therefore, by adapting to MOSFET structure, complementary device structures, known as CMOS can be fabricated. MOS-based power device is made of an insulating layer, which covers the semiconductor substrate (Abdullah et al., 2005). This insulating layer plays many important functions, such as passivation of semiconductor surface, electrical insulation of selected structures of semiconductor devices, isolation to other devices like metal contact, higher current gain cutoff frequency due to a smaller input capacitance

(Irokawa et al., 2004) and protecting the device from environmental hazards (Kikuta et al., 2006). The gate oxide serves as an insulating layer for the gate to sustain a high transverse electric field. Thus, the channel conductance can be modulated (Cheong et al., 2008).

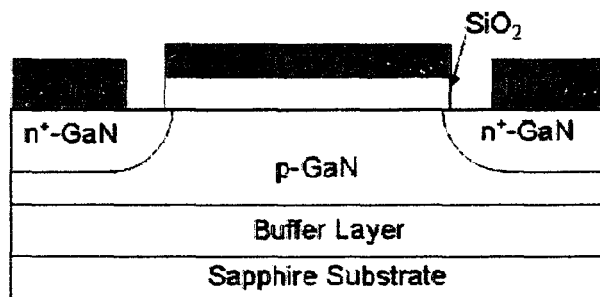


Figure 2.3: Schematic cross-sectional of GaN MOSFET (Takehiko et al., 2008).

2.2.1 MOS Capacitor

Metal-oxide-semiconductor (MOS) structure comprises of gate oxide, metal electrode, and semiconductor is one of the most widely used systems in electronic devices, especially in integrated circuits. In order to investigate the electrical properties of the MOS-based devices, MOS capacitor needs to be fabricated. MOS capacitor is the heart of all MOS-based devices and it is a two terminal device consists of a gate oxide sandwiched between a semiconducting substrate and a metal electrode. Besides aluminum, other type of metals may also be used as the metal electrode. In order to provide an electrical contact to the semiconducting substrate, a layer of metal electrode is deposited at back of the substrate. The basic structure of MOS capacitor is shown in Figure 2.4.

When the MOS capacitor is under zero bias conditions, there are no charges present in the oxide or at the oxide-semiconductor interface. However, the

application of bias to the MOS capacitor will cause the emergence of charges at the interfaces of metal-oxide and oxide-semiconductor as well as the oxide. The appearance of charges in the metal-oxide interface, oxide, and oxide-semiconductor interface is detrimental to the MOS-based devices because the performance and stability of these devices will be affected by these charges (Pierret, 1990; Schroder, 1998).

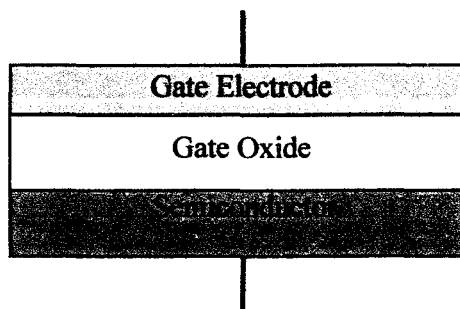


Figure 2.4: The basic structure of MOS capacitor.

2.2.1.1 Influence of Applied Bias on MOS-Capacitor

When positive bias ($V_G > 0$) is applied to n-type semiconductor substrate, accumulation condition is obtained as the Fermi energy (E_F) in the metal is lower than E_F in the semiconductor as shown in Figure 2.5. Thus, a positive sloping of the energy bands in both the insulator and semiconductor occurred. Under this condition, greater amount of electron, which is the majority carrier concentration for n-type semiconductor exist near the oxide-semiconductor interface than in the semiconductor. When observed from a charge point of view, positive charges are placed on the gate due to the application of $V_G > 0$. In order to maintain a balance of charge, electron must be attracted toward the semiconductor-oxide interface (Pierret, 1990; Schroder, 1998).

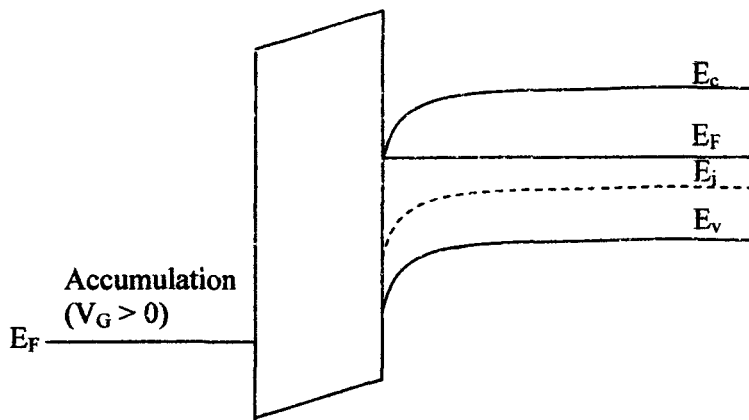


Figure 2.5: Energy band diagram for an ideal n-type MOS-capacitor under accumulation condition (Pierret, 1990).

When small negative bias ($V_G < 0$) is applied, small negative sloping of the energy bands in both the oxide and semiconductor take place due to the slightly higher E_F in the metal than the E_F in the semiconductor. This is known as depletion as the electrons concentration in the oxide-semiconductor interface has been decreased to less than the doping concentration (N_A or N_D) of the semiconductor. The energy band diagram under depletion condition can be observed in Figure 2.6 (Pierret, 1990; Schroder, 1998).

Further increase the negative bias ($V_G < V_T$) applied to the MOS capacitor gate, more bending up of the bands at the semiconductor surface will take place and the concentration of the minority carrier holes at the surface will be more than concentration of majority carrier electrons. Thus, the surface region will change from n-type to p-type. It is termed as inversion due to the change in character of the surface region as displayed in Figure 2.7 (Pierret, 1990; Schroder, 1998).

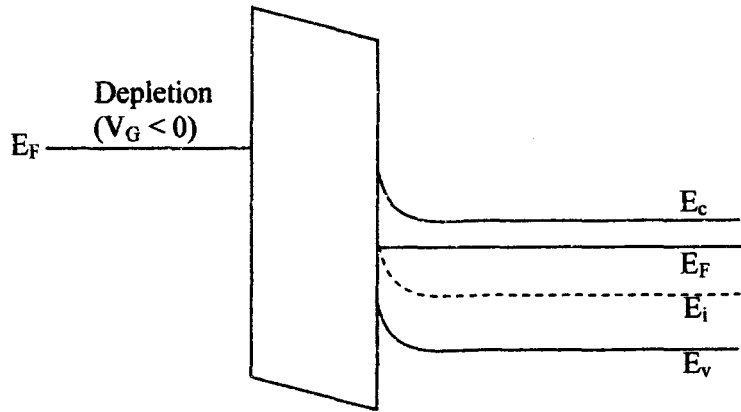


Figure 2.6: Energy band diagram for an ideal n-type MOS-capacitor under depletion condition (Pierret, 1990).

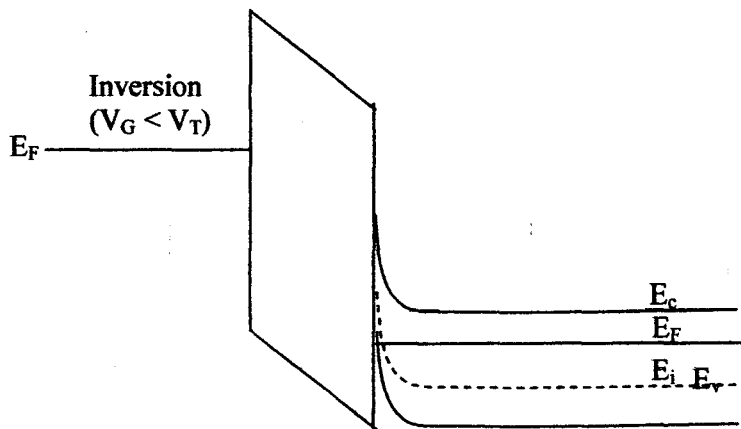


Figure 2.7: Energy band diagram for an ideal n-type MOS-capacitor under inversion condition (Pierret, 1990).

2.2.1.2 Capacitance-Voltage (C-V) Characteristics of MOS-Capacitor

In order to understand the internal nature of the MOS-capacitor, it is of importance to perform the capacitance-voltage (C-V) measurement to obtain the C-V characteristic of the MOS capacitor. The measured capacitance of a MOS capacitor varies as a function of the applied voltage. When the device is driven from accumulation (point A) into depletion (point B) as shown in Figure 2.8, the

inversion-layer charge is negligible compared with the bulk charge. When the voltage is increased further than point B, inversion layer is formed if the voltage is swept slowly enough to allow generation of the minority carriers (Pierret, 1990; Schroder, 1998).

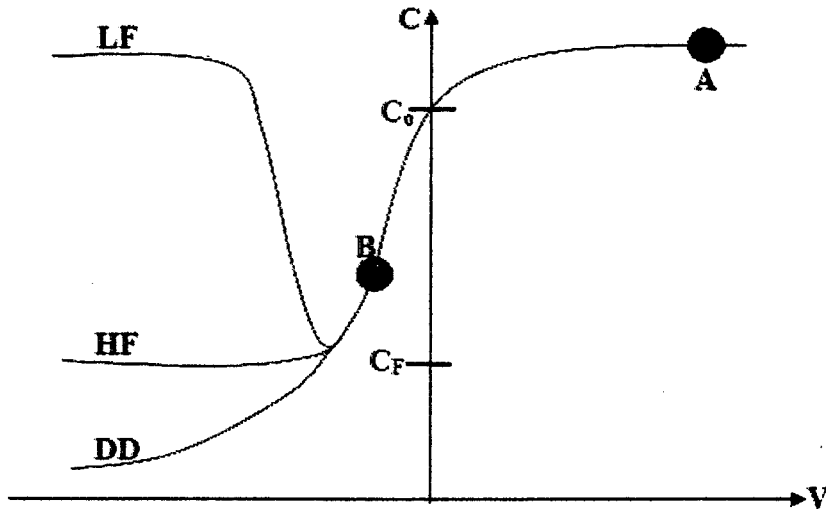


Figure 2.8: Low-frequency (LF), high-frequency (HF), and deep-depletion (DD) capacitance-voltage curves for n-type MOS capacitor (Pierret, 1990).

Low-frequency (LF) curve is obtained if the ac probing voltage used in the capacitance measurement is sufficiently low frequency that the inversion charge is able to follow the ac probing voltage and the dc sweeping voltage. High-frequency (HF) curve is obtained when sufficiently low dc sweep voltage and high ac voltage frequency are used. Deep depletion (DD) curve is measured when the inversion charge does not have sufficient time to be thermally generated due to high sweep voltage rate, irrespective of the ac probing voltage frequency (Pierret, 1990; Schroder, 1998).

2.2.1.3 Breakdown of Gate Oxide in MOS-Capacitor

When electric field is applied to a MOS-capacitor, gate oxide needs to undergo several degradation mechanisms. One of the degradation mechanisms involves gate oxide breakdown, which is a multistage event. It is also termed as trap generation process that leads to soft-breakdown or hard-breakdown. During the breakdown event, the stored energy in the capacitor is partially discharged through the breakdown region. The occurrence of soft- or hard-breakdown relies on the oxide thickness, oxide area, magnitude of the stored energy, and the extent of the local damage (Dumin, 2002). Thinner gate oxide has a higher probability of experiencing multiple soft-breakdowns prior to hard-breakdown. During the soft-breakdown of the gate oxide, the damaged region due to the discharge of the stored energy in the MOS-capacitor will turn into an open circuit. As for thicker gate oxide, it has the ability to store larger energy. Thus, the first breakdown of a thicker gate oxide is usually a destructive breakdown due to the larger damaged region (Dumin, 2002). This is known as hard-breakdown (Dumin, 2002).

Figure 2.9 shows the degradation processes that occur inside the gate oxide leading to the hard breakdown. Initially, the as-deposited gate oxide consists of only a few traps. When electric field is applied to the MOS-capacitor, traps, which act as scattering centers and pathway for current to leak through the oxide, are generated. The increment of electric field will generate higher density of traps in the gate oxide. Ultimately, the traps will act as a conducting path between the cathode and anode, whereby soft-breakdown takes place. After the soft-breakdown, the breakdown region will become open-circuited. This allows the MOS-capacitor to recharge through the circuit power supply and generate more traps inside the gate oxide. The