UNIVERSITI SAINS MALAYSIA

Laporan Akhir Projek Penyelidikan Jangka Pendek

Design of Low Power Low Noise Amplifier for RF Application

By

Dr. Norlaili Mohd. Noh

Assoc. Prof. Dr. Tun Zainal Azni Zulkifli

2012

UNIVERSITI SAINS MALAYSIA

LAPORAN AKHIR PROJEK PENYELIDIKAN JANGKA *PENDEK*

FINAL REPORT OF SHORT TERM RESEARCH PROJECT

Sila kemukakan laporan akhir ini melalui Jawatankuasa Penyelidikan di Pusat Pengajian dan Dekan/Pengarah/Ketua Jabatan kepada Pejabat Pelantar Penyelidikan

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1. **Nama Ketua Penyelidik:**
Name of Research Leader
Norlaili Mohd. Noh

☐ Profesor Madya/ *Assoc. Prof.* ☑ Dr./ *Dr.* ☐ Encik/Puan/Cik *Mr/Mrs/Ms*

2. **Pusat Tanggungjawab (PTJ):**
School/Department

School of Electrical and Electronic Engineering

3. **Nama Penyelidik Bersama:**
Name of Co-Researcher

Assoc Prof. Dr. Tun Zainal Azni Zulkifli

4. **Tajuk Projek:**
Title of Project

Design of Low Power Low Noise Amplifier for RF Application

5. **Ringkasan Penilaian/***Summary of Assessment*:	Tidak Mencukupi *Inadequate* 1	2	Boleh Diterima *Acceptable* 3	Sangat Baik *Very Good* 4	5
i) **Pencapaian objektif projek:** *Achievement of project objectives*	☐	☐	☐	☑	☐
ii) **Kualiti output:** *Quality of outputs*	☐	☐	☐	☑	☐
iii) **Kualiti impak:** *Quality of impacts*	☐	☐	☑	☐	☐
iv) **Pemindahan teknologi/potensi pengkomersialan:** *Technology transfer/commercialization potential*	☐	☐	☑	☐	☐
v) **Kualiti dan usahasama :** *Quality and intensity of collaboration*	☐	☐	☐	☑	☐
vi) **Penilaian kepentingan secara keseluruhan:** *Overall assessment of benefits*	☐	☐	☐	☑	☐

6. Abstrak Penyelidikan

(Perlu disediakan di antara 100 - 200 perkataan di dalam **Bahasa Malaysia dan juga Bahasa Inggeris**. Abstrak ini akan dimuatkan dalam Laporan Tahunan Bahagian Penyelidikan & Inovasi sebagai satu cara untuk menyampaikan dapatan projek tuan/puan kepada pihak Universiti & masyarakat luar).

Abstract of Research
(An abstract of between 100 and 200 words must be prepared in Bahasa Malaysia and in English). This abstract will be included in the Annual Report of the Research and Innovation Section at a later date as a means of presenting the project findings of the researcher/s to the University and the community at large)

Memandangkan penguat hingar rendah adalah blok pertama dalam sistem penerima, penguat hingar rendah dianggap sebagai salah satu daripada peringkat yang paling penting yang hendak direkabentuk. Cabaran besar dalam mencapai matlamat penguat hingar rendah adalah untuk mengimbangi antara beberapa parameter reka bentuk seperti gandaan kuasa S21, parameter pantulan masukan S11, parameter pengasingan balikan S12, parameter pantulan keluaran S22, angka hingar dan kelinearan. Dalam projek ini, reka bentuk penguat hingar rendah kuasa rendah seperti topologi pemadanan masukan dan hingar serentak terkekang kuasa mudah, penggunaan semula arus, kaskod terlipat, berbilang piawai dan pemadanan masukan dan hingar serentak terkekang kuasa berpenimbal salir sepunya dikaji, dianalisis dan direkabentuk. Penguat hingar rendah kuasa rendah dengan topologi pemadanan masukan dan hingar serentak terkekang kuasa mudah dan pemadanan masukan dan hingar serentak terkekang kuasa berpenimbal salir sepunya telah dihantar untuk fabrikasi. Perbandingan telah dibuat dan keunggulan satu terhadap yang lain ditentukan.

Since the low noise amplifier is the first block in a receiver system, the low noise amplifier is considered as one of the most important stage to be designed. The great challenge in achieving the low noise amplifier goals is to balance the trade-off between design parameters such as the power gain S21, input reflection coefficient S11, reverse isolation S12, output reflection coefficient S22, noise figure and linearity. In this project, low power LNA designs such as the Simple Power Constrained Simultaneous Noise and Input Matching, current reuse, folded cascode, multistandard and Power Constrained Simultaneous Noise and Input Matching with Common Drain buffer topologies were studied, analyzed and designed. The Simple Power Constrained Simultaneous Noise and Input Matching and the Power Constrained Simultaneous Noise and Input Matching with Common Drain Buffer were sent for fabrication. Comparisons were made and the superiority of one over the others were determined.

7. Sila sediakan laporan teknikal lengkap yang menerangkan keseluruhan projek ini.

[Sila gunakan kertas berasingan]
Applicant are required to prepare a Comprehensive Technical Report explaining the project.
(This report must be appended separately)

Please refer to Appendix A.

Senaraikan kata kunci yang mencerminkan penyelidikan anda:
List the key words that reflects your research:

Bahasa Malaysia	*Bahasa Inggeris*
a. Kuasa rendah	a. Low power
b. Penguat hingar rendah	b. Low noise amplifier
c. Penguat hingar rendah pemadanan masukan dan hingar serentak terkekang kuasa	c. Power constrained simultaneous noise and input matching low noise amplifier
d. Penguat hingar rendah kaskod terlipat	d. Folded cascode low noise amplifier
e. Penguat hingar rendah penggunaan semula arus	e. Current reuse low noise amplifier
f. Penguat hingar rendah berbilang piawai	f. Multistandard low noise amplifier
g. Penguat hingar rendah pemadanan masukan dan hingar serentak terkekang kuasa berpenimbal salir sepunya	g. Power constrained simultaneous noise and input matching with common drain buffer low noise amplifier

8. Output dan Faedah Projek
Output and Benefits of Project

(a) * **Penerbitan Jurnal**
Publication of Journals
(Sila nyatakan jenis, tajuk, pengarang/editor, tahun terbitan dan di mana telah diterbit/diserahkan)
(State type, title, author/editor, publication year and where it has been published/submitted)

1. *Mohd. Noh, N.*, Hashim A., Tan K. Y. and Tan Y. Y. "Design and Analysis of the Current Reuse Technique and Folded Cascode Power Constrained Simultaneous Noise and Input Matching LNAs with distributed and lumped parasitic," Asia Pacific Conference on Circuits and Systems (APCCAS 2010), 6 – 9 December 2010, Kuala Lumpur, Malaysia.
2. Tan Thiam Loong, Awatif Hashim, *Norlaili Mohd Noh*, Mohd Tafir Mustaffa. "1.575 GHz to 2.48 GHz Multi-standard Low Noise Amplifier Using 0.18 μm CMOS with On-Chip Matching," 2011 IEEE Symposium on Industrial Electronics & Applications (ISIEA2011), Langkawi, Malaysia, 25 – 28 September 2011.
3. *Mohd. Noh, N.*, Hashim, A. (2011). "Design and Analysis of Monolithic Inductively-degenerated Cascode Based Low Noise Amplifiers," IETE Journal of Education, 52 (2), pp. 71-82.

The published papers can be referred to Appendix B, C and D.

(b) **Faedah-faedah lain seperti perkembangan produk, pengkomersialan produk/pendaftaran paten atau impak kepada dasar dan masyarakat.**
State other benefits such as product development, product commercialisation/patent registration or impact on source and society.

The product development for this project is the chip fabricated at Silterra (M) Sdn Bhd. The measurement results are expected to be similar to the post layout simulation results. These chips are useful for research purpose for further studies.

* Sila berikan salinan/*Kindly provide copies*

(c) **Latihan Sumber Manusia**
Training in Human Resources

i) Pelajar Sarjana:
Graduates Students
(Perincikan nama, ijazah dan status)
(Provide names, degrees and status)

Awatif Binti Hashim, Bachelor Degree of Electronic Engineering, pursuing MSc in Analog and Digital IC Design in the School of Electrical & Electronic Engineering, USM. Expected to graduate in 2013.

ii) Lain-lain:
Others

---

9. Peralatan yang Telah Dibeli:
Equipment that has been purchased

3 April 2012

Tandatangan Penyelidik
Signature of Researcher

Tarikh
Date

Komen Jawatankuasa Penyelidikan Pusat Pengajian/Pusat
Comments by the Research Committees of Schools/Centres

2 conferences and 1 journal publication have been produced. 1 MSc by research student is expected to graduate.

Prof. Madya Dr. Kamal Zuhairi Zamli
Timbalan Dekan
(Pengajian Siswazah & Penyelidikan)
Pusat Pengajian Kejuruteraan Elektrik & Elektronik
Kampus Kejuruteraan
Universiti Sains Malaysia

TANDATANGAN PENGERUSI
JAWATANKUASA PENYELIDIKAN
PUSAT PENGAJIAN/PUSAT
Signature of Chairman
[Research Committee of School/Centre]

9/4/12.

Tarikh
Date

UNIVERSITI SAINS MALAYSIA
UNIT KUMPULAN WANG PENYELIDIKAN/RU
JABATAN BENDAHARI KAMPUS KEJURUTERAAN
PENYATA KUMPULAN WANG
TEMPOH BERAKHIR 3/2012

4/2/2012

Status Projek : AKTIF

Tajuk Projek : DESIGN OF LOW POWER LOW NOISE AMPLIFIER FOR RF APPLICATION

No Projek (Agensi) :

Pusat Pengajian : Pusat Pengajian Kejuruteraan Elektrik dan Elektronik

Tempoh Projek : 2009 / 11 - 2012 / 3

No Akaun : 304 / 6039048

Penyelidik : NORLAILI MOHD NOH

Vot	Keterangan	Peruntukan Asal	Perbelanjaan Tahun Lalu	Peruntukan Semasa	Tanggungan	Belanja	Jumlah Belanja	Baki	%
11000	Gaji	29,516.00	$23,326.70	$0.00	$0.00	$67.85	$67.85	$6,121.45	0.00
15000	Lain-lain Emolumen	0.00	$500.00	$0.00	$0.00	$500.00	$500.00	($1,000.00)	0.00
		$29,516.00	**$23,826.70**	**0.00**	**$0.00**	**$567.85**	**$567.85**	**$5,121.45**	0.00
21000	PERJALANAN DAN SARA HIDUP	1,400.00	$2,511.14	$0.00	$0.00	$0.00	$0.00	($1,111.14)	0.00
23000	PERHUBUNGAN DAN UTILITI	400.00	$75.00	$0.00	$0.00	$0.00	$0.00	$325.00	0.00
27000	BEKALAN DAN ALAT PAKAI HABIS	500.00	$5,941.40	$0.00	$0.00	$394.80	$394.80	($5,836.20)	0.00
29000	PERKHIDMATAN IKTISAS DAN HOSPITALITI	4,000.00	$5,976.78	$0.00	$0.00	$186.20	$186.20	($2,162.98)	0.00
		$6,300.00	**$14,504.32**	**0.00**	**$0.00**	**$581.00**	**$581.00**	**($8,785.32)**	0.00
35000	HARTA-HARTA MODAL LAIN	2,664.00	$0.00	$0.00	$0.00	$0.00	$0.00	$2,664.00	0.00
		$2,664.00	**$0.00**	**0.00**	**$0.00**	**$0.00**	**$0.00**	**$2,664.00**	0.00
77000	SUMBANGAN	0.00	($1,000.00)	$0.00	$0.00	$0.00	$0.00	$1,000.00	0.00
		$0.00	**($1,000.00)**	**0.00**	**$0.00**	**$0.00**	**$0.00**	**$1,000.00**	0.00
		$38,480.00	**$37,331.02**	**$0.00**	**$0.00**	**$1,148.85**	**$1,148.85**	**$0.13**	0.00

APPENDIX A

A. Project Portfolio

Project Title	Design of Low Power Low Noise Amplifier for RF Application
Project Objective	1. To study and analyze low power low noise amplifier (LNA) for RF application 2. To design and characterize LNAs for RF and low power application 3. To design and characterize a low power $0.18\mu m$ CMOS LNA for ultra-wide-band (UWB) application.
Date of Commencement	1/12/2009
Date of Completion	30/11/2011
Amount of approved Grant	RM 38,480.00
Amount for first distribution	RM 22,430.00
Amount for second distribution	RM 16,050.00
Balance of Grant (latest statement of accounts by March 2012)	RM 0.13

B. Gantt Chart

	M 1-2	M 3-4	M 5-6	M 7-8	M 9-10	M 11-12	M 13-14	M 15-16	M 17-18	M 19-20	M 21-22	M 23-24	M 25-28
Study and analyze the low power LNA topologies	■	■											
Design and simulation			■	■									
Design optimization					■	■							
Fabricate the design						■	■						■
Characterization the developed chip							░	░					
Analyze the measurement results									░	░			
Evaluate the overall performance of the chip											░	░	
Report					*	*				*			*

■ Achieved

░ Expected outcome

C. Report summary

Based on the objectives and Gantt chart stated and shown in the project proposal, the project has progressed well within 1 year from the date of commencement. Effective from 1st January 2011, Silterra had started to impose fabrication fees. The designs that we had sent to Silterra in September 2010 were not fabricated as Silterra had stopped all MPW (Multi-project wafer) fabrication until the finalized fabrication fees were determined. Since 1st January 2011, the fabrication fee is RM7000/design for 0.18-μm CMOS technology and RM11000/design for 0.13-μm CMOS technology.

In February 2012, Silterra (M) Sdn Bhd had kindly offered to fabricate the LNAs in this project for free. However, the process that was being offered is for the 0.13-μm CMOS. Modifications to the design were made to meet the design specification for this new process. The 0.13-μm CMOS is a newer process, having more options in setting value of components and suitable for low power design as the voltage suppy is only 1.2 V (versus 1.8 V required in the 0.18-μm process) . Hence, other low power topologies have been studied and analysed to achieve those requirements. Simple PCSNIM cascode LNA and PCSNIM LNA with Common Drain (CD) buffer design have been chosen to achieve the requirements set by Silterra (M) Sdn Bhd.

I. Simple Power Constrained Simultaneous Noise and Input Matching (PCSNIM) cascode LNA

PCSNIM technique enables simultaneous noise and input matching for low-power implementations (Andreani & Sjoland, 2001; Nguyen & Lee, 2003). PCSNIM is especially suitable for low-power implementation in mobile radio transceivers. In this technique, even if the transistor is small in size and resulting in small C_{gs}, noise and input matching can still be achieved by manipulating the value of C_{ex}. For Simple PCSNIM LNA, the cascode is having the luxury of consuming all the current. With higher current consumed, the noise figure (NF) becomes better. Hence, this topology is able to provide the best NF. If NF is not a specification to be fulfilled, smaller current can be consumed with smaller size transistors.

The schematic can be seen in the Figure 1. Width of M_1 is same as width of M_2. A feedback technique is adopted by using a degeneration inductor, L_s. This type of input matching is suitable for narrow-band applications and also for large transistor, thus high power dissipation, and high frequency of operation.

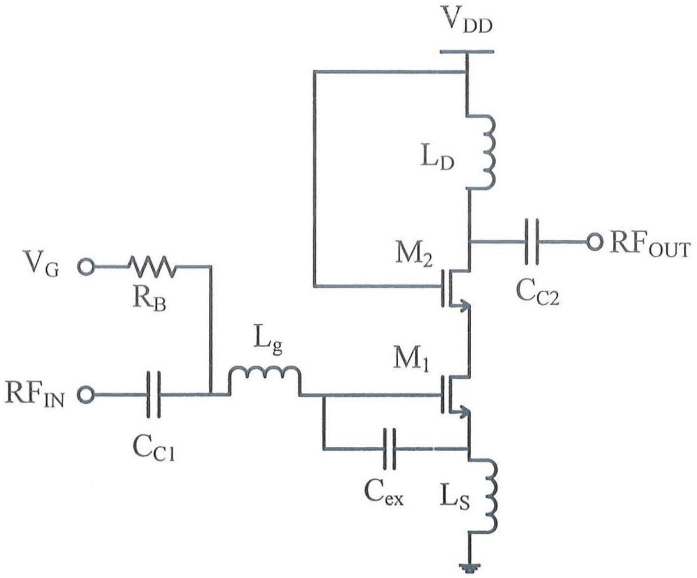


Figure 1: Simple PCSNIM cascode LNA schematic

II. PCSNIM LNA with CD buffer

This technique is used to achieve an output matching at the output stage. The matching circuitry is replaced with an output buffer. Instead of using L-C network that requires large space due to the inductors being huge passives, there are two capacitors and transistors with a resistor to perform the task. Figure 2 shows the PCSNIM with output buffer LNA.

A common-drain transistor is used as the buffer, shown as M_3. M_4 is operating as current-source. L_d is to resonate with C_d,C_{gs_M3},C_0,C_{gd_M4} and the bondpad capacitance to operate at 2.45 GHz. C_{C2} is the coupling capacitor, to isolate the biasing of the buffer from the cascode. To do that, the large capacitor (in pF) is needed. R_D is to isolate the signal path from the current mirror. The transistor M_2 width is half of the M_1's width. In terms of linearity performance, M_2 has more influenced as compared to M_1. Therefore, if the linearity of the LNA needs to be enhanced, the M_2 should be the one to be modified (Mohd. Noh, 2009). A PCSNIM cascode LNA with CD buffer is designed to maintain the matched conventional PCSNIM NF with much less layout space consumed. The power gains of the LC-matched PCSNIM and PCSNIM with CD buffer are comparable but both PCSNIM lost in term of linearity. However, this method will be better for circuit integration as it requires less space.

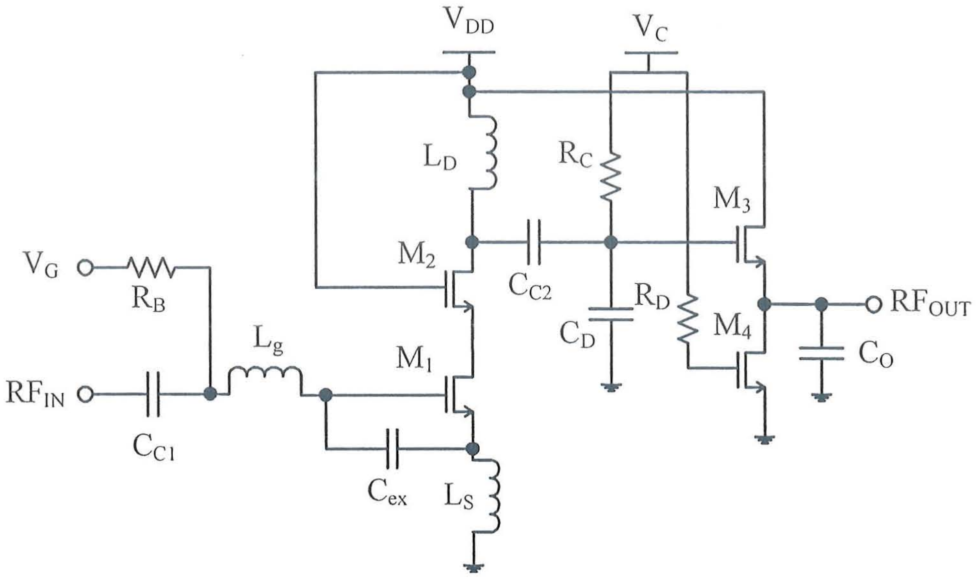


Figure 2: PCSNIM LNA with CD buffer schematic

Two designs had been sent for fabrication to Silterra (M) Sdn Bhd on 22nd February 2012. Hence, RM22000 has been saved due to free fabrication. That indicates that the expected outcomes for the first twelve months had been achieved. Fabricated chips will be obtained in May. Hence, the characterization will be performed in May.

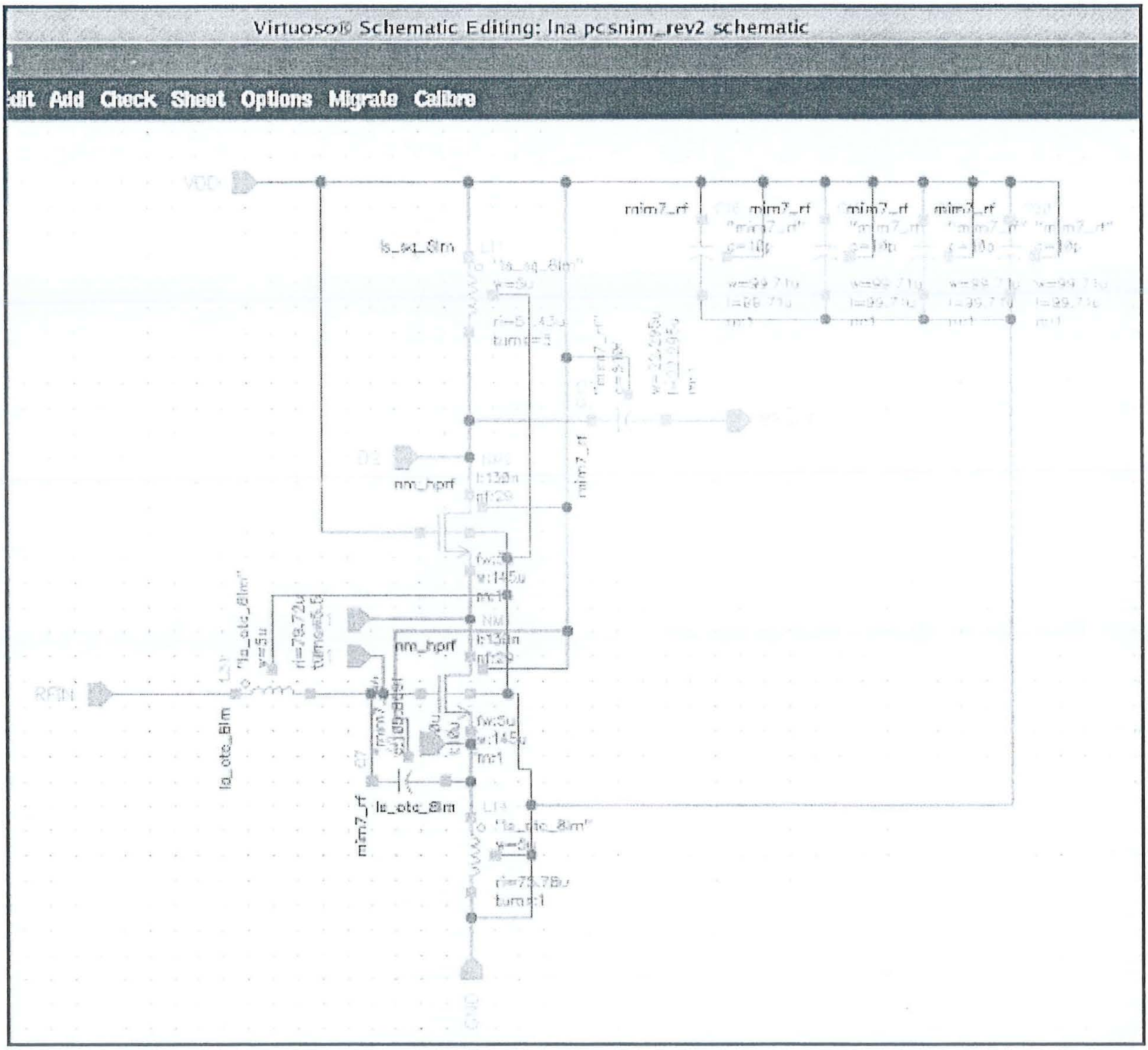


Figure 3: Simple PCSNIM cascode LNA

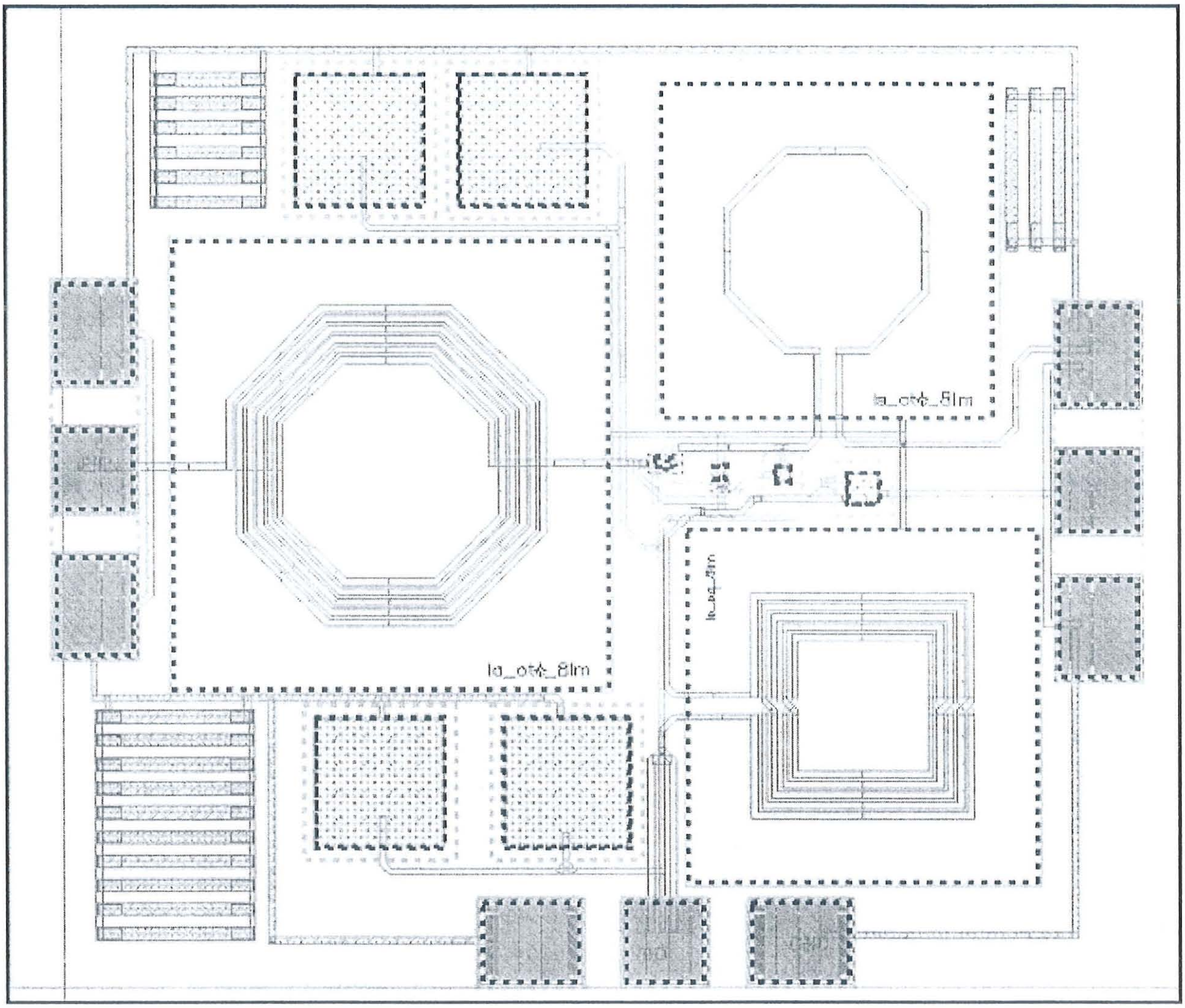


Figure 4: Layout design for the simple PCSNIM cascode LNA

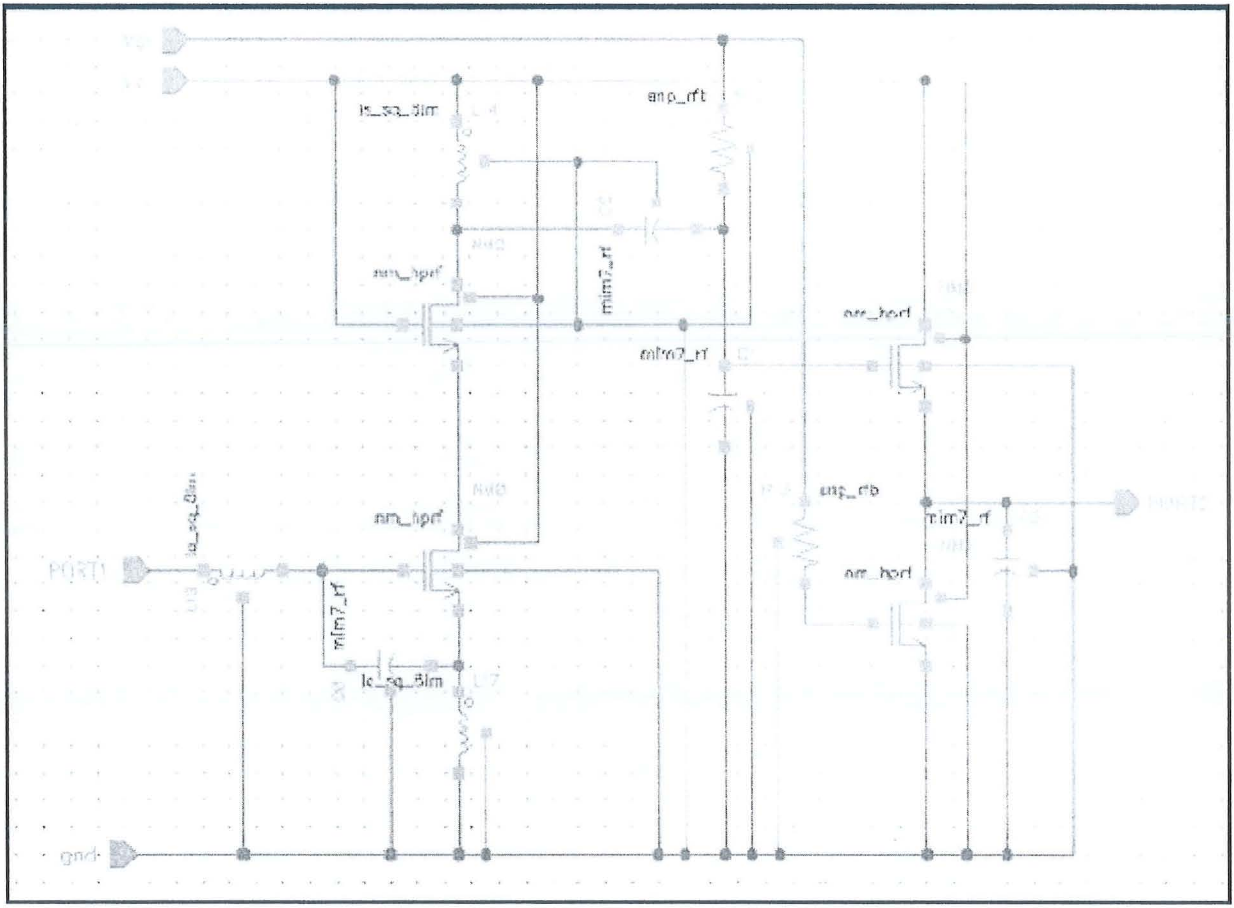


Figure 5: Schematic for the PCSNIM cascode LNA with Common Drain (CD) buffer.

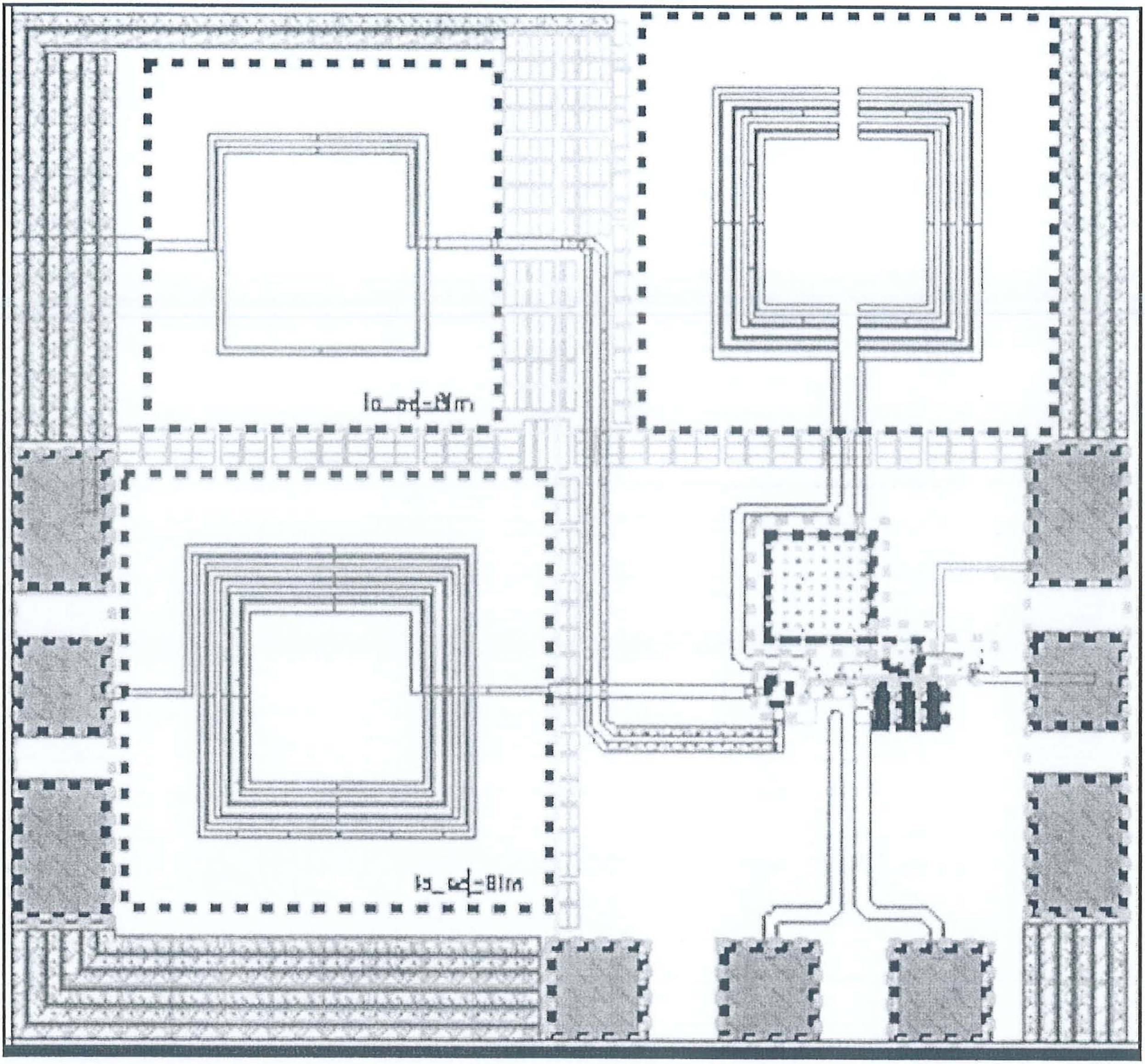


Figure 6: Layout for the PCSNIM cascode LNA with CD buffer.

(a) Results

The designs have to fulfill the required specification. The following Table 1 shows the RF performance metrics for the mentioned LNA.

Table 1. RF parameters and pre-layout results

Parameter	Desired Specs	Simple PCSNIM cascode LNA	PCSNIM cascode LNA with CD buffer
Frequency (GHz)	2.4-2.5	2.45	2.45
Bandwidth (MHz)	100	672	440
Noise Figure (dB)	2	1.684	3.08
IIP3 (dBm)	-10	-10	-
P1dB (dBm)	-20	-	-
S_{21} (dB)	> 22	20.98	16.30
S_{11} (dB)	< -10	-14.69	-21.90
S_{22} (dB)	< -10	-13.95	-15.10
S_{12} (dB)	< -20	-35.77	-54.50
V_{dd} (V)	1.2	1.2	1.2
Current consumption I_d (mA)	4	3.80	3.9

Once obtained, the measurement results will be compared to the post-layout simulation results.

2 journal publications were promised to be published in the project proposal. Upon the completion of this project, 2 papers have been published in conference proceedings and 1 in an international journal. The two papers were published in the Asia Pacific Conference on Circuit and Systems (APCCAS) 2010 conference proceeding and the 2010 IEEE Symposium on Industrial Electronics & Applications (ISIEA2011) conference while one journal paper was published in the Institution of Electronics and Telecommunication Engineers (IETE) Journal of Education. These published papers can be referred to Appendix B, C and D.

D. References

Andreani, P. and Sjoland, H. (2001). Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier. *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing.* 48(9): 835 – 841.

Nguyen, T.-K. and Lee, S.-G. (2003). Noise and Gain Optimization Technique for RF-Integrated CMOS Low Noise Amplifier. Proceedings of the 2003 IEEE Conference on Electron Devices and Solid-State Circuits. Hong Kong, December 16-18. 221 – 224

N.M. Noh, "Development of inductively-degenerated LNA for WCDMA application utilizing 0.18um RFCMOS technology," PhD thesis. Universiti Sains Malaysia,Penang, Malaysia, 2009.

APPENDIX B

Design and Analysis of Monolithic Inductively-Degenerated Cascode Based Low Noise Amplifiers

Norlaili Mohd. Noh
School of Electrical and Electronic Engineering, USM.

Awatif Hashim
Pursuing Postgraduate study in Universiti Sains Malaysia (USM)

Abstract

This paper is on the design and analysis of the five types of inductively-degenerated cascode LNA topologies. The topologies are Simultaneous Noise and Input Matching (SNIM), Power-constrained Simultaneous Noise and Input Matching (PCSNIM), Current-reuse (CR), Folded-cascode (FC) and PCSNIM with output buffer. For each topology, the functionality and design are discussed. Equations are given to enable better understanding on how the circuits perform. The characteristics that distinguish one topology from the others are highlighted. These LNAs were simulated using Silterra's 0.18 μm CMOS technology and the designs were based on a common current consumption of 4 mA to enable comparative analysis. The results obtained conformed to the theories presented. The performances of the LNAs are within the desired range and in accordance to the W-CDMA requirement.

Keywords : Inductively-degenerated cascode LNA, simultaneous noise and input matching, power-constrained simultaneous noise and input matching, current-reuse, folded-cascode, power-constrained simultaneous noise and input matching with output buffer.

1. INTRODUCTION

Amongst the design goals of an LNA are to achieve good noise figure (NF), gain, power consumption and linearity performances in accordance to the targeted application. Hence, the choice of LNA topology for a specific application is crucial in determining the achievement of the expected performance. Five LNA topologies based on the inductively-degenerated cascode structure were studied and analyzed for the W-CDMA application. The SNIM has high input resistance and transconductance, similar to that of a common-source (CS), and a good frequency response such that can be provided by a common gate (CG) [1, 2]. The PCSNIM enables simultaneous noise and input matching even for small devices and low power operations [3-5]. In the CR, the input transistor of a cascode is replaced with an inverter-like combination of PMOS and NMOS to reduce power consumption but is still able to maintain the transconductance and consequently the gain [6]. The FC LNA was not only designed for low voltage operation but also for good noise performance [7]. For monolithic design, PCSNIM with output buffer LNA provides good gain and noise performance without the need of external matching circuitries [8].

This paper discusses on the design of all the mentioned topologies with detailed description on the functionality of each one of them. The descriptions are supported by relevant equations for better understanding. Designs for each topology were based on a common current consumption of 4 mA, which is an estimated value for a single-ended 0.18 μm LNA for W-CDMA application. A common current was set to enable comparative analysis amongst the topologies.

1.1 Design of the Inductively Degenerated Based LNAs

The list of symbols used in this paper is as shown in Table 1.

SNIM LNA

The SNIM LNA circuit is shown in Figure 1. Flow chart of the design methodology of the topology is given in Figure 2.

(i) Calculation of transistor size based on the Power Constrained Noise Optimization (PCNO) Technique

The transconductance of the transistor, M_1 is

$$g_m = \alpha\mu_n C_{ox} \frac{W}{L} V_{ov} \qquad (1)$$

Foundry specified electron mobility, μ_n, is given as 0.039 m²/Vs. $\alpha \approx 1$ and $C_{ox} = 9.4 \times 10^{-3}$ F/m². V_{ov} is the overdrive voltage of the transistor. From the PCNO method, the quality factor of the input stage is [8].

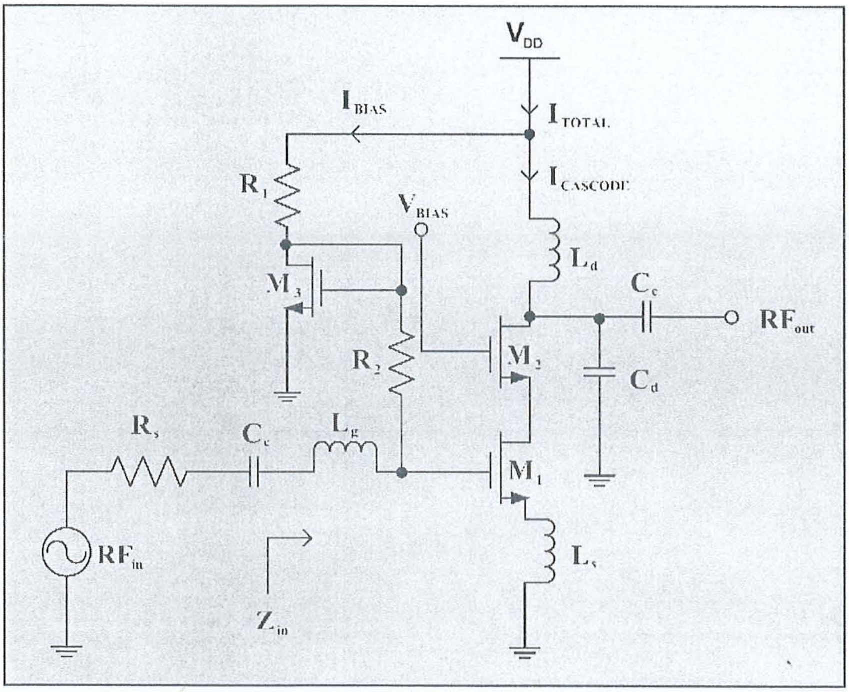


Figure 1 : Inductively-degenerated cascode LNA [10] with input inductance, Lg. This is the SNIM topology

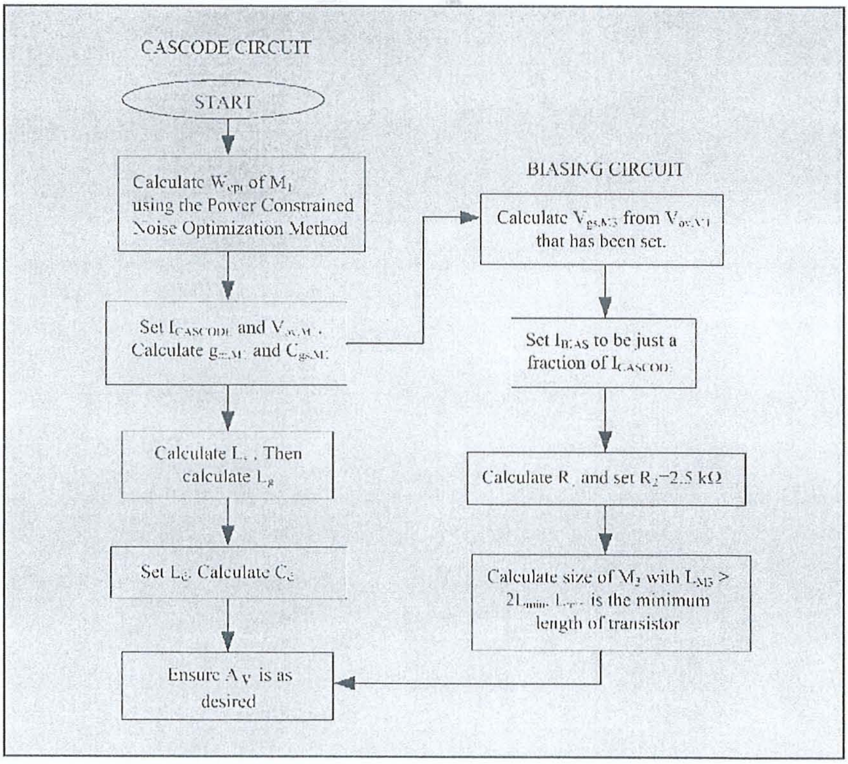


Figure 2 : Flowchart of the LNA design methodology

Table 1 : List of symbols.

g_m	Transconductance of the transistor
a	Noise parameter, α and $\alpha = g_m / g_{d0}$
μ_n, μ_p	Mobility of electron, hole
C_{oxn}, C_{oxp}	Oxide capacitance. For NMOS, $C_{oxn} = 9.4 \times 10^{-3}$ F/m^2. For PMOS, $C_{oxp} = 8.9 \times 10^{-3}$ F/m^2
W	Transistor's width
L	Transistor's channel length
V_{ov}	Overdrive voltage
K_{ox}	Relative permittivity of silicon dioxide
ε_0	Permittivity of free space, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
t_{ox}	Oxide-thickness
Q_S	Quality factor in the form of the actual source (input) conductance
C_{gs}	Gate-Source capacitance
γ	Noise parameter, $\gamma = 2/3$ for long-channel
δ	Coefficient of gate noise, $\delta = 2\gamma = 4/3$ for long-channel
c	Correlation coefficient, c = j0.395 for long-channel devices
f_T	Transition frequency
F	Noise factor
ω_T	Transition angular frequency
ω_o	Operating angular frequency
χ	Noise parameter that includes both correlated and uncorrelated portions of the transistor's gate noise

$$Q_S = \frac{1}{\omega_o R_S C_{gs}} \tag{2}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{3}$$

Therefore,

$$W = \frac{3}{2C\omega_o Q_S R_S LC_{ox}} \tag{4}$$

Transition frequency,

$$\omega_T \approx \frac{g_m}{C_{gs}} \approx \frac{g_m}{\frac{2}{3} WLC_{ox}} \tag{5}$$

An optimum condition will occur when the quality factor of the source is at its optimum. The optimum Q_S [9, 10]

$$Q_{S,opt} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1 + \sqrt{1 + \frac{3}{|c|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \tag{6}$$

With $|c| = 0.395$ and $\gamma/\delta = 0.5$, $Q_{S,opt}$ is calculated to be 4 [9]. The difference in the noise factor is not very significant when $Q_{S,opt}$ is changed from 3.9 to 4.5 [11, 12]. $Q_{S,opt} = 4.5$ can be chosen to enable the value of smaller transistor at the input. A smaller device consumes smaller current, and consequently, power. Based on Equation (4), $Q_{S,opt} = 4.5$, when $W_{opt} = 293$ µm. W_{opt} is the optimum width of the transistor at the lowest noise figure (NF). For physical transistor design, a multi-finger technique can be implemented for better matching and reduced gate resistance [12]. If multi-finger transistor is used, every finger needs to have a consistent width. If 5 μm is used, the total width of the transistor must be in multiplication of 5 μm [12]. Hence, W_{opt} can be taken as 290 μm. Based on Equation (1) to Equation (5), calculated C_{gs} is 0.33 pF, g_m is 59 mA/V, ω_T is 1.7879 rad/s, f_T = 28.4 GHz, ω_T/ω_o is 13.3 at f_o= 2.14 GHz (the W-CDMA operating frequency). When L_g and gate resistance contributions to the noise are neglected, the noise factor is found to be [12]:

$$F = 1+4.84\ (\omega_o/\omega_T). \tag{7}$$

From Equation (7), F is found to be 1.364. For the calculation above, V_{ov} is 100 mV. This is a reasonable estimation for a 0.18 μm design as it provides some margin for process variation.

(ii) Calculation of L_s and L_g

The input impedance of the inductively-degenerated LNA in Figure 1 is given in Equation (8) [10].

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{8}$$

At resonance, only the real part of Equation (8) exists. The input resistance is given by (9) indicating that the combination of the transistor with the degeneration inductor provides input matching [1].

$$R_{in} = \mathrm{Re}\left[Z_{in}\right] = \frac{g_m L_s}{C_{gs}} \tag{9}$$

Also at resonance,

$$L_g = \frac{1}{\omega_o{}^2 C_{gs}} - L_s \tag{10}$$

L_g should not be large as it can contribute to a higher NF. This is because [9]

$$F = 1 + \frac{R_{L_g}}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_S}\left(\frac{\omega_o}{\omega_T}\right) \tag{11}$$

where R_{Lg}, R_g and R_s are the L_g, gate and input source resistances, respectively. Referring to Equation (10), the L_g can be made smaller if C_{gs} and L_s can be made larger. Referring to Equation (3), C_{gs} is dependent on the width and length of the transistor. A small device will need a large width in order to increase its C_{gs}. The trade-off to fulfilling this requirement is in the higher current consumed (hence, higher power consumption) as can be seen from Equation (12),

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right)^2 \tag{12}$$

On the other hand, if the L_s is increased, the voltage gain will be degraded as shown by the open circuit voltage gain equation below [12].

$$A_{vo} = \frac{-g_m \omega_o{}^2}{\begin{bmatrix} s^2 C_{gs} \omega_o{}^2 \\ \left(L_g + L_s\right) \end{bmatrix} + s\omega_o{}^2 \begin{bmatrix} C_{gs}\left(R_s + R_{L_g}\right) \\ + g_m L_s \end{bmatrix} + \omega_o{}^2} \frac{sL_d + R_{L_d}}{\begin{bmatrix} s^2 L_d C_d \\ + sC_d R_{L_d} + 1 \end{bmatrix}} \tag{13}$$

where R_{Ld} and R_{Lg} are the internal resistances of L_d and L_g, respectively. In SNIM, the problems arise in achieving high gain and good noise performance when the device is small.

Assuming α as equals to 1, and R_{in} is 50 Ω, L_s can then be calculated. From Equation (9), L_s = 0.28 nH ≈ 0.3 nH. However, the smallest inductor available from the Silterra 0.18 μm CMOS model libraries is 1.65 nH. Hence, the smallest inductance that can be used (with size of design taken into consideration) is 0.55 nH from three of the 1.65 nH connected in parallel. L_g can be calculated by using Equation (10) and with the mentioned values, L_g is 16.2 nH. The nearest inductance value from the Silterra model libraries is 15.8 nH.

(iii) L_d and C_d

C_d can be calculated from Equation (14) with the operating frequency of 2.14 GHz [13] and L_d set to a certain value.

$$\omega_o = 1\big/\sqrt{C_d L_d} \tag{14}$$

If L_d is set at 15.8 nH, C_d is calculated to be 0.35 pF.

(iv) Biasing Circuit

The biasing circuit has M_3 which forms a current-mirror with M_1. For a W-CDMA application 0.18 μm LNA design, a total current of 4 mA is expected [14, 15]. Thus, the current through M_3 can be in hundreds of μA since a too high of a current for the biasing circuitry will only increase the overall current consumption of the LNA. The equation relating the transistors of the current mirror with their associated currents are shown below.

$$\frac{W_{M_1}/L_{M1}}{W_{M3}/L_{M3}} = \frac{I_{D,M1}}{I_{D,M3}} \qquad (15)$$

Since M_3 should not be large to prevent large current consumption by the biasing circuit, a 20 µm width transistor is capable of carrying the amount of estimated current. The length of M_3 should not be at its minimum and, hence, was set to 0.36 µm. Since $V_{ov,M1} = 0.1$ V, $V_{GS,M1}$ can be determined from $V_{ov,M1} = V_{GS,M1} - V_{th,M1}$. $V_{GS,M1} = V_{GS,M3} = V_{DS,M3.}$ Once $V_{DS,M3}$ is known, R_1 can be calculated from $(V_{DD} - V_{DS,M3})/I_{BIAS}$. The value of R_2, on the other hand, is not very critical as long as it is much greater than the impedance at the gate of M_1 but small enough to be contributing insignificantly to the noise performance of the LNA. R_2 can be 2.5 kΩ.

(v) C_c

C_c is the coupling capacitor and the capacitance can be any large value such as 75 pF.

1.2 PCSNIM LNA

The difference between the SNIM and PCSNIM is the additional C_{ex} in parallel with C_{gs}. The schematic of PCSNIM is shown in Figure 3. C_{ex} can be obtained from

$$C_{ex} = C_t - C_{gs} \qquad (16)$$

The input resistance at resonance now becomes

$$R_{in} = \frac{g_m L_S}{C_t} \qquad (17)$$

and $$L_g = \frac{1}{\omega_0^{\,2} C_t} - L_s \qquad (18)$$

From Equation (18), L_g can be made smaller by increasing C_t. In order to achieve better noise performance (by having a smaller L_g), L_g can be set at 7.66 nH (based on the available inductors from the foundry's model library). Referring to Equation (17), if the transistor's width is to be maintained at 290 µm, the R_{in} can be fixed at its 50 Ω if $L_s/C_t = 847$ H/F. Using simple mathematics, when $L_g = 7.66$ nH, L_s can be calculated to be 0.57 nH. Based on the available Silterra 0.18 µm CMOS model libraries, the smallest inductor is 1.65 nH. To obtain a 0.57 nH, three of the 1.65 nH were connected in parallel resulting in a 0.55 nH of inductance. Hence, $C_t = 0.65$ pF and $C_{ex} = 0.32$ pF.

Compared with SNIM, PCSNIM is able to provide good noise and input matching even when the transistor is small by manipulating the value of $C_{ex.}$

1.3 CR

In the CR topology, M_1 is replaced by the inverter like combination of the PMOS and NMOS. This is to reduce power consumption but at the same time maintaining the transconductance so that the gain will not be reduced [6]. Figure 4 shows the CR LNA. The advantage of having the inverter connection instead of just one NMOS can be explained by analyzing Figure 5. Besides Equation (1), transconductance for a transistor such as in Figure 5 (a) can also be represented by

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)(I_D)} \qquad (19)$$

For the circuit in Figure 5 (b):

$$g_{m1} = \sqrt{2\mu_n C_{oxn}\left(\frac{1}{2}\frac{W}{L}\right)\left(\frac{1}{2}I_D\right)} = \frac{1}{2}\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \qquad (20)$$

$$g_{m2} = \sqrt{2\mu_p C_{oxp}\left(\frac{1}{2}\frac{W}{L}\right)\left(\frac{1}{2}I_D\right)} = \frac{1}{4}\sqrt{2\mu_n C_{oxn}\frac{W}{L}I_D} \qquad (21)$$

with the assumption that $\mu_p = \mu_n/4$ and $C_{oxn} \approx C_{oxp}$. g_{m1} and g_{m2} are the transconductances for M_1 and M_2, respectively. Hence, $g_{mT} = 3/4\ g_{m.}$ Although I_D is halved due to halved transistor size, g_m is ¾ of its original value. We can say that to produce a similar g_m, the current flowing through this inverter is half of that flowing through the M_1 in SNIM and PCSNIM.

(i) Calculation of transistor size

$V_{GS,M1} = V_{G,M1} = V_{G,M2} = 0.75$ V to ensure that both M_1 and M_2 are in saturation. This will provide about 0.25 V of overdrive voltage as $V_{th} \approx 0.5$ V. If the total current flowing through the W-CDMA LNA is expected to be 4 mA and allocating a few hundred

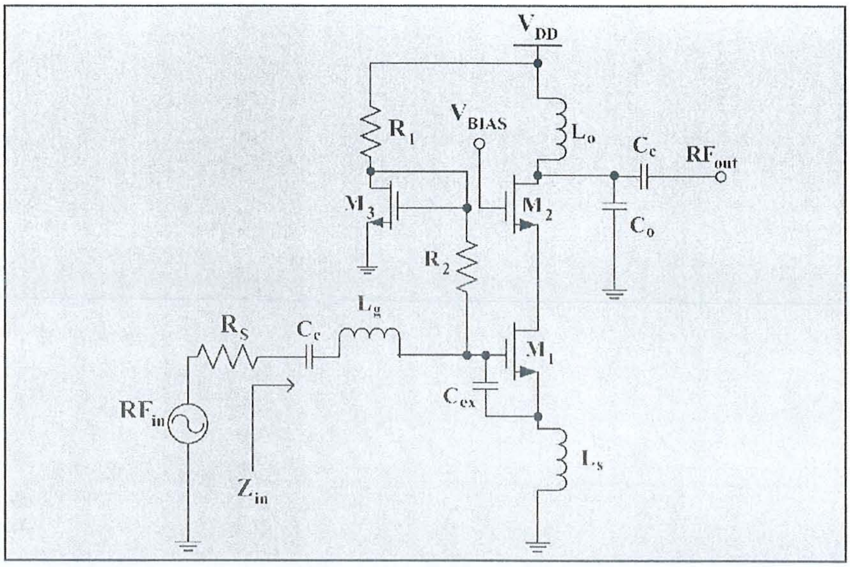


Figure 3 : The PCSNIM cascode LNA with additional capacitor across the input transistor

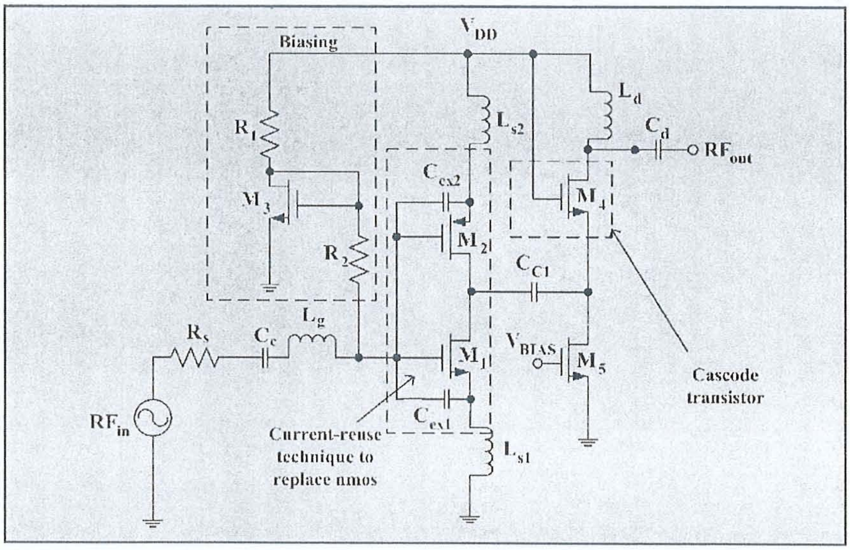
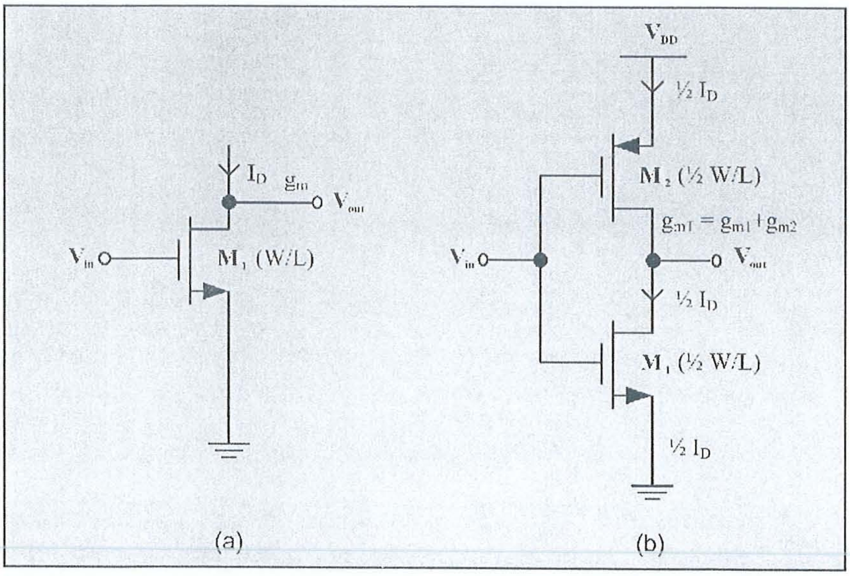


Figure 4 : The CR LNA



(a) (b)

Figure 5 : (a) Single NMOS. (b) NMOS and PMOS in inverter connection [6],[16]

μA for the biasing circuit, then M_1 (in the conventional cascode like in SNIM and PCSNIM) of 60 μm is sufficient to let this value of current flow (refer to Equation (12)). Since M_4 in Figure 4 is operating the same way as the cascode transistor in the conventional cascode circuit (like in SNIM and PCSNIM), it will have the same size as the M_1. Since the same g_m from M_1 in the conventional cascode (like in SNIM and PCSNIM) can be obtained with only approximately half the current (i.e. 1.9 mA) from the inverter NMOS and PMOS in CR, the size of the PMOS and NMOS in the inverter can be halved.

(ii) Determining the passive components at the input stage

C_{ex1} and C_{ex2} were implemented to enable a smaller L_g to be used (as discussed under PCSNIM). Assume $L_{s1} \approx L_{s2}$, $C_{t1} = C_{gs1} + C_{ex1}$ and $C_{t2} = C_{gs2} + C_{ex2}$. $C_{gs1} \approx C_{gs2}$ as $W_1 = W_2$ and $C_{ox1} \approx C_{ox2}$ (refer to Equation (3)). Taking $C_{ex1} = C_{ex2}$ will result in $C_{t1} = C_{t2}$. The input impedance of the circuit in Figure 4 is as shown in Equation (22). At resonance $R_{in} = R_e[Z_{in}] = 50\ \Omega$.

$$Z_{in} = sL_g + \frac{\begin{gathered}2\left(\frac{1}{s^3C_t^3} + s^3L_{s1}^3\right) + \left\{\begin{matrix}2\left(\frac{3L_{s1}}{sC_t^2} + \frac{3sL_{s1}^2}{C_t}\right) - \\ \frac{5}{4}\left(\frac{1}{sC_t} + sL_{s1}\right)\left(\frac{L_{s1}}{C_t}\right)^2 g_{m1}^2\end{matrix}\right\} \\ + \frac{3}{2}\left(\frac{1}{s^2C_t^2} + s^2L_{s1}^2\right)\left(\frac{L_{s1}}{C_t}\right)g_{m1} + 3\left(\frac{L_{s1}}{C_t}\right)^2 g_{m1} \\ - \frac{3}{4}\left(\frac{L_{s1}}{C_t}\right)^3 g_{m1}^3\end{gathered}}{4\left(\frac{1}{s^2C_t^2} + \frac{2L_{s1}}{C_t} + s^2L_{s1}^2\right) - \frac{9}{4}\left(\frac{L_{s1}}{C_t}\right)^2 g_{m1}^2} \tag{22}$$

By using $C_{gs1} = 0.0341$ pF and $g_{m1} = 15.25$ mA/V for the 30 μm M_1 of the CR LNA, $L_{s1} = 0.3$ nH. To determine L_g, the total imaginary part of Equation (22) is 0. It is calculated that L_g is 40 nH [8]. This is a very large inductor connected at the input and can contribute to a very high noise performance. As L_{s2} is connected to V_{DD} and a bondwire inductance to other than ground is 1.2 nH, the total inductance between the drain of M_2 and the external V_{DD} source is 1.5 nH.

Optimization of L_g and L_s can be performed to obtain good performance in gain and noise. Optimization may result in L_s to be 0.55 nH (a parallel of three 1.65 nH) and L_g = 12.9 nH (which will give better noise performance).

(iii) L_d and C_d

Since the L_d is to resonate with C_d , L_d can be set to 12.9 nH and C_d is then calculated to be 0.43 pF (using Equation (14)).

(iv) Biasing circuit

Since $V_{GS,M1} = V_{GS,M3} = V_{DS,M3} = 0.75$ V, the $V_{ov,M3}$ will be large as $V_{th,M3} \approx 0.5$ V. To prevent a large current from flowing through M_3 as this transistor is just for biasing, its width needs to be made smaller. Hence, M_3 can have a width of 10 μm with length of 0.36 μm, making 12 as the ratio of the mirrored current to the bias current (using Equation (15)). Thus, the current in the biasing circuit was estimated to be 0.32 mA. With the drain voltage of M_3 known, R_1 can be calculated. R_1 = (1.8-0.75) V / 0.32 mA ≈ 3.3 kΩ.

(v) Determining the size of M_5

With a current of 1.58 mA flowing through M_4 (i.e. 3.8 mA - 0.32 mA – 1.9 mA), M_5 was added to the circuit to act as the current source. V_{GS} of the M_5 was set to 0.75 V and with this biasing condition, a 20 μm by 0.18 μm is sufficient to perform the task (using Equation (12)).

(vi) C_{c1}

For the C_{C1}, the capacitor's function is to isolate the dc flowing through M_4 from the biasing through the inverter pair. A capacitance of 0.92 pF can be implemented to perform this task.

1.4 FC

The folded-cascode LNA is shown in Figure 6. M_1 is to amplify the signal and M_2 acts as the current buffer. The supply voltage is close to the bias voltage and thus the output swing is limited. The folding of M_2 helps to eliminate the parasitic capacitances at the drain of M_1 by resonating with L_d. It also helps to suppress the noise contribution of a common gate transistor like M_2 at the output [17]. L_o is to resonate with the output capacitance at the operating frequency.

The width of M_1 is determined from Equation (4) with the parameter values as specified for SNIM and PCSNIM. Since the impedance of FC is approximately the same as the input impedance of PCSNIM, L_g, C_{ex} and L_s can be determined by the same way.

Current that is expected to flow through M_1 can be calculated from Equation (12) and found to be 1.89 mA when V_{ov} = 80 mV (the overdrive voltage needs to be small as V_{DD} is close to the bias voltage). The total current supplied to the LNA was set at 4 mA. If the bias current through M_3, $I_{D,M3}$, is set at 0.1 mA, the current through M_2, $I_{D,M2}$, will be 4 mA – 1.89 mA – 0.1 mA = 2 mA. $R_1 = (0.6 - 0.58)$ V/ 0.1 mA = 0.2 kΩ.

The width of M_2 can be calculated from Equation (12). $V_{ov,M2} \approx 0.2$ V ($V_{SG,M2} = 0.6$ V and threshold voltage of PMOS is about 0.4 V for a 0.18 μm process). Hence, $W_{M2} \approx 180$ μm. By using Equation (3), $C_{sg,M2}$ is 0.2 pF. L_d is to resonate with $C_{sg,M2}$ to tune to 2.14 GHz. Using Equation (14), $L_d = 29$ nH. The highest available inductor with the Silterra 0.18 μm CMOS model libraries is 22.9 nH. Equation (14) can be used again to determine C_o. If L_o is set at 10.7 nH, C_o is calculated to be approximately 0.52 pF.

1.5 PCSNIM with output buffer

Referring to Figure 7, the input stage of this topology is the same with the PCSNIM shown in Figure 3. The buffer is implemented as a cascode on its own has very high output impedance. If the PCSNIM is connected directly to a load with low impedance, the gain will drop drastically. Hence, the buffer, which is actually the source follower M_4, acts as an impedance transformer to avoid the loading effect. M_5 is operating as a current-source. L_d is to resonate with C_d, $C_{gs,M4}$, C_o and $C_{gd,M5}$ to provide tuning at the 2.14 GHz. C_{c1} is the coupling capacitor that will isolate the biasing of the buffer from the cascode. R_o is to function the same way as R_2. The width of M_1, g_m and C_{gs} can be maintained at 290 μm, 0.33 pF and 59 mA/V, respectively. L_g, L_s and C_{ex}

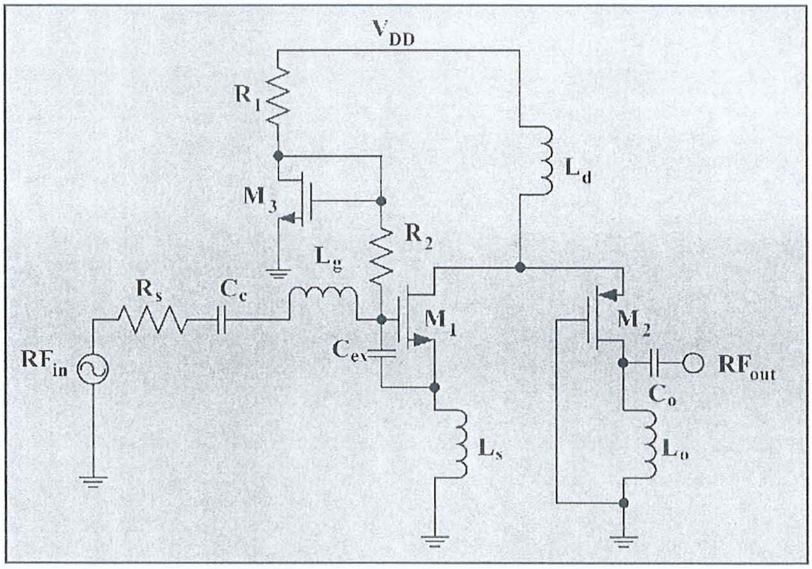


Figure 6 : The FC LNA

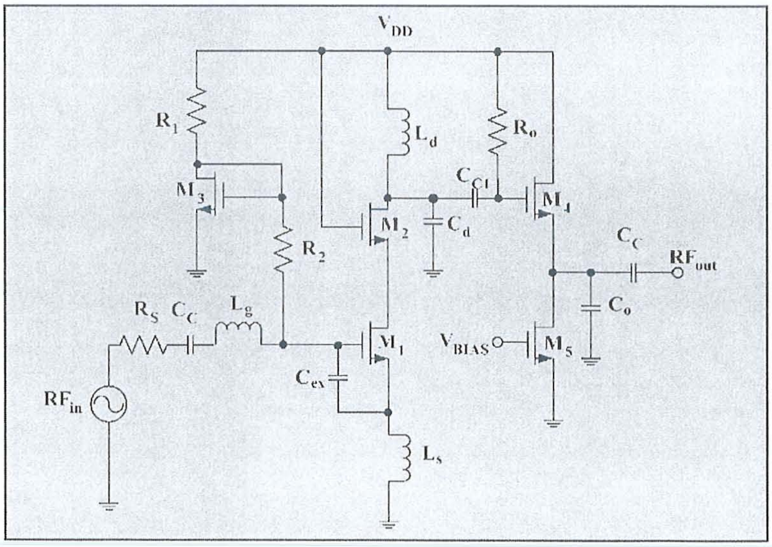


Figure 7 : The modified PCSNIM with output buffer LNA

Table 2 : Design parameters and optimized component values used in the SNIM, PCSNIM, CR, FC and PCSNIM with output buffer.

	SNIM	PCSNIM	CR	FC	PCSNIM with buffer
f_0 (GHz)	2.14				
L (μm)	0.18				
t_{oxn}, t_{oxp} (nm)	3.65, 3.88				
C_{oxn}, C_{oxp} (mF/m^2)	9.45, 8.9				
R_S (Ω)	50				
μ_n, μ_p (m^2/Vs)	0.039, 0.01				
R_1, R_2 (kΩ)	9, 2.5	9, 2.5	3.3, 10	0.2, 10	9, 2.5
R_O (kΩ)	na	na	na	na	2.5
C_c (pF)	75	75	75	1	75
C_{c1} (pF)	na	na	0.92	na	10
$C_{gs,M1}$ (pF)	0.33	0.33	0.03	0.33	0.33
C_{ex} (pF)	na	0.32	0.18 for both	0.32	0.32
C_d (pF)	0.35	0.35	0.43	na	0.35
C_o (pF)	na	na	na	0.52	0.13
L_g (nH)	15.8	7.66	12.9	7.66	7.66
L_d (nH)	15.8	15.8	12.9	22.9	15.8
L_s (nH)	0.55	0.55	na	0.55	0.55
L_{s1},L_{s2} (nH)	na	na	0.55	na	na
L_o (nH)	na	na	na	10.7	na
M_1 (μm/μm)	290/0.18	290/0.18	30/0.18	290/0.18	290/0.18
M_2 (μm/μm)	290/0.18	290/0.18	30/0.18	180/0.18	145/0.18
M_3 (μm/μm)	20/0.36	20/0.36	10/0.36	40/0.36	20/0.36
M_4 (μm/μm)	na	na	60/0.18	na	100/0.18
M_5 (μm/μm)	na	na	20/0.18	na	100/0.18

* *na means "not applicable".*

Table 3 : Summary of the comparison between the different modified inductively-degenerated cascode LNA.

LNA Topology	Features
SNIM	This is the conventional inductively –degenerated CS with L_s as its degeneration inductor.
PCSNIM	Contains L_s and an additional capacitor, C_{ex}, across the G-S of the input transistor. This configuration is to obtain noise input impedance that closely matches the circuit input impedance.
CR	An NMOS and a PMOS in a CMOS inverter configuration replaces the input NMOS transistor in the SNIM. This configuration enables lower current consumption without deteriorating the transconductance much.
FC	The NMOS and PMOS in a folded-cascode configuration. The supply voltage is slightly more than the biasing voltage. This configuration is suitable for low-voltage operation.
PCSNIM with output buffer	The buffer transforms the high output impedance of the cascode to a value equals to the 50 W required. The buffer is a common-drain with a common-source current source. The output impedance of the common-drain determines the output impedance of this LNA and can be made to equal 50 W by setting the size of M_4 . With the improvement in the output matching, gain and NF also improve.

Table 4 : Post-layout simulated performance metrics of the 5 LNAs with the W-CDMA requirements at 2.14 GHz.

Performance Metrics	SNIM	PCSNIM	PCSNIM with buffer	CR	FC	W-CDMA (Reynolds, 2003b)
S_{21} (dB)	11.0	8.1	19.6	17.1	13.8	15±1
S_{11} (dB)	-10.2	-16.1	-10.9	-11.3	-10.4	<-10
S_{22} (dB)	-1.0	-0.6	-13.4	-22.0	-10.6	<-10
S_{12} (dB)	-38.9	-37.7	-44.8	-51.6	-43.3	<-20
NF (dB)	2.8	1.8	1.7	2.2	1.9	<2.5
IIP_3 (dBm)	-1.9	1.3	-9.9	-3.4	-1.9	-3
I_{DC} (mA) (cascode)	3.7	3.7	3.9	3.5	3.9	4*
V_{dd} (V)	1.8	1.8	1.8	1.8	0.6	1.8*
Power consumption(mW)	6.7	6.7	7.0	6.3	2.3	7.2

* *V_{dd} and I_{DC} were set at 1.8 V and 4 mA, respectively, due to 0.18µm CMOS technology used and the estimated 9 to 18 dB of gain for an LNA of this technology [14].*

are maintained at the calculated values obtained from the PCSNIM design.

If L_d is fixed at 15.8 nH, C_d is calculated to be 0.35 pF from Equation (14). The output resistance of a source follower like M_4 is $1/g_m$. To transform the output impedance of the cascode to 50 Ω, the ouput resistance of M_4 should be 50 Ω. Hence, g_m=0.02 S. From Equation (1) with α=1 and an overdrive voltage of 0.1 V, $W_{M5} = W_{M4}$ will be approximately 100 µm. Expected current to flow can be calculated from Equation (12) and found to be 1 mA. A large capacitance can be used for C_{c1} while R_o is equals to the value of R_2 of the biasing circuit.

Design parameters and optimized component values used in the SNIM, PCSNIM, CR, FC and PCSNIM with output buffer is shown in Table 2.

2. COMPARISON ON THE INDUCTIVELY-DEGENERATED CASCODE LNA

Table 3 summarizes the distinct features that differentiate the five modified inductively-degenerated cascode LNA topologies discussed in this paper. The SNIM is the conventional inductively-degenerated cascode LNA.

3. RESULTS AND DISCUSSIONS

The simulation performed on all five configurations showed results that conformed to the theory as shown in Table 4. The S_{11} in SNIM and PCSNIM show a much better performance as compared to the S_{22} because of the degeneration inductor, L_s. The inductively-degenerated topology helps in providing input matching on-chip. The S_{22} results also show the difficulty in matching the output stage of both SNIM and PCSNIM to 50 Ω. This is because of the very high output impedance of the cascode network in these two topologies.

Both SNIM and PCSNIM can achieve input and noise matching simultaneously, but the PCSNIM has better noise performance as the L_g contribution to the overall noise was reduced due to the implementation of a smaller L_g. Smaller L_g possessed smaller series resistance and this is the reason for the better NF in the PCSNIM. Smaller L_g can be utilized because of the existence of C_{ex} between the gate and source of M_1 in PCSNIM.

The PCSNIM with output buffer provides on-chip output matching which greatly improves the S_{22}. Due to the matched output, the PCSNIM with output buffer provides the best gain amongst the three topologies.

The CR was found to be able to maintain a comparable gain with the PCSNIM with output buffer although it consumed a lesser current of 3.5 mA as compared to the 3.9 mA consumed by the latter. The power consumption of these two topologies were compared as they both have on-chip matching circuitry and supplied by the same amount of V_{DD}. Hence, it is confirmed that the CR can reduce the amount of current but still maintaining the desired gain.

The FC, which was supplied by the 0.6 V, is not only suitable for low-power designs but achieved a very good NF of 1.9 dB.

The overall results obtained show that the PCSNIM with output buffer can provide good gain and noise performance, but at the expense of the linearity and power consumption. However, this is acceptable if the linearity and power consumption are still within the requirements of the W-CDMA.

4. CONCLUSION

Detailed description on the design and analysis of the inductively-degenerated based LNAs are given. The described LNA topologies are the SNIM, PCSNIM, CR, FC and PCSNIM with buffer. The designs were using the parameters specified by the Silterra foundry for the 0.18 μm CMOS process. Simulation results show that all the topologies are able to fulfill the desired W-CDMA specifications. The SNIM and PCSNIM are able to provide simultaneous input and noise matching, the CR consume the least current, the FC enables very good noise performance and comparable gain at a much reduced supply voltage and finally, the PCSNIM with output buffer can provide on-chip output matching.

5. Acknowledgement

Authors would like to thank Collaborative Micro-electronic Design Excellence Centre (CEDEC) for supporting Cadence EDA and providing the measurement service. Also thanks to Silterra (M) Sdn Bhd. for the 0.18 μm CMOS model libraries and fabrication service. Special acknowledgement to Universiti Sains Malaysia short term research grant for the funding of this work.

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APPENDIX C

1.575 GHz to 2.48 GHz Multi-standard Low Noise Amplifier using 0.18-μm CMOS with On-Chip Matching

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Abstract—**A wideband Low Noise Amplifier (LNA) is demonstrated by using the inductively degenerated LNA architecture. This wideband operates in range of 1.575 GHz to 2.48 GHz frequency band. The design of the LNA utilizes the Power Constraint Noise Optimization (PCNO) technique in determining the device size. The simulation results achieved the maximum power gain S_{21} at 13.7 dB to 10.3 dB, input reflection coefficient S11 at −7.2 dB to −9.5 dB, output reflection coefficient S_{22} at −17 dB to −10 dB, reverse isolation S_{12} at −54.4 dB to −52.1 dB and noise figure (NF) at 2.31 dB to 3.12 dB in the frequency range. Linearity result is based on the Input Third-Order Intercept Point (IIP3) is −5.48 dBm. The design draws and obtained at low total power consumption at 14.4 mW and all results met specification. The design was implemented in 0.18 μm CMOS technology. The performances obtained are from the LNA with on-chip matching circuitries.**

Keywords*- Multi-standard LNA; Inductively degenerated topology; Low power design*

I. INTRODUCTION

Wireless communication has evolved into fulfilling the needs of multi-standard applications. This is to satisfy the customers and economic requirement. More benefits can be obtained by having more standards in one system. [1]. As such, we may have a reception unit operating at frequencies of 1.575 GHz for GPS, 2.11 − 2.17 GHz for UMTS and 2.4 − 2.48 GHz for Bluetooth and WLAN [2].

The primary challenge in designing multi standard receivers is increasing functionally hardware LNA [2]. LNA is commonly used as the first stage in the receiver front-end. Hence, having a good LNA is crucial for the suitable performance of the receiver in the communication environments. The performance requirements of RF receivers can be quite tough, when requiring good sensitivity, high gain and excellent NF at one time [3]. The multi-standard LNA presented in this paper is based on the technique proposed in [4]. Table 1 shows the requirement performance metric of multi standard LNA.

TABLE I
MULTI STANDARD LNA SPECIFICATIONS [4]

Performance Metrics	Multi-standard LNA (GPS, UMTS, Bluetooth, WLAN)
$\|S_{21}\|_{max}$	> 13.5dB
NF_{max} (in 3dB bandwidth)	3.2dB
IIP3 (worst case)	−4.5dBm
Bandwidth ($\|S_{11}\| < -10$dB)	1.5-2.65GHz
Bandwidth ($\|S_{22}\| < -10$dB)	> 2.55GHz
Bandwidth ($\|S_{12}\| < -50$dB)	1-2.6 GHz
-3dB Bandwidth ($\|S_{21}\|$)	1-2.6 GHz

Section II gives the theory behind work. Section III explores LNA design. Section IV describes the results achieved by proposed work. Last but not least, conclusion given in Section V.

II. PROPOSED LNA ARCHITECTURE

Cascode amplifiers topology combines the high input resistance and large transconductance offered by a Common Source (CS) amplifier with the current-buffering capability and good high-frequency response of a Common Gate (CG) amplifier. Although the cascode is actually a cascade of a CS with a CG, it is normally treated as a single-stage amplifier [5].The advantages of this method are the Miller effects can be reduced and able to improve the performance metric such as the reverse isolation [6].

A. PCNO Technique

In PCNO technique, simultaneous gain and noise matching is possible at any amount of power dissipation. This is achieved by proper selection of the degeneration

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inductor, L_s at any given transistor size [7]. Under fixed drain current, there exists a transistor's width which can result in a low NF. The width of the optimum device is written as follows [8, 9]

$$W_{opt,P_D} = \frac{3}{2}\frac{1}{\omega_o L C_{ox} R_s Q_{s,opt,P_D}} \quad (1)$$

where Q_{s,opt,P_D} is the quality factor of the input circuit of the LNA that leads to the power-constrained minimum NF [8, 9]:

$$Q_{s,opt,P_D} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \quad (2)$$

where $|c|$=0.395 and γ/δ= 0.5 to give $Q_{s,opt,P_D} \approx 4$ [8].

The relationship between the power dissipation, P_D, and F is as follows [5] :

$$P_D = \left[\frac{\gamma\omega_0 L}{3v_{sat}(F-1)}\right]^2 \frac{P_o}{Q_s^3}\left\{\left[1+\frac{\delta}{5\gamma}\right]+2|c|Q_s\sqrt{\frac{\delta}{5\gamma}}+\frac{\delta}{5\gamma}Q_s^2\right\}^2 \quad (3)$$

From the graph plotted for P_D vs Q_s at different steps of F, given in [5], it can be seen that a small NF can be obtained at the expense of a higher P_D. A decrease in power causes a decrease in gain and noise factor. According to Table I, the required NF and gain should be below 3 dB and above 13 dB, respectively; so a trade-off between NF, power gain and power consumption is to be considered when designing the LNA.

B. *Input Impedance Matching*

For impedance matching at the input of the LNA as shown in Fig. 1, the following equation yields the input impedance of the design. At resonance, input impedance is:

$$Z_{in} = R_{in} + jX_{in} \quad (4)$$

where the resistive part of input impedance is:

$$R_{in} = \frac{\frac{B}{B^2-A^2}}{\left(\frac{A^2}{B^2-A^2}\right)^2 - \left(\omega C_1 + \left(\frac{A^2}{B^2-A^2}\right)\right)^2} \quad (5)$$

$$A = \omega L_S + \omega L_2 - \frac{1}{\omega C_{gs}}$$

$$B = \frac{g_m L_S}{C_{gs}}$$

R_{in} is the real part of Z_{in} and it should be set to 50 Ω. The reactance part of impedance is:

$$X_{in} = \omega.\left(L_1 + \frac{\omega C_1 + E}{F^2 - (\omega C_1 + E)^2}\right) \quad (6)$$

$$E = \frac{A}{B^2-A^2} \text{ and } F = \frac{B}{B^2-A^2}$$

where (6) is the imaginary part of Z_{in} and must be set to zero. From (5), g_m, L_2, L_s and C_{gs1} are the transconductance, inductor at the gate M_1, source degenerative inductor and external gate-source capacitance, respectively.

C. *Output Impedance Matching*

For impedance matching at the output of the LNA as shown in Fig. 1, the following equation yields the output admittance of the design [10]:

$$Y_L = sC_d + \frac{1}{r+sL} + \frac{1}{R_d+sL_d} \quad (7)$$

where r is the series resistance of L_d. C_d , L_d , L and R_d are the load capacitor, load inductors and load resistor, respectively. At resonance, C_d, L_d, and L will be eliminated and leaving the real impedance into play.

III. LNA DESIGN

A. *Circuit Implementation*

The design starts with the determination of the optimum width, W_{opt}, of the input transistor, M_1, in Fig. 1 by using the PCNO technique. Optimum width means the width of the input transistor that can provide the circuit input impedance to be very close to the value of the noise input impedance. In this way, the resultant circuit's NF will be close to the minimum NF, NF_{min}.

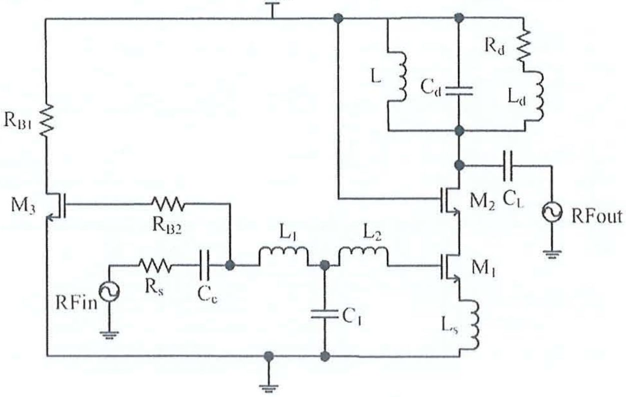

Figure 1. Proposed inductively degenerated cascode LNA for multi-standard applications

The equation used to determine W_{opt} is given in (1) resulting [5],[8]:

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_S} \quad (10)$$

where W_{opt} is the optimum width and L is the effective channel length of the M_1 transistor. C_{ox} is the oxide capacitance and the input circuit quality factor, Q_{in}, is set equal to 4.5.

Schematic design of LNA is shown in Fig. 1. In this figure, a current mirror is formed by the transistor M_1, M_3 and the resistor of R_{B1} for the purpose of DC biasing to the

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input transistor. The ratio of M_3 and M_1 determines the current flowing through the cascode branch. Proper selection of M_1's width determines the voltage across G-S of M_1. The width of M_1 is calculated to be 290 μm. Besides, the smaller width of transistor M_3 is preferred so that the power headroom of the bias circuitry can be minimized. A T-matching network is designed to obtain the desired bandwidth [4]. At biasing circuit, a large resistor value of R_{B2} is chosen to avoid noise performance degradation [4] as well as minimizing the coupling capacitance and load capacitance value.

L and C_d function as tuned load at the output. L_d is added to the circuit in series with resistive load, R_d in terms of gain control and get a good output matching with no output buffer [10]. Due to the inductive nature of this load compensates the gain roll-off of LNA at high frequencies [4]. Degeneration inductor, L_s, enables more flexibility in matching the input stage to 50 Ω. It also influences the gain of the LNA. Combination of L_s and L_g will tune the input to the desired frequency.

From (10), the optimum width of transistor M_1 was obtained equal to 280 μm. The width of cascode transistor M_2 was set equivalent to width of M_1; hence, gate-drain overlap can reduce impedance looking into gate and drain of M_1. However, this will degrade both noise performance and input matching.

This is to accomplish a better IIP3 based on the study by [8]. M_2 has more influence on the linearity performance of the cascode as compared to M_1. In the study performed by [8], it was found that the IIP3 of M_2 improves with the increase of DC biasing of M_2. While L_d enables node capacitance at the drain of M_2 to resonate with it to tune the output to the resonating frequency and provide additional band-pass filtering. To give more flexibility in tuning the output to the desired frequency and additional filtering, C_d is included in the circuit. Hence, L_d let only a very small voltage across it due to its series resistance which is beneficial for low power design. The size of L_s can, in fact, be made smaller to generate a better gain and NF. NF can be improved by lowering L_s because the series resistance grows with the value of inductance and the noise factor is proportional to this series resistance.

B. *Layout Implementation*

Using a standard CMOS 0.18 μm technology, the multi-standard LNA is implemented for 1.575 GHz, 2.11 to 2.17 GHz and 2.4 to 2.48 GHz frequency bands. For circuit verification, Calibre was used to obtain post-layout simulation results. Fig. 2 shows the layout of the LNA.

IV. EXPERIMENTAL RESULT

A. *S-Parameters*

The The proposed design LNA achieved input reflection coefficient, S_{11} of −7.2dB to −9.5dB and output reflection coefficient, S_{22} of −17dB to −10dB in the frequency range of 1.575GHz − 2.48GHz.

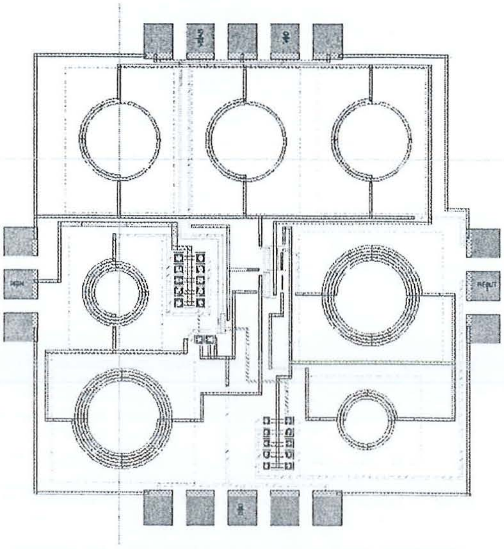

Figure 2. Layout of LNA for multi-standard application

Fig. 3 shows the S-parameter results. The required gain, S_{21} for the wideband LNA application is 13.7 dB to 10.3 dB while the reverse isolation, S_{12} with value of −54.4 dB to −52.1 dB in the required frequency bands. It is observed that LNA exhibits good reserve isolation.

B. *Noise Figure*

The NF is about 2.31 dB to 3.12 dB in the frequency range of 1.575 − 2.48 GHz as can be seen in Fig. 4.

C. *Linearity*

Fig. 5 shows the IIP3 of post-layout result. The result has met the specification of the wideband design, i.e. IIP3 > −3 dBm.

D. *Results Comparison*

Table II gives the summary performance of the LNA achieved in the post-layout simulation in this work in comparison with previous work by [4]. It is found that the gain and the NF performances are slightly worse than the ones obtained by [4]. This is due to the effects by the on-chip matching implemented in this work. The work in [4] has its matching circuitries performed off-chip.

V. CONCLUSION

A wideband LNA is demonstrated by using the inductively degenerated LNA architecture. The designed LNA demonstrated a gain of 13.7 dB, 13.5 dB to 12.6 dB and 2.98 dB to 3.12 dB for the operating frequencies 1.575 GHz, 2.11 GHz to 2.17 GHz and 2.4 GHz to 2.48 GHz, respectively. The minimum gain achieved in this large of frequencies is of 10.3 dB while the maximum NF is 3.12 dB. Total power consumption is 14.4 mW.

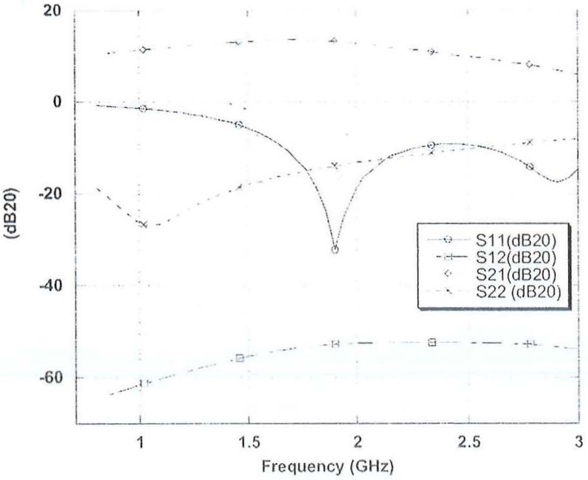

Figure 3. S-Parameter results

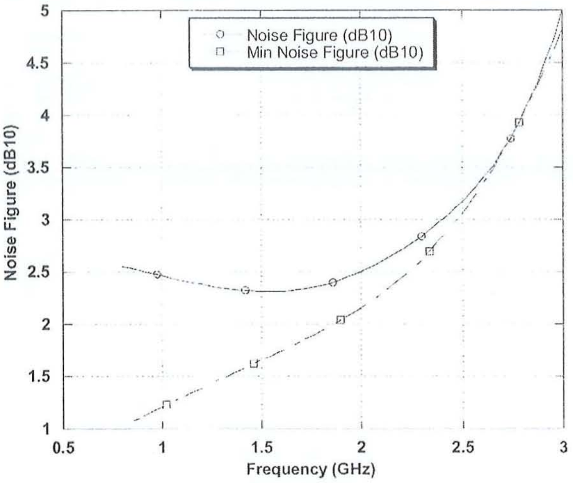

Figure 4. Noise Figure results

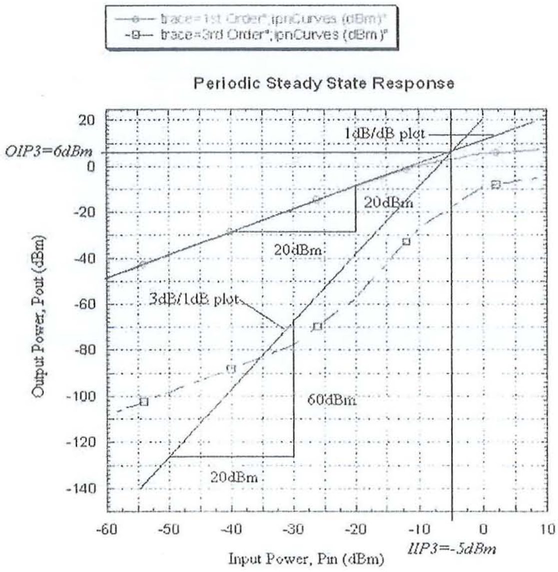

Figure 5. Input third-order intercept point (IIP3) at 2.44 GHz.

TABLE II
RESULTS COMPARISON

Parameters	**Proposed design**	**Previous work [4]**
Frequency (GHz)	1.575-2.4	1.5-2.6
$\lvert S_{21} \rvert$ (dB)	13.7	15.4
NF_{max} (dB)	3.12	0.9
IIP3 (dBm)	-3.01	-2.5
Bandwidth ($\lvert S_{11} \rvert <$ −10dB)	1.7-2.3 GHz	1.5-2.6 GHz

ACKNOWLEDGMENT

Authors would like to thank Collaborative Micro-electronic Design Excellence Centre (CEDEC) for supporting Cadence EDA tools software and the measurement work. Also thanks to Silterra (M) Sdn Bhd. for the 0.18 µm CMOS model libraries and for the fabrication of the chips. Special acknowledgement to Universiti Sains Malaysia incentive and short term research grant for the funding of this work.

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APPENDIX D

Design and Analysis of the Current Reuse Technique and Folded Cascode Power Constrained Simultaneous Noise and Input Matching LNAs with distributed and lumped parasitic

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***Abstract*— Two LNA topologies were implemented to study on the performance of the post-layout simulation with lumped and distributed parasitic. The performance of the post-layout simulation with different types of parasitic is benchmarked against the measurement results for both topologies previously designed using the post-layout simulation with lumped parasitic. The LNA topologies are the Current Reuse Technique (CRT) Power Constrained Simultaneous Noise and Input Matching (PCSNIM) and the Folded Cascode (FC) PCSNIM. These designs were implemented on Silterra's 0.18µm CMOS process. It is found that the post-layout simulations with distributed parasitic better resemble the measurement results. Based on this finding, the optimization of the CRT and FC PCSNIM LNAs were performed. The S_{11}, S_{21} and S_{22} are -14.48dB, 17.44dB and -18.48dB, respectively, for the CRT and -20.52dB, 16.39dB and -22.88dB, respectively, for the FC. The results show that both LNAs are able to comply to the requirements of the WCDMA application.**

***Keywords*— Lumped parasitic, distributed parasitic, Current Reuse Technique, Folded Cascode, PCSNIM.**

I. INTRODUCTION

The common objectives in designing a low noise amplifier (LNA) are to provide high gain, to achieve as minimum noise figure (NF) as possible, to minimize the nonlinearities and finally to have good input and output impedance matching as this will ensure maximum power transfer and optimized gain and noise performances [1]. For wireless applications, additional objectives are to achieve low power consumption and good reverse isolation. These performance metrics are interdependent and not always work in each other's favor. In practice, most of these metrics trade with each other, making the design of the LNA a multi-dimensional optimization problem. Thus, although the LNA circuit is relatively small in size (requiring only a few devices), the optimization of the performance metrics requires intuition and experience to arrive at an acceptable compromise amongst the trade-off.

II. CIRCUIT DESIGN

The LNA design in this work is for the W-CDMA application. TABLE I shows some typical performance requirements for the LNA in such a system.

TABLE I
TYPICAL PERFORMANCE REQUIREMENTS FOR LNA IN A W-CDMA SYSTEM

Parameters	Specifications
Frequency bandwidth	2110 MHz -2170 MHz
Power gain, S_{21}	> 15 dB
Input/Output matching, S_{11} and S_{22}	< -10 dB
Noise Figure, NF	< 2.5 dB
3rd –order Input Intercept Point, IIP_3	> -3 dBm

Two designs have been considered in this work. First design is a Current Reuse Technique (CRT) Power-constrained Simultaneously Noise and Input Matching (PCSNIM) LNA. The second design is a folded-cascode (FC) PCSNIM LNA. The schematics of the CRT and FC topologies are shown in Fig. 1 and Fig. 2, respectively.

PCSNIM is a technique that combines the Simultaneous Noise and Input Matching (SNIM) and Power-constrained Noise Optimization (PCNO) techniques for simultaneous noise and input match and for low power implementation [2], [3]. The input impedance (Z_{in}) and input noise (Z_{opt}) equations for this topology are as shown below [4]:

$$Z_{in} = \frac{1}{sC_c} + sL_g + \frac{1}{sC_t} + sL_s + \frac{g_m L_s}{C_t} \qquad (1)$$

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega_o C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - j\omega L_s \qquad (2)$$

where $C_t = C_{gs} + C_{ex}$, C_{gs} is the gate-source capacitance for M_1, g_m is the transconductance of M_1, ω_o is the operating angular frequency, α, δ, and γ are the noise parameters and c is the noise correlation coefficient. Refer to Fig. 1 and Fig. 2 for L_g, L_s and C_i.

A. CRT PCSNIM LNA.

Figure 1 shows the schematic of CRT PCSNIM [5].

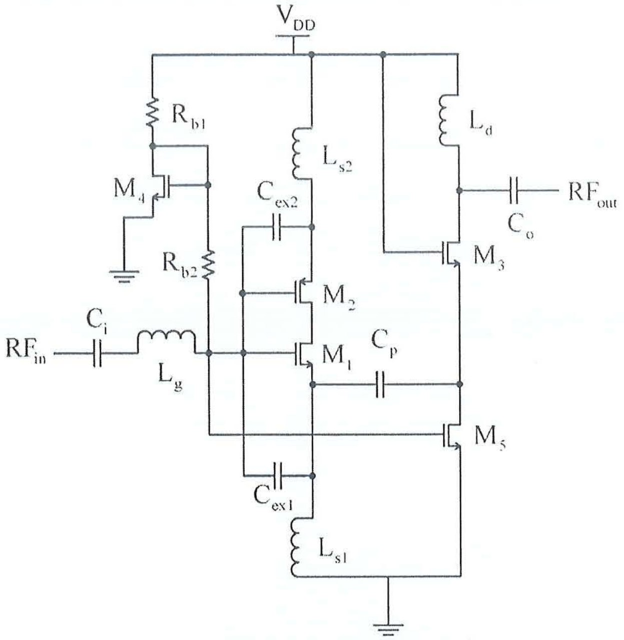

Fig. 1 The CRT PCSNIM LNA schematic [5].

The LNA first stage is an inverter nMOS (M_1) and pMOS (M_2) [6]. The current flowing through M_1 is the same with the current flowing through M_2 because they shared the same supply voltage.

The key of this design is that given the same bias current, the effective transconductance of the coupled transistors is $g_{m1} + g_{m2}$ versus simply g_{m1} for the case when only M_1 exists [4].

$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \qquad (3)$$

$$g_{m2} = \frac{1}{\sqrt{3.9}}\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \approx 0.5g_{m1} \qquad (4)$$

$$g_{mT} = g_{m1} + g_{m2} = 1.5g_{m1} \qquad (5)$$

The result is the transconductance of the single stage is 1.5 times more without having to increase the bias current. The second stage is followed by transistor M_3 configured as a common-gate device. The main purpose of this device is to increase the overall gain of the LNA. Transistor M_4, and resistors R_{b1} and R_{b2}, set the dc bias for M_1 and M_2. Transistor M_4 essentially forms a current mirror with transistors M_1 and M_5. R_{b1} sets the current of the bias circuitry, which generates the bias voltage at the gate of transistor M_1 and M_2. Resistor R_{b2} provides large resistance to the bias circuitry for the input signal. L_g and L_s are used to provide simultaneous noise and input matching. Inductor, L_d is to resonate with the output capacitance for output matching.

It is found that to match the input to 50Ω, L_g has to be very large and therefore occupying more die area. Unfortunately, large value of L_g will also contribute to the increase in NF. To overcome this problem, two C_{ex} are added to the gate of the coupled transistor to reduce the value of L_g. The equation for the input impedance is [4]:

$$Z_{in} = \frac{V_{in}}{I_g} = sL_g + Z_{M1}//Z_{M2} \qquad (6)$$

Optimizing the values for L_g and L_{s1} will result in optimum gain and low noise figure of the LNA.

B. FC PCSNIM LNA.

The idea behind the conventional cascode amplifier is to convert the input voltage to a current and apply the current to a common gate stage [7]. However the input and cascode devices need not be of the same type [6]. For example, a PMOS and NMOS combination can be used to perform the same function. In order for this type of amplifier to operate properly, a current source is needed to bias both transistors. Fig. 2 shows the configuration for the folded cascode LNA. In contrast to the conventional cascode amplifier which requires larger voltage headroom for its operation, the folded-cascode amplifier requires supply voltage close to the bias voltage, V_g of M_1 [7] making it suitable for low power application especially in wireless application. However, one disadvantage of this topology is that it consumes a total bias current which

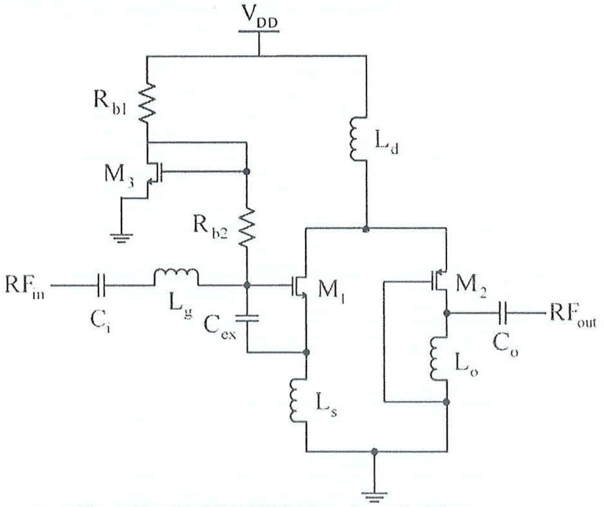

Fig. 2 The FC PCSNIM LNA schematic [7].

is higher than that of the conventional cascode in order to achieve a comparable performance [7].

The operation of the circuit in Fig. 2 is as follows. M_1 acts as an amplifier for the incoming signal and converts the voltage change at the gate to current change in the drain while M_2 act as a current buffer. The folding of the M_2 helps to eliminate the parasitic capacitance at the drain node of the M_1 by resonance with the inductance at the supply pin L_d. This will help suppress the noise contribution of the M_2 at the output and hence avoiding the signal loss into the silicon substrate.

The L_g, L_s and C_{ex} are to provide input matching of the LNA to the source while the L_o provide output matching to the load. The C_i and C_o act as DC block to prevent the leakage of DC voltage to the subsequent stages.

III. EXPERIMENTAL RESULTS

The CRT PCSNIM LNA shown in Figure 1 are having component values of R_{b1}=3.4 kΩ, R_{b2}=10 kΩ, L_{s1}=L_{s2}=0.55 nH, C_i=2.9 pF, C_p=915 fF, C_o=310 fF, C_{ex1}=C_{ex2}=175 fF, L_g=L_d=10.7 nH, W_{M1}=W_{M2}=30 µm, W_{M3}=60 µm, W_{M4}=10µm and W_{M5}=20µm. While FC PCSNIM LNA shown in Figure 2 are having component values of R_{b1}=200 Ω, R_{b2}=10 kΩ, L_s=0.55 nH, C_i=20 pF, C_o=360 fF, C_{ex}=386 fF, L_g=5.35 nH, L_d=6.94 nH, L_o=10.7 nH, W_{M1}=400 µm, W_{M2}=160 µm, and W_{M3}=40 µm.

There were 2 types of post-layout simulation performed in this work; one is using the lumped parasitic and the second is by using the distributed parasitic. The differences in both types of parasitic are shown in Fig. 3. In this work, the lumped is of the C+CC (capacitors and coupling capacitors) type and the distributed is of the R+C+CC (parasitic resistors, capacitors and coupling capacitors) type.

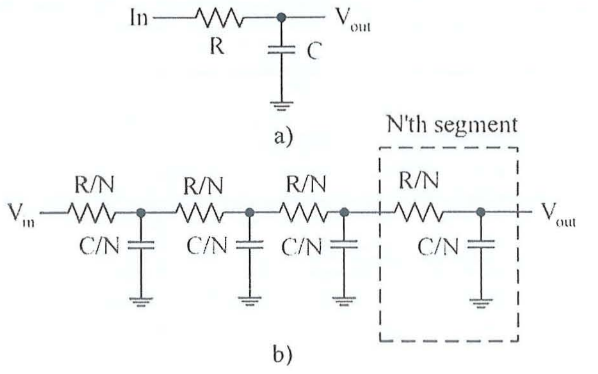

Fig. 3(a) Lumped parasitic and (b) distributed parasitic (N = no. of segments)

By using lumped parasitic, the results will not be as close to the measured results as that can be contributed by the simulation using the distributed parasitic. This is because the lump parasitic will not be able to provide more realistic parasitic as it only considers capacitors in its analysis as compared to the distributed R+C+CC; i.e. resistive and capacitive parasitic [1].

TABLE III

A. CRT PCSNIM LNA.

TABLE II

COMPARISON ON LUMPED AND DISTRIBUTED POST-LAYOUT SIMULATION WITH MEASUREMENT RESULTS FOR THE CRT PCSNIM LNA

Analyses		**S_{11} (dB)**	**S_{12} (dB)**	**S_{21} (dB)**	**S_{22} (dB)**
Lumped post-layout simulation results	Optimum value (dB)	-18.48	-51.07	17.02	-19.49
	Frequency (GHz)	2.06	2.06	2.05	2.06
Distributed post-layout simulation results	Optimum value (dB)	-21.53	-51.33	17.20	-21.30
	Frequency (GHz)	2.18	2.23	2.19	2.24
Measured results	Optimum value (dB)	-22.26	-19.07	6.241	-15.43
	Frequency (GHz)	2.30	2.46	2.56	2.52

TABLE II shows the difference between the post-layout simulations with lumped parasitic, distributed parasitic and the measured results performed on the CRT PCSNIM LNA. When post-layout simulation was performed with the lumped parasitic, the optimum frequencies of the S-parameters had shifted to left of the desired 2.14 GHz. Hence, to optimize the design, the designer will naturally try to move the optimum frequencies to the right. In contrast, the distributed post-layout simulation results show that the optimum frequencies of the same S-parameters had shifted to the right and therefore, the optimization of the design will be to move it to the left. Therefore, the optimization of the lumped simulation will not be accurate since shifting frequency to the right will make the optimum frequency of all S-parameters shifted more to the right when the design comes back from fabrication.

It is seen that post-layout simulations with distributed parasitic give closer readings to the measured results. The measurement plots indicate that the S_{11} and S_{22} are not tuned to the desired 2.14 GHz but differ from it by 7.5% and 17.8%, respectively. In addition, the measured S_{12} and S_{21} are tuned at 2.46 GHz and 2.56 GHz, which are 15% and 19.6% away from the frequency of interest, respectively. This shows that although the lumped post-layout simulation has shown that the optimum frequencies for S-parameters are quite close to 2.14 GHz, the measured results had shown that the frequencies have moved far to the right.

B. FC PCSNIM LNA.

TABLE III shows the difference between the post-layout simulations with lumped parasitic, distributed parasitic and the measured results performed on the FC PCSNIM LNA. It is seen that the post-layout simulations with distributed parasitic give closer readings to the measured results which is similar to the findings found for the CRT PCSNIM LNA.

COMPARISON ON LUMPED AND DISTRIBUTED POST-LAYOUT SIMULATION WITH MEASUREMENT RESULTS FOR THE FC PCSNIM LNA

Analyses		S_{11} (dB)	S_{12} (dB)	S_{21} (dB)	S_{22} (dB)
Lumped post-layout simulation results	Optimum value (dB)	-35.41	-41.73	17.08	-13.42
	Frequency (GHz)	2.08	2.02	1.96	1.96
Distributed post-layout simulation results	Optimum value (dB)	-25.14	-44.39	16.1	-17.63
	Frequency (GHz)	2.14	2.26	2.23	2.29
Measured results	Optimum value (dB)	-8.52	-29.30	8.37	-8.06
	Frequency (GHz)	3.06	3.94	2.08	2.20

The measurement plots indicate that the S_{11} and S_{22} are not tuned to the desired 2.14 GHz but differ from it by 43% and 2.8%, respectively. In addition, the measured S_{12} and S_{21} are tuned at 3.94 GHz and 2.08 GHz, which are 84% and 2.8% away from the frequency of interest, respectively. This shows that although the lumped post-layout simulation has shown that the optimum frequencies for S-parameters are quite close to 2.14 GHz, the measured results had shown that the frequencies have moved far to the right.

C. *The design optimization of the CRT and FC PCSNIM LNAs.*

Based on the finding obtained from the experiments, the design of CRT AND FC PCSNIM LNAs was optimized to conform to the requirements of the WCDMA application. For an optimized CRT PCSNIM LNA, grounded capacitor, C_1=32 pF and C_2=1.57 nF is connected to R_{b2} and L_d, respectively. TABLE IV shows the performance of both topologies after the optimization. For CRT PCSNIM LNA, the changes to the components' values are C_o=370 fF, W_{M1}=W_{M2}=40 μm and W_{M3}=80 μm. For FC PCSNIM LNA design, the changes to the components' values are C_i=4 pF, C_o=410 fF, C_{ex}=350 fF, L_g=7.66 nH, L_d=6.94 nH, L_o=10.7 nH, W_{M1}=320 μm, W_{M2}=200 μm, and W_{M3}=15 μm.

TABLE IV
OPTIMIZED DISTRIBUTED POST-LAYOUT SIMULATION RESULTS OF CRT AND FC PCSNIM LNA

Analyses	CRT	FC
S_{11} (dB)	-14.48	-20.52
S_{12} (dB)	-51.40	-44.58
S_{21} (dB)	17.44	16.39
S_{22} (dB)	-18.48	-22.88

The results displayed are fulfilling the requirements set by the W-CDMA standard. The S-parameters are all tuned to the desired 2.14 GHz.

D. *The photomicrograph of CRT and FC PCSNIM LNA*

Fig. 4 shows the photomicrograph of CRT and FC PCSNIM LNA.

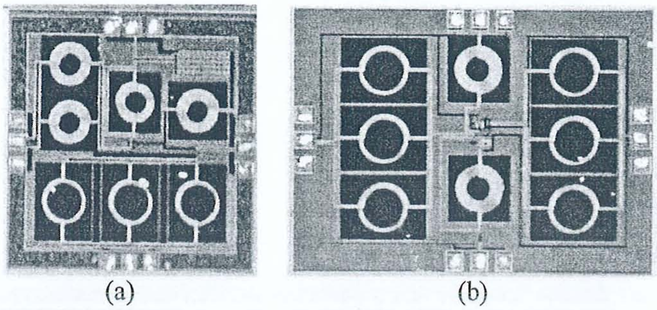
(a) (b)

Fig. 4(a) Photomicrograph of CRT PCSNIM LNA (b) Photomicrograph of FC PCSNIM LNA

IV. CONCLUSIONS

A study on the post-layout with lumped and distributed simulation versus measurement results are shown for two LNA topologies, the CRT PCSNIM LNA and the FC PCSNIM LNA. It is found that the post-layout simulation with distributed parasitic are closely resembling the measured performance. The optimized design post-layout simulation results show that they are closely meeting the specifications of the W-CDMA system desired.

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