UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2013/2014 Academic Session

June 2014

EEE 344 – SYSTEM VLSI
[SISTEM VLSI]

Duration : 2 hours
Masa : 2 jam

Please check that this examination paper consists of **THIRTEEN (13)** pages of printed material before you begin the examination.

*[Sila pastikan bahawa kertas peperiksaan ini mengandungi **TIGA BELAS (13)** muka surat bercetak sebelum anda memulakan peperiksaan ini]*

Instructions: This question paper consists **SIX (6)** questions. Answer **FOUR (4)** questions. All questions carry the same marks.

*[**Arahan:** Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **EMPAT (4)** soalan. Semua soalan membawa jumlah markah yang sama]*

Answer to any question must start on a new page.

[Mulakan jawapan anda untuk setiap soalan pada muka surat yang baru]

"In the event of any discrepancies, the English version shall be used".

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah diguna pakai]

1. (a) Explain the following region of enhancement n-MOSFET with an appropriate cross sectional MOSFET:

Terangkan rantau peningkatan n-MOSFET bersama keratan rentas MOSFET yang sesuai:

(i) Depletion region
kawasan Susutan

(ii) Inversion region
rantau penyongsangan

(20 marks/markah)

(b) Refer to **Figure 1**
*Rujuk **Rajah 1***

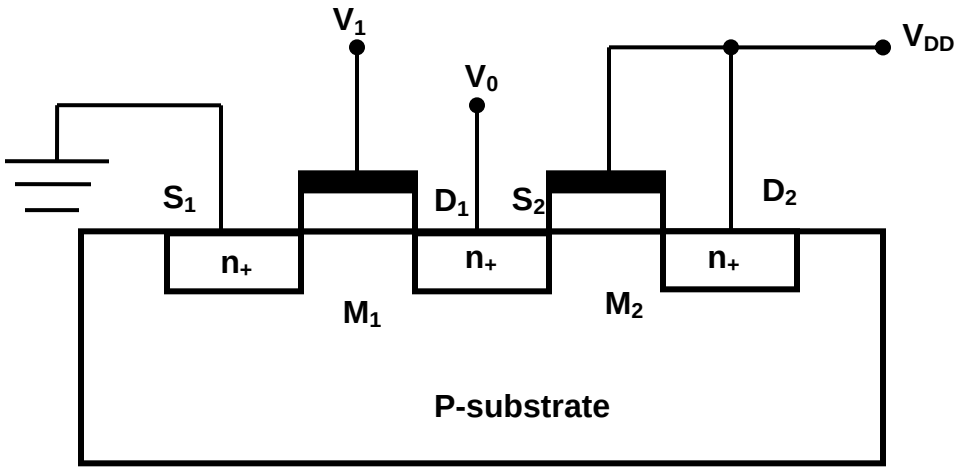

Figure 1
Rajah 1

(i) **Figure 1** shows the configuration of two n-MOSFET transistors (M1 and M2) are connected as series on the p-substrate silicon. When two transistors are conducting, there is a nonzero drain-to-source voltage on M1, which means that the source of M2 is not at the same potential as substrate. Thus, with an appropriate an relationship equation, explain how this configuration can affect the threshold voltage and suggest the solution to avoid the problem.

Rajah 1 *menunjukkan struktur dua transistor n-MOSFET (M1 dan M2) yang disambungkan secara sesiri pada p-substrat silikon. Apabila dua transistor di dalam mod* ***ON****, terdapat voltan bukan sifar antara longkang ke sumber di M1, ini bermaksud bahawa sumber M2 tidak pada voltan yang sama pada substrat. Oleh itu, dengan persamaan hubungan yang yang sesuai, terangkan bagaimana konfigurasi ini boleh menjejaskan voltan ambang dan cadangkan penyelesaian untuk mengelakkan masalah tersebut.*

(30 marks/markah)

(ii) M2 is replaced to the enhancement n-MOSFET. Then M2 is assumed as load and M1 is assumed as deriver. From this cross sectional, sketch the suitable schematic circuitry.

M2 digantikan kepada penambahan n-MOSFET. Kemudian M2 diandaikan sebagai beban dan M1 diandaikan sebagai pemandu. Dari keratan rentas ini, lakarkan litar skematik yang sesuai.

(10 marks/markah)

(iii) From answer (ii), determine the dc transistor currents and voltages in the circuitry. Consider the transistor parameters:

Dari jawapan (ii), tentukan arus transistor at dan voltan pada litar itu. Pertimbangkan parameter transistor:

V_{TND} = 1V, V_{TNL}=-2V, K_{nD} = 50 µA/V^2, and K_{nL} = 10 µA/V^2. Determine the V_0 for V_1 = 5V.

(40 marks/markah)

2. (a) Explain the voltage transfer characteristic (VTC) with an ideal graph for V_{out}-V_{in}. In this graph label the V_{th} and V_{DD}

Terangkan ciri pindah voltan (VTC) dengan graf V_{out}-V_{in} yang sesuai. Labelkan V_{th} dan V_{DD} di dalam graf tersebut.

(10 marks/markah)

(b) State 3 advantages of depletion load inverter compared with enhancement load inverter.

Nyatakan 3 kelebihan beban kekurangan penyongsang berbanding dengan beban peningkatan penyongsang.

(10 marks/markah)

(c) Refer to **Figure 2**,
*Rujuk kepada **Rajah 2***

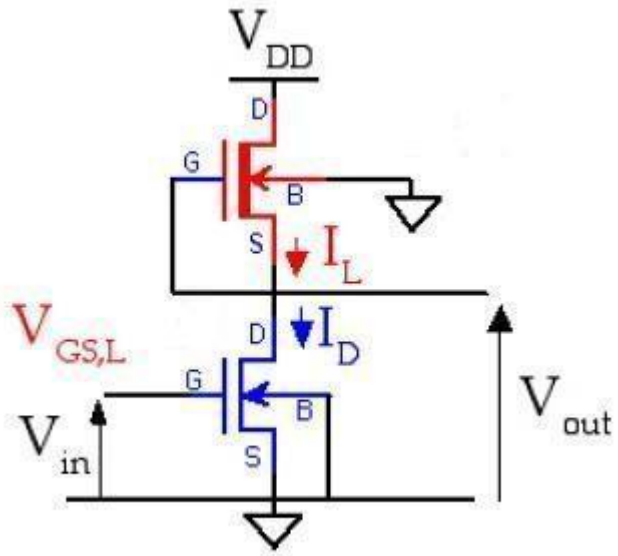

Figure 2
Rajah 2

Assume width, length, threshold voltage load, transconductance n-MOSFET and relative transconductance are *W, L,* V_{T0}, K_n and K_R, respectively.)

Anggapkan lebar, panjang, beban voltan ambang, transkonduktor n-MOSFET dan transkonduktor relatif adalah masing masing W, L, V_{T0}, K_n *dan* K_R.)

(i) Derive for I_L, I_D for load and driver transistor

Terbitkan bagi I_L, I_D *untuk beban dan pemandu transistor*

(40 marks/markah)

(ii) Derive the critical voltage V_{OH} and V_{OL} for this inverter.
Terbitkan V_{OH} voltan yang kritikal dan V_{OL} penyongsang ini

(40 marks/markah)

3. (a) Sketch the CMOS inverter circuitry and show the oxide capacitance, junction capacitance and interconnect capacitance. Then show the C_{load} at worst case.

Lakarkan litar penyongsang CMOS dan tunjukkan kemuatan oksida, kemuatan simpang dan kemuatan sambung. Kemudian tunjukkan C_{load} pada kes terburuk.

(15 marks/markah)

(b) Define the delay time with an appropriate graph for V_{in}-*t* and V_{out}-*t* for **ideal input** Show the equation for an average propagation delay.

Tentukan masa tunda dengan graf yang sesuai bagi V_{in}-t dan V_{out}-t untuk input ideal. Tunjukkan persamaan untuk lengah perambatan purata

(15 marks/markah)

(c) Consider a CMOS inverter with Cload = 1.0 pF and VDD = 5V, where the IV characteristics of the n-MOS transistor driver are

$$k_n' = \mu_n C_{ox} = 20\ \mu A/V^2,\ (W/L)_n = 10 \text{ and } V_{TOn} = 1.0V$$

Pertimbangkan penyongsang CMOS dengan C_{load} = 1.0 pF dan V_{DD} = 5V dan ciri-ciri IV pemandu n-MOS transistor adalah

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Use both the average-current method and differential equation method, calculate τ_{fall} (time elapsed between the time $V_{out} = V_{90\%}$=4.5 V to $V_{out} = V_{10\%}$=0.5V)

Gunakan kedua-dua kaedah purata semasa dan kaedah persamaan pembezaan, kirakan τ_{fall} (masa berlalu antara masa yang $V_{out} = V_{90\%} = 4.5$ V untuk $V_{out} = V_{10\%} = 0.5V$)

(40 marks/markah)

(d) Determine W_n and W_p of the n-MOS and p-MOS transistor based on the following specification

Tentukan W_n dan W_p untuk n-MOS dan p-MOS transistor berdasarkan spesifikasi berikut

(i) Delay time of 2 ns for a V_{out} transition from 4V to 1V with C_{load} = 1.0 pF

masa lewat 2 ns untuk peralihan V_{out} dari 4V ke 1V dengan $C_{load} = 1.0$ pF

(ii) V_{th} = 2V and V_{DD} = 5V

$V_{th} = 2V$ dan $V_{DD} = 5V$

Process and device parameters are as follows:
Proses dan parameter peranti adalah seperti berikut:

$K_n' = \mu_n C_{ox}$ = 30μA/V2

$K_p' = \mu_p C_{ox}$=10μA/V2

$L_n = L_p$=1.0μm

V_{TOn}=1.0V

V_{TOp}=-1.5V

W_{min}=2 μm (limited by design rules)
W_{min}=2 μm (dihadkan oleh undang undang rekabentuk) 30 marks

(30 marks/markah)

4. (a) What is a definition of sequential circuit?
Apakah definisi litar berjujukan?

(20 marks/markah)

(b) Draw a gate-level circuit which can implement the SR flip flop truth table as shown in Table 4.
Lukis litar aras-get flip flop SR mengikut jadual kebenaran seperti pada Jadual 4.

(20 marks/markah)

S	R	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

Table 4 : SR flip flop Truth Table
Jadual 4 : Jadual Kebenaran Flip Flop SR

(c) Draw a basic CMOS Master Slave Flip Flop.
Lukiskan flip-flop tuan-hamba mengunakan get CMOS.

.(60 marks/markah)

5. (a) (i) Determine logic function F based on circuit in Figure 5(a).
Tentukan fungsi logic F berdasarkan Rajah 5(a).

(ii) Calculate W_L/L_L so that V_{OL} does not exceed 0.3 V.
Kirakan W_L/L_L supaya V_{OL} tidak melebihi 0.3 V.

$V_{T,load} = -3V$, $V_{T,driver} = 1$ V

(30 marks/markah)

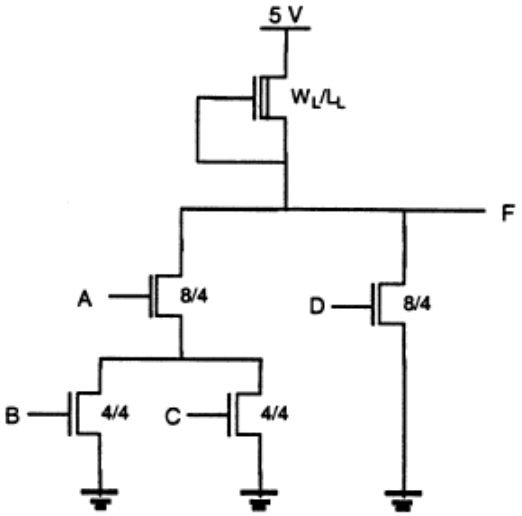

Figure 5(a) : A Dynamic Logic Circuit
Rajah 5(a) : Litar logik dinamik

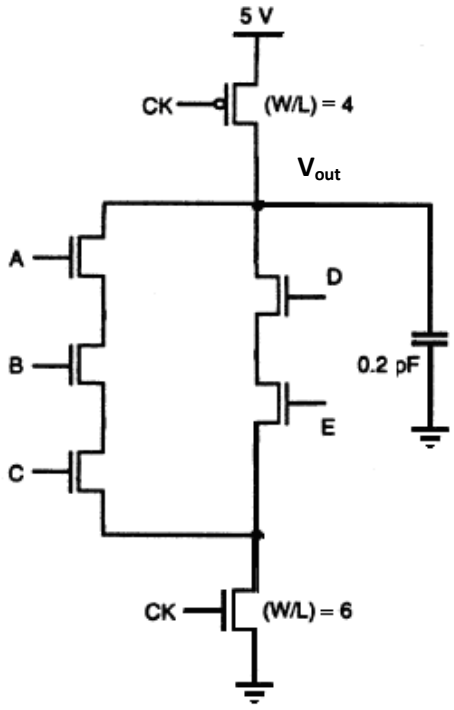

Figure 5(b) : A Dynamic Logic Circuit
Rajah 5(b) : Litar logik dinamik

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(b) If signals as shown in Figure 5(c) are applied to the circuit [Figure 5(b)], draw the expected V_{out} waveform.

Sekiranya isyarat seperti dalam Rajah 5(c) disalurkan kepada litar [Rajah 5(b)], lukiskan gelombang $V_{out.}$

(10 marks/markah)

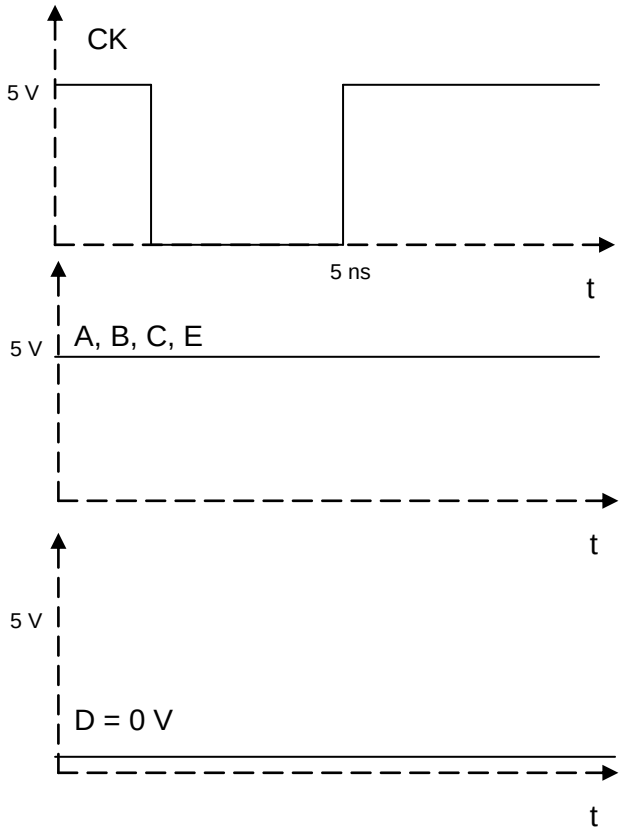

Figure. 5(c) : CK, A, B, C, D and E waveforms.
Rajah 5(c) : Gelombang CK, A, B, C, D dan E

(c) The parameters for circuit in Figure 5(b) are as follows.
V_{ton} = 1 V, V_{top} = -1 V, k'_n = 50 μA/V^2 , k'_P = 25 μA/V^2 and W/L ratios for each NMOS device is 9. With initial V_{out} = 0 V and input signals as shown in Figure 5(c), calculate time required for V_{out} (during charge up) to reach 50 % of V_{DD} (5 V).

Parameter untuk litar dalam Rajah 5(b) adalah seperti berikut.
V_{ton} = 1 V, V_{top} = -1 V, k'_n = 50 μA/V^2 , k'_P = 25 μA/V^2 dan nisbah W/L untuk setiap NMOS ialah 9. Pada mulanya V_{out} = 0 V dan isyarat masukan adalah seperti dalam Rajah 5(c), kira masa diperlukan untuk V_{out} (semasa pengecasan) sampai 50 % daripada V_{DD} (5 V).

(60 marks/markah)

6. (a) What is volatile memory and non-volatile memory?
Apakah ingatan meruap dan ingatan tak meruap? (25 marks/markah)

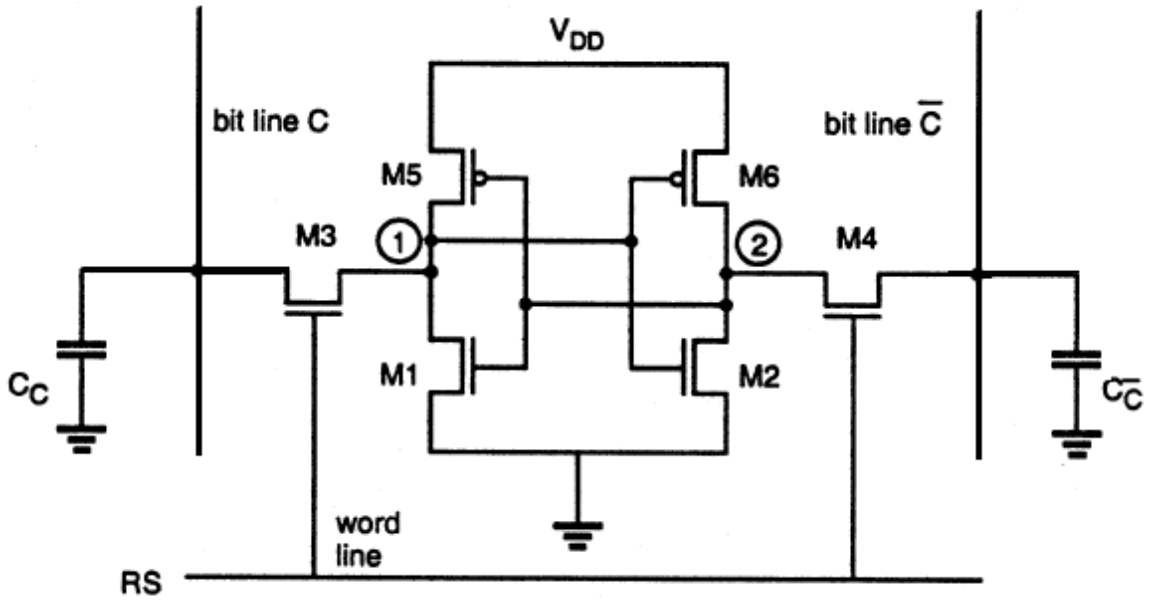

Figure 6 : CMOS SRAM
Rajah 6 : SRAM CMOS

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(b) The circuit in Figure 6 has parameters as follows.
Parameter untuk litar dalam Rajah 6 adalah seperti berikut.

V_{ton} = 0.7 V, V_{top} = -0.7 V, k'_n = 20 μA/V^2 , k'_P = 10 μA/V^2 , γ = 0.4 $V^{1/2}$ and $|2\phi_F|$ = 0.6 V.

If W/L ratios for M1 and M2 is 1, M3 and M4 is 2/4.
Assuming that the storage bit is 0, state of cell can be changed for $V_C \leq$ 0.5 V and M1 initially OFF

Sekiranya nisbah W/L untuk M1, M2 ialah 1 dan M3, M4 ialah 2/4. Andaikan bit simpanan ialah 0, keadaan sel berubah apabila $V_C \leq$ 0.5 V$\leq$ dan pada mulanya M1 'OFF'.

(i) Confirm that M5 is saturated
Pastikan M5 berada dalam tepu. (15 marks/markah)

(ii) Confirm that M3 is in linear region.
Pastikan M3 berada dalam kawasan lelurus. (15 marks/markah)

(iii) Determine W/L for M5 and M6.
Tentukan nilai W/L untuk M5 dan M6. (45 marks/markah)

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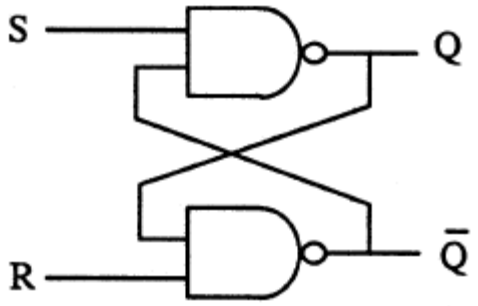
Ans:

4

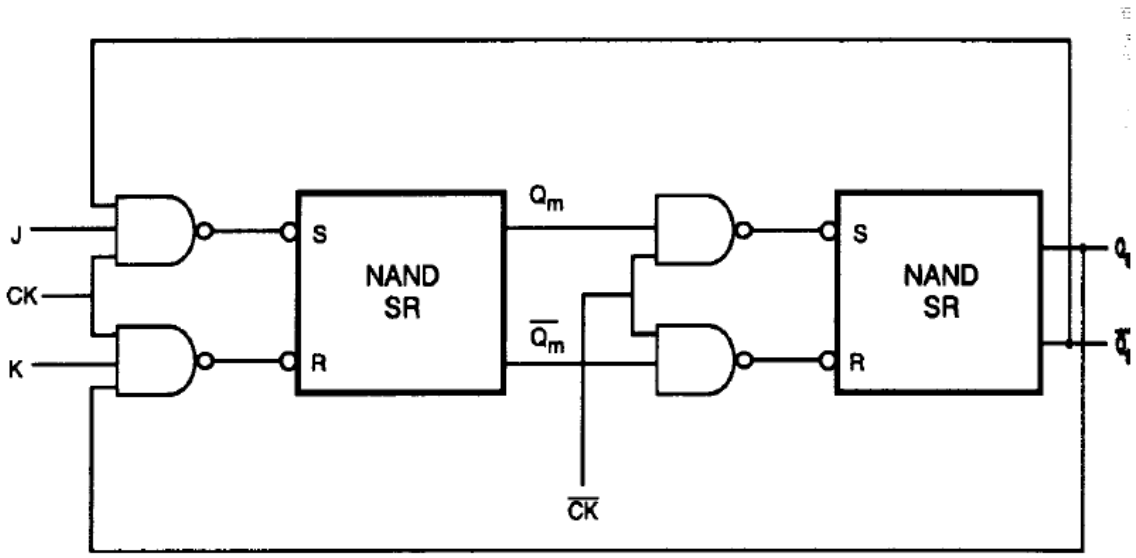
(a). Its output is determined by the current inputs as well as previously applied input variables.

(b).



(c).

Criteria of the answer should be CMOS based, example answer should from gate level….



5 (a).

(a) $F = \overline{A(B+C)+D}$

(b) V_{OL} maximum occurs when A=1, D=0 and either (but not both) B=1 or C=1. Under these conditions, the circuit may be simplified as a depletion load inverter with the equivalent driver W/L given below.

$$\left.\frac{L}{W}\right|_{equiv} = \frac{4}{8} + \frac{4}{4} = \frac{3}{2}$$

$$\therefore \left.\frac{W}{L}\right|_{equiv} = \frac{2}{3}$$

When V_{OL} = 0.3 V, V_{IN} = 5V, the load in saturated and driver in linear region.

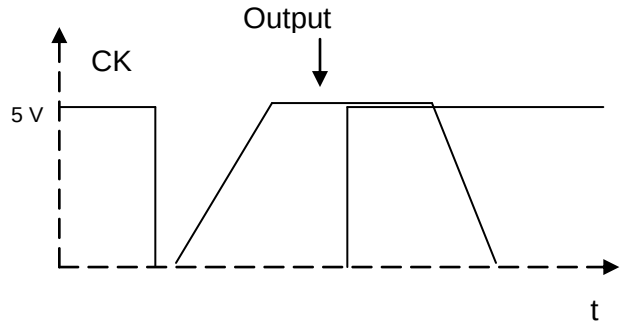
$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}\left(V_{GS,load} - V_{T,load}\right)^2 = k'\frac{2}{3}\left[(V_{IN} - V_{T,driver})V_{out} - \frac{1}{2}V_{out}^{\,2}\right]$$

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}(0+3)^2 = k'\frac{2}{3}\left[(5-1)\times 0.3 - \frac{1}{2}\times 0.3^2\right]$$

$(W/L)_{load} = 0.171$

Therefore $(W/L)_{load} \leq 0.171$ for $V_{OL} \leq 0.3$ V.

(b).



(c).

Assume the time it takes for the transistor to stay in saturation region is τ_s then,

$$\tau_s = \frac{C_L \cdot \Delta V}{I_{P,SAT}} = \frac{C_L \cdot \Delta V}{\frac{1}{2} k'_p \left(\frac{W}{L}\right)_p (V_{GS} - V_T)^2} = \frac{0.2pF \cdot 1}{\frac{1}{2} \cdot 25\mu A \cdot 4 \cdot (-5+1)^2} = 0.25ns$$

The time it takes from saturation region to 50% V_{DD} is

$$\tau_{50\%} - \tau_s = \frac{C_L \cdot \Delta V}{I_{AVG}} = \frac{C_L \cdot \Delta V}{\frac{1}{2}\left(I_{p,SAT} + I_{p,LIN}\right)}$$

$$= \frac{0.2pF \cdot (4 - 2.5)}{\frac{1}{2} \cdot \left(0.8 + 4 \times 25\left(-(-5+1) \times 2.5 - \frac{1}{2} \times 2.5^2\right) \times 10^{-3}\right) mA} = 0.4ns$$

$$\tau_{50\%} = 0.65ns$$

6

(a). Volatile memory is a device in which the stored information is lost when the power supply is switched off. Non volatile memory retains the information when the power ceases.

(b).

(i) For M5 ; VGS = 0-5 = -5 V, VDS = 0.7-5 = -4.3 V, So it is confirmed that M5 is in saturated.

(ii) M3: VGS = 5 -0.5 = 4.5 V, VDS = 0.7-0.5 = 0.2, So it is confirmed that M3 is in linear region.

(iii) a. Calculate real Vt= 0.81 V.

b. Equate current of M5 and M3.

c. W/L= 0.078.