UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2012/2013 Academic Session

June 2013

EEE 344 – System VLSI
[Sistem VLSI]

Duration : 3 hours
[Masa : 3 Jam]

Please check that this examination paper consists of **ELEVEN (11)** pages printed material and **ONE (1)** page of Appendix before you begin the examination.

*[Sila pastikan bahawa kertas peperiksaan ini mengandungi **SEBELAS (11)** mukasurat bercetak beserta Lampiran **SATU (1)** muka surat bercetak sebelum anda memulakan peperiksaan ini.]*

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

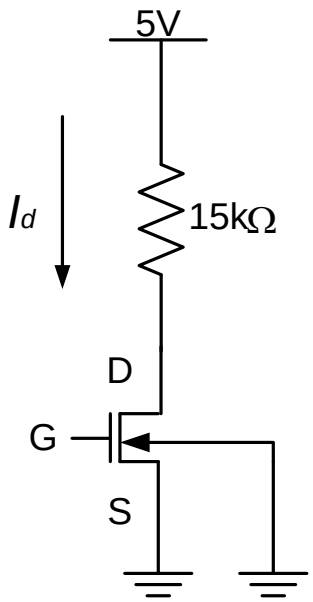
[***Arahan:*** *Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **LIMA (5)** soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. (a) Diberi sebuah litar seperti dalam Rajah 1(a). Sekiranya $V_{T0,n} = 0.6V, \mu_n C_{ox} = 200\mu A/V^2, W/L = 3$. Abaikan kesan perubahan panjang saluran dan substrate bias $(\lambda = 0, \gamma = 0)$.

Consider a circuit shown in Figure 1(a). Given, $V_{T0,n} = 0.6V, \mu_n C_{ox} = 200\mu A/V^2, W/L = 3$ *Neglect the channel-length modulation and substrate bias effect* $(\lambda = 0, \gamma = 0)$



Rajah 1(a)
Figure 1(a)

(i) Sekiranya $V_{GS} = 1.5V$, tentukan nilai V_{DS} dan I_d

If $V_{GS} = 1.5V$ *, determine the values of* V_{DS} *and* I_d

(20 markah/*marks*)

(ii) Sekiranya $V_{GS} = 1.8V$, tentukan nilai V_{DS} dan I_d

If $V_{GS} = 1.8V$, determine the values of V_{DS} and I_d

(30 markah/*marks*)

(b) Diberi sebuah litar seperti dalam Rajah 1(b). Voltan yang dinyatakan adalah berasaskan kepada bumi. Sekiranya,

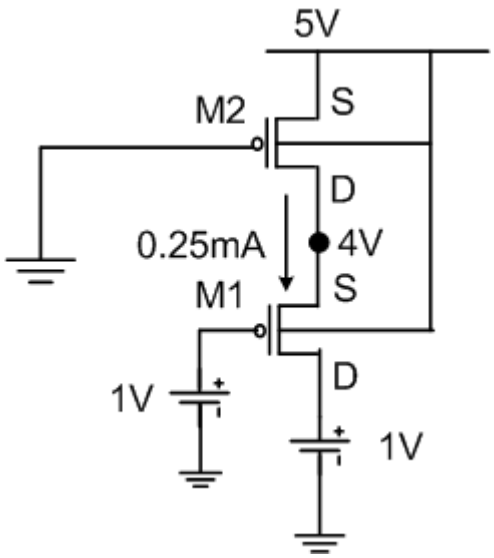
$$V_{T0,p} = -0.5V, \mu_p C_{ox} = 3.4 \times 10^{-5} A/V^2, \phi_F = 0.77V, \gamma = -0.69V^{1/2}$$

Abaikan kesan perubahan panjang saluran $(\lambda = 0)$.

Consider a circuit shown in Figure 1(b). The shown voltages are with respect to the ground. Given,

$$V_{T0,p} = -0.5V, \mu_p C_{ox} = 3.4 \times 10^{-5} A/V^2, \phi_F = 0.77V, \gamma = -0.69V^{1/2}$$

Neglect the channel-length modulation effect $(\lambda = 0)$.



Rajah 1(b)
Figure 1(b)

(i) Tentukan nilai voltan ambang bagi transistor M1 dan M2
Determine the threshold voltages for transistors M1 and M2

(10 markah/*marks*)

(ii) Tentukan mod operasi bagi transistor M2 dan kira nilai (W/L) nya.

Determine the operation region of transistor M2 and calculate the value of its (W/L).

(20 markah/*marks*)

(iii) Tentukan mod operasi bagi transistor M1 dan kira nilai (W/L) nya.

Determine the operation region of transistor M1 and calculate the value of its (W/L).

(20 markah/*marks*)

2. Rekabentuk sebuah penyongsang CMOS dengan menentukan lebar saluran bagi transistor nMOS dan pMOS supaya $V_{th} = 2.2V$ dan $\tau_r = 5ns$. Anggap

$$V_{DD} = 5V, V_{T0,n} = 0.8V, \mu_n C_{ox} = 50\mu A/V^2, V_{T0,p} = -1V, \mu_p C_{ox} = 20\mu A/V^2, L_n = L_p = 1\mu m, C_L = 2pF$$

Anda boleh menggunakan kaedah purata arus untuk τ_r dan anggap isyarat masukan adalah ideal (tanpa masa naik dan turun).

Abaikan kesan perubahan panjang saluran $(\lambda = 0)$.

Design a CMOS inverter by determining the channel width of the nMOS and pMOS transistors such that $V_{th} = 2.2V$ *and* $\tau_r = 5ns$. *Assume that :-*

$V_{DD} = 5V, V_{T0,n} = 0.8V, \mu_n C_{ox} = 50\mu A/V^2, V_{T0,p} = -1V, \mu_p C_{ox} = 20\mu A/V^2, L_n = L_p = 1\mu m, C_L = 2pF$

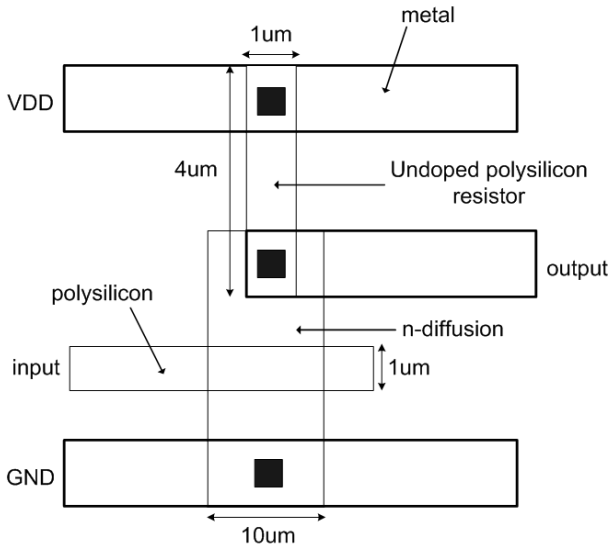
You may use the average current method for the τ_r *and assume that the input signal is an ideal step pulse (no rise and fall times).*

Neglect the channel-length modulation effect $(\lambda = 0)$ *for both transistors.*

(100 markah/*marks*)

3. Diberi susunatur seperti di Rajah 3. Ianya adalah sebuah litar penyongsang. Abaikan kesan perubahan panjang saluran dan substrate bias $(\lambda = 0, \gamma = 0)$.

Consider the layout shown in Figure 3. It is an inverter. Neglect the channel length modulation effect and substrate bias effect $(\lambda = 0, \gamma = 0)$.



Undoped polysilicon sheet resistivity = $2.5k\Omega/square$

Rajah 3
Figure 3

(a) Lukis litar skematik transistor untuk susunatur di atas.

Draw the transistor level schematic that represents the layout

(5 markah/*marks*)

(b) Terbitkan formula untuk mengira voltan kritikal $V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_{th}$

Derive the formula to calculate the critical voltages $V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_{th}$

(55 markah/*marks*)

(c) Sekiranya,

$$V_{DD} = 5V, V_{TO,n} = 1V, V_{TO,p} = -0.7V, \mu_n C_{ox} = 25\mu A/V^2, \mu_p C_{ox} = 5\mu A/V^2$$

dan litar tersebut adalah bersambung dengan $C_L = 1pF$. Anggap isyarat masukan adalah ideal (tanpa masa naik dan turun). Kira τ_{PLH} dengan menggunakan kaedah persamaan pembezaan.

Given

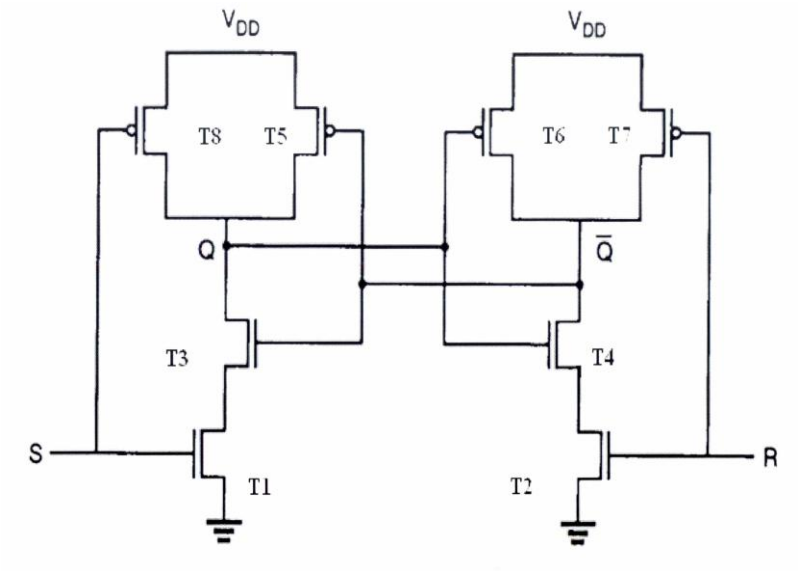
$$V_{DD} = 5V, V_{TO,n} = 1V, V_{TO,p} = -0.7V, \mu_n C_{ox} = 25\mu A/V^2, \mu_p C_{ox} = 5\mu A/V^2$$

and the circuit is connected to $C_L = 1pF$. *Assume that the input signal is an ideal step pulse (no rise and fall times). Calculate* τ_{PLH} *using the differential equation method.*

(40 markah/*marks*)

4. (a) Apakah definisi litar berjujukan? Sila rujuk Rajah 4(a).

What is definition of sequential circuit? Please refer Figure 4(a).

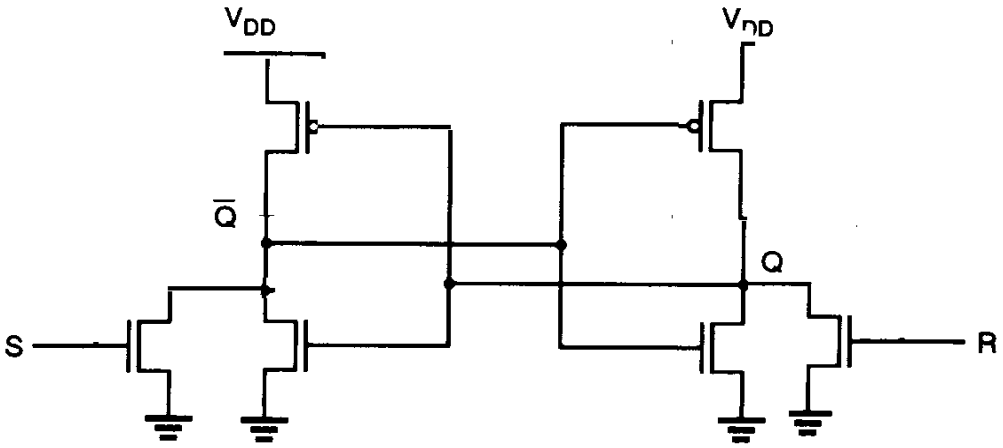


Rajah 4(a)
Figure 4(a)

(25 markah/*marks*)

(b) Berdasarkan Gambarajah 4(a). Sekiranya S = 0 V dan R = 3 V. Apa nilai voltan pada Q?. Apa nilai yang sesuai untuk V_T.? Terangkan.

Based on Figure 4(a). If S = 0 V and R = 3 V (VDD). What is the voltage at Q? What is the suitable value of V_T (Threshold voltage)? Explain.



Rajah 4(b)
Figure 4(b)

(35 markah/*marks*)

(c) Diberikan NMOS (Untuk S dan R) memiliki W/L yang sama Rajah 4(b). Penyongsang: W/L NMOS ialah 2 dan W/L PMOS ialah 5.

k'n= 2k'p and k'p= 20 μA/V^2 . Vtn= |Vtp|=1 V, V_{DD}=5 V.

Given NMOS (for S and R) have same W/L. Inverters: NMOS W/L is 2 and PMOS W/L is 5.

k'n= 2k'p and k'p= 20 μA/V^2 . Vtn= |Vtp|=1 V, V_{DD}=5 V.

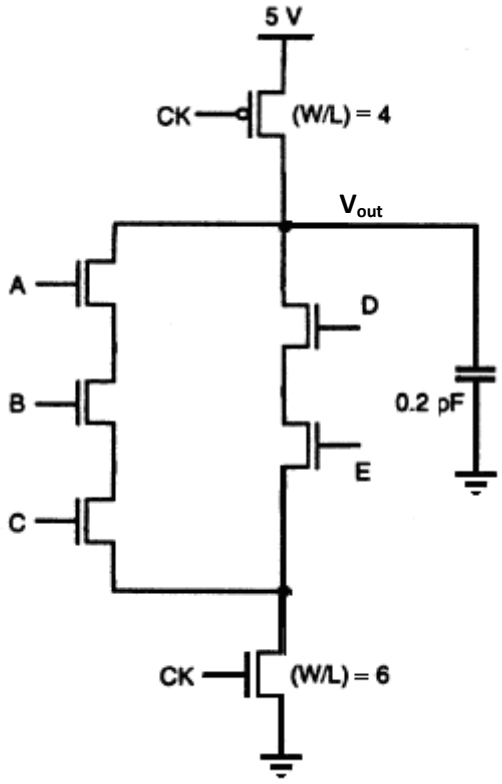
Apakah saiz minimum bagi NMOS untuk S atau R?

What is the minimum size of NMOS for S or R?

(40 markah/*marks*)

5. (a) Berdasarkan Rajah 5(a), apakah fungsi Boolean untuk V_{out}?

Based on Figure 5(a), what is the Boolean function of V_{out}?



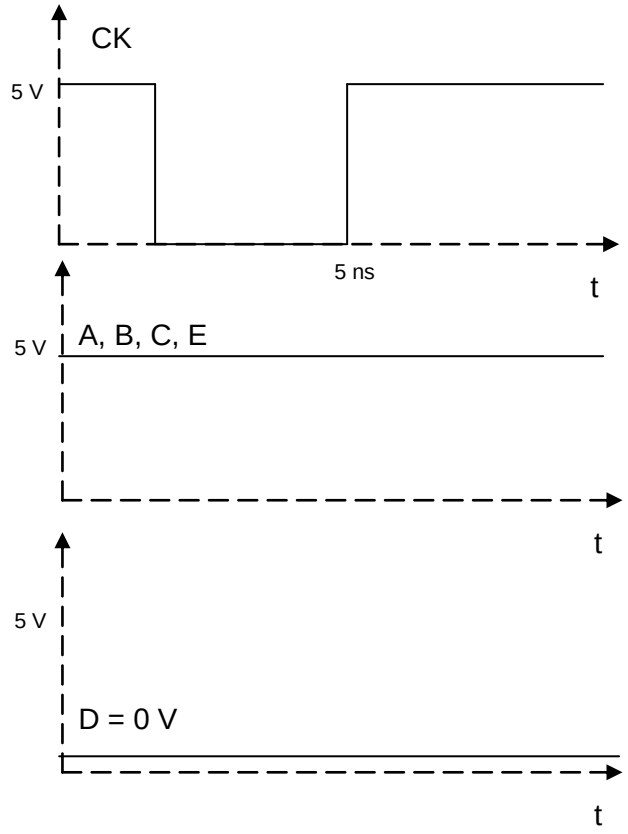
Rajah 5(a) Litar logik dinamik

Figure. 5(a) A Dynamic Logic Circuit

(20 markah/*marks*)

(b) Sekiranya isyarat seperti dalam Rajah 5(b) disalurkan kepada litar Rajah 5(a), lukiskan gelombang $V_{out.}$

If signals as shown in Figure 5(b) are applied to the circuit (Figure 5(a), draw the expected V_{out} waveform.



Rajah 5(b) : Gelombang CK, A, B, C, D dan E
Figure 5(b) : CK, A, B, C, D and E waveforms.

(20 markah/*marks*)

(c) Parameter untuk litar dalam Rajah 5(a) adalah seperti berikut :

V_{ton} = 1 V, V_{top} = -1 V, k'_n = 50 μA/V^2 , k'_P = 25 μA/V^2 dan nisbah W/L untuk setiap NMOS ialah 9. Pada mulanya V_{out} = 0 V dan isyarat masukan adalah seperti dalam rajah. 7, kira masa diperlukan untuk V_{out} (semasa pengecasan) sampai 50 % daripada V_{DD} (5 V).

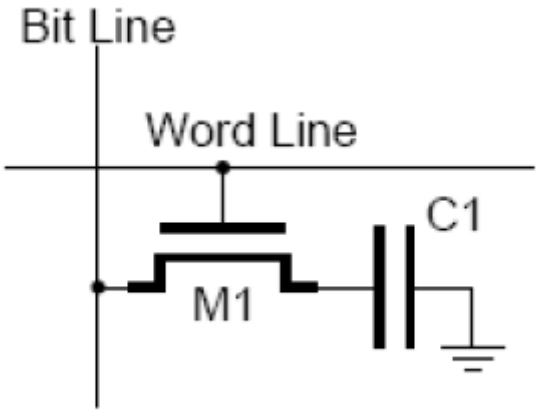
The parameters for circuit in Figure 5(a) are as follows :

V_{ton} = 1 V, V_{top} = -1 V, k'_n = 50 μA/V^2 , k'_P = 25 μA/V^2 and W/L ratios for each NMOS device is 9. With initial V_{out} = 0 V and input signals as shown in Figure 5(b), calculate time required for V_{out} (during charge up) to reach 50 % of V_{DD} (5 V).

(60 markah/*marks*)

6. (a) Berikan terbitan masa untuk nyahcas pemuat C1 kepada separuh voltan asal.(voltan simpanan).

Give the formula of the time to discharge the capacitor C1 to the half of the initial voltage (eg. stored voltage).



Rajah 6(a)
Figure 6(a)

(35 markah/*marks*)

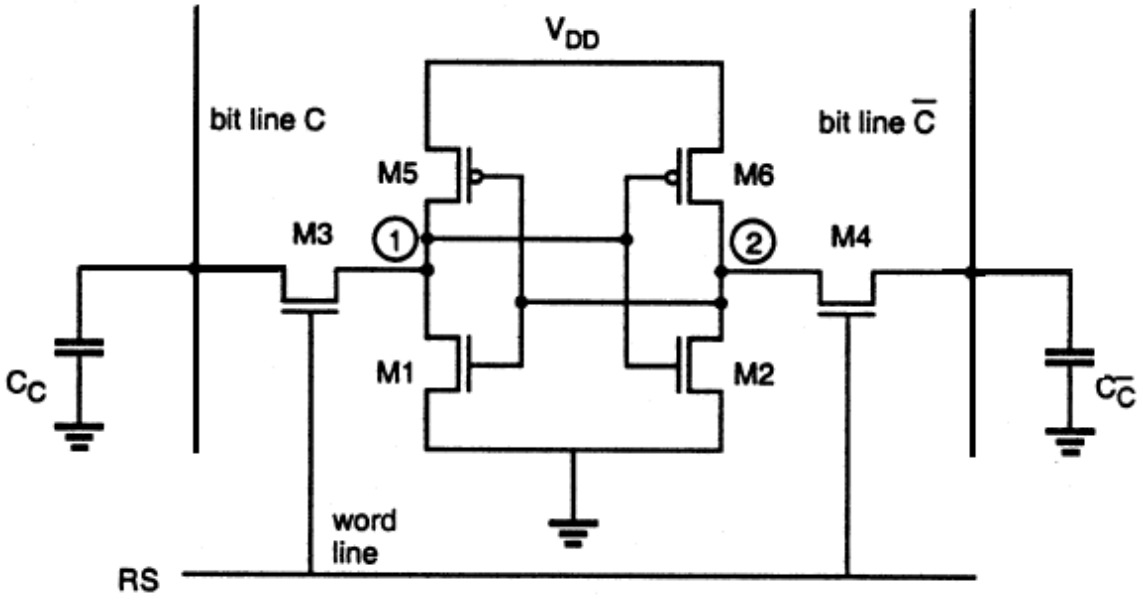
(b) Andaikan voltan bercas penuh bagi pemuat simpanan ialah 2.5 V, nilai C1 ialah 20 fF dan arus bocor bagi transistor ialah 40 pA, kirakan masa untuk nyahcas pemuat C1 kepada separuh voltan.

Assuming that the voltage on the fully charged storage capacitor is V = 2.5 V, the capacitor C1 is 20 fF and that the transistor leakage current is I = 40 pA, calculate the time to discharge the capacitor C1 to the half of the initial voltage.

(25 markah/*marks*)

(c) Gambarajah 6(c) ialah SRAM CMOS, terangkan operasi bagi baca dan tulis.

Figure 6(c) is a typical CMOS SRAM, explain the operation of read and write.



Rajah 6(c) : SRAM CMOS
Figure 6(c) : CMOS SRAM

(40 markah/*marks*)

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