UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013 & January 2014

EEE 554/4 – Digital Integrated Circuit Design

Duration : 3 hours

Please check that this examination paper consists of **SEVEN (7)** pages printed material before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) (i) What are the advantages of standard cell based approach as compared with full custom based approach?

(8 marks)

(ii) Explain three advantages of HDL compared to traditional schematic-based design?

(12 marks)

(b) Find a test pattern that can detect s-a-1 at net u of the following circuit

```
module circuit1(f, a, b, c, d);
  output f;
  input a, b, c, d;

  and (p, a, b);
  not (r, c);
  and (u, r, d);
  or (v, p, c);
  not (t, p);
  or (w, t, u);
  and (f, v, w);

endmodule
```

(25 marks)

(c) Design a digital circuit that output the minimum number of four 8-bit numbers by instantiating the Verilog modules **comp** and **mux**. You need to develop also the test bench to verify the designed circuit.

```
module comp(out, in0, in1);
  output out;
  input [7:0] in0, in1;

  assign out = (in0 < in1)? 1'b1 : 1'b0;

endmodule

module mux(out, in0, in1, sel);
  output [7:0] out;
  input [7:0] in0, in1; input sel;

  assign out = sel? in0 : in1;

endmodule
```

(55 marks)

2. Design a digital circuit based on following specification using Verilog HDL. Apart from the Verilog codes, you also have to develop the block diagram (consists of datapath and control units) and the ASMD chart.
The inputs are as follows :-
(i) Four values (T0, T1, T2, T3) of temperature readings from four different sensors. Each of the value is 8-bit.
(ii) An 8-bit WT indicating the user-specified temperature value at which the warning signal should be asserted.
(iii) A 1-bit CLR that will clear the warning signal
(iv) A 1-bit START that will start the operation
(v) A 1-bit RESET (asynchronous, active low) that will reset the circuit
(vi) A 1-bit CLK as the clock

The output is a warning signal 1-bit W that will be asserted in the next clock cycle when the average temperature over the four-readings exceeds the user-specified temperature value. The warning signal W should remain high until the CLR input is asserted. If the average temperature does not exceed the user-specified temperature value, the operation cycle repeats where the circuit will process the next four readings. Assume that the temperature readings are available at every clock cycle as long as the START signal is asserted. You are not allowed to use the arithmetic operators (*, /, *, **, %).

(100 marks)

3. Design a digital circuit based on following specification using Verilog HDL. Apart from the Verilog codes, you also have to develop the block diagram (consists of datapath and control units) and the ASMD chart.
The inputs are as follows :-

(i) An 8-bit DATA indicating the input value
(ii) A 1-bit START that will start the operation
(iii) A 1-bit RESET (asynchronous, active low) that will reset the circuit
(iv) A 1-bit CLK as the clock

The output indicates the maximum difference between any DATA of every four input values. Assume that the DATA is available at every two clock cycles after the START signal is asserted.

For example, the sequence of the DATA and the OUT are as follows :
2nd clock cycle : DATA = 8'd8
4th clock cycle : DATA = 8'd19
6th clock cycle : DATA = 8'd10
8th clock cycle : DATA = 8'd5
9th clock cycle : OUT = 19 - 5 = 14
10th clock cycle : DATA = 8'd26
12th clock cycle : DATA = 8'd8
14th clock cycle : DATA = 8'd20
16th clock cycle : DATA = 8'd1
17th clock cycle : OUT = 26 - 1 = 25

(100 marks)

…4/-

4. (a) IR drop and congestion are some of the problems faced during placement. Describe the methods used to overcome these problems.

(20 marks)

(b) Figure 4(b) shows a problematic segmented floorplan that may lead to long interconnections between the bottom and top of the die. Design the placement of this floorplan so that the wire length can be reduced.

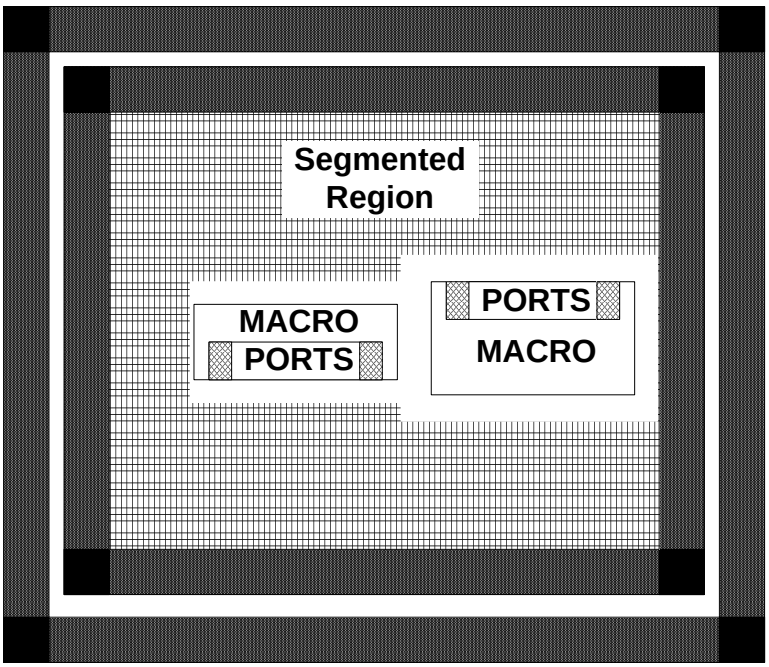


Figure 4(b) : Segmented floorplan.

(20 marks)

(c) Using Figure 4 as an example, describe the term 'trap pocket' and show methods in mitigating this problem.

(30 marks)

(d) When floorplanning a design that contains regions that will be shut down, we need to consider the placement of switch cells and the routing of the steep control signals. The two most common styles are Ring style and Grid style. Using the switch layout as an example, describe the difference between the two. State the advantages and disadvantages of both styles.

(30 marks)

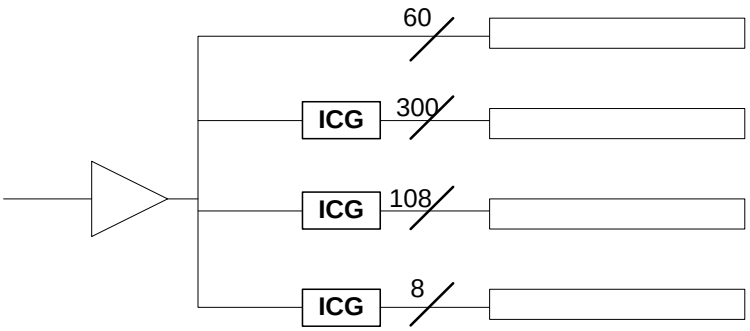
5. Define the term clock gating. Describe one of the methods to insert clock gating in a circuit.

(20 marks)

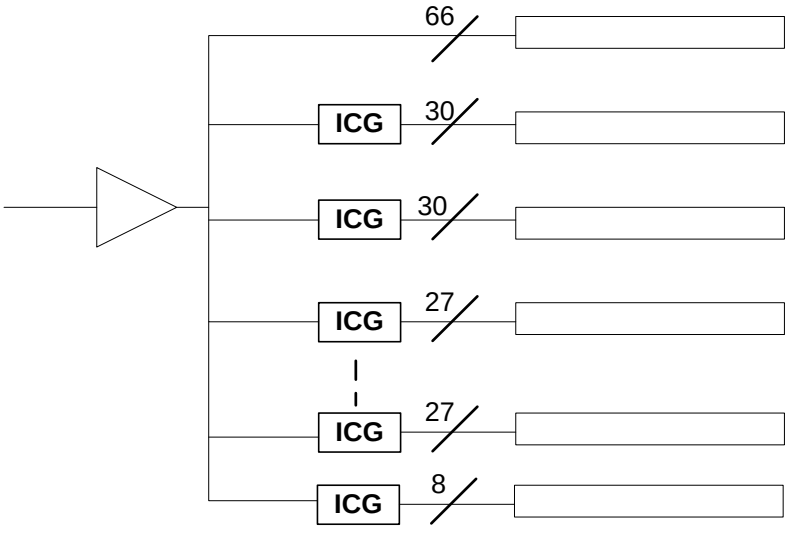
(a) What are the rules for auto insertion of ICG cells? State the command used for clock gating in Synopsys.

(20 marks)

(b) Consider the figures below. Discuss the difference between the two figures in terms of fan-out and skew.



(a)



(b)

Figure 5.1: Auto insertion of ICG cells: fan-out.

(30 marks)

(c) Figure 5.2 shows a clock tree synthesis (CTS) incorporated circuit. Discuss whether this circuit can be further optimized. State the implications of these methods.

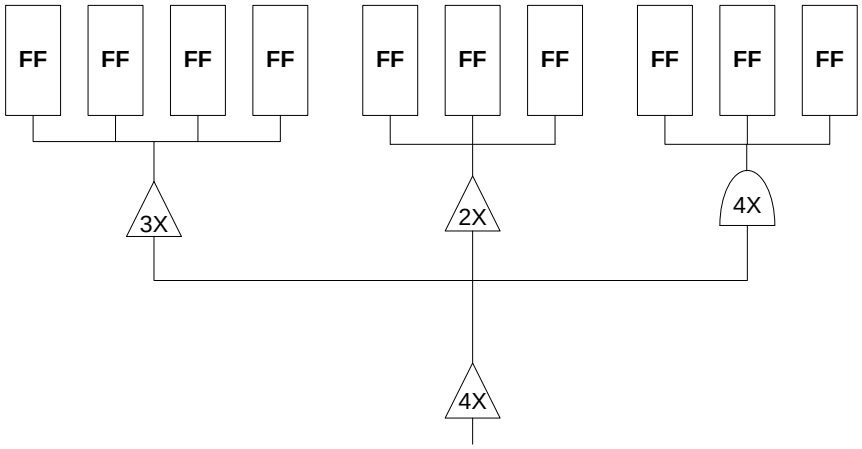


Figure 5.2: CTS incorporated circuit.

(30 marks)

6. Define the terms Design Rule Check (DRC) and Layout versus Schematic (LVS).

(20 marks)

(a) Consider the figure below, which is used to describe the antenna effect. In your own words, describe the meaning of antenna effect.

(10 marks)

(b) Based on antenna rules, which of the two configurations need to be avoided. How would you overcome this antenna problem? (Illustrate using the figure provided).

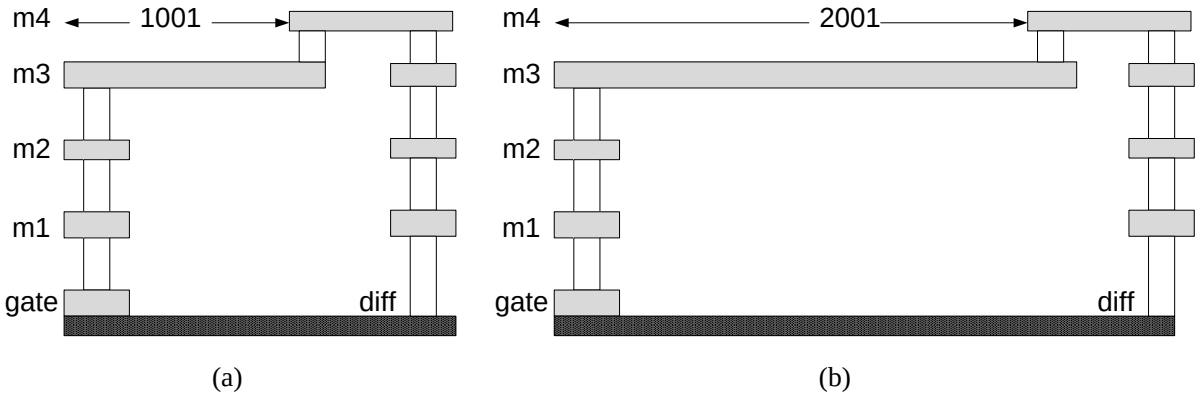


Figure 6.1: An illustration of antenna effect.

(35 marks)

(c) Consider Figure 6.2, what is the combination of thicknesses and widths for 6 layers interconnection (M1-M6) which gives the worst setup/hold. Can this information be obtained in this case? Describe the statistical tool that can provide this information.

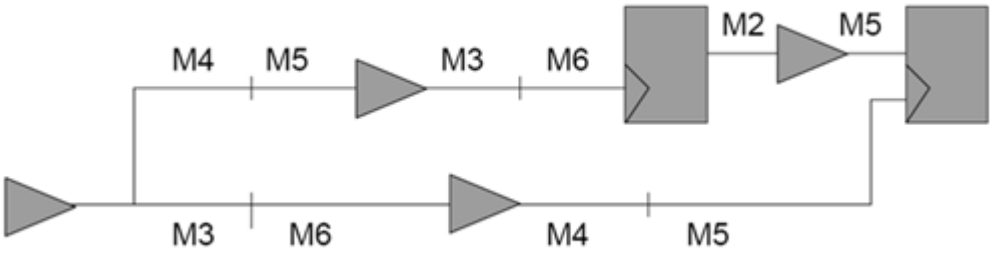


Figure 6.2 : Worst case timing for 6 layers interconnection.

(35 marks)

oooooOoooo