UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013 & January 2014

EEE 553/4 – Semiconductor Devices and Solid State Technology

Duration : 3 hours

Please check that this examination paper consists of **SIX (6)** pages printed material and **ONE (1)** page of Appendix before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) What is threshold voltage and its relationship with V_{sb} and the corresponding capacitance?

(2 marks)

(b) Drain current of MOS transistor can be derived from $I_{ds} = WQ_{inv}v$ which is based on simple charge sheet model.

(i) Derive the basic drain current equation, $I_{ds} = \frac{W}{L} C_{oxe}\mu_{es}\left(V_{gs} - V_t - \frac{m}{2}V_{ds}\right)V_{ds}$

Explain *m.*

(4 marks)

(c) Derive completely the V_{dsat} based on the above equation.

(4 marks)

(d) Explain the definition of flat band energy diagram. Draw the flat band energy diagram for n-MOSFET. Assume the gate is metal. (shows all the work functions and potentials, Fermi level, intrinsic Fermi level, vacuum level in this diagram)

(8 marks)

(e) Explain the strong inversion with energy band diagram for n-MOSFET

(2 marks)

2. (a) Equation 2.1 shows the velocity saturation is factored into the basic drain current equation. Equation 2.2 includes the velocity saturation.

$$I_d = \frac{1}{1+\frac{V_{ds}}{E_{sat}L}} \frac{WC_{oxe}\mu_{eff}}{L}\left(V_g - V_t - \frac{V_{ds}}{2}\right)V_{ds} \quad \text{.....equation} \qquad (2\text{-}1)$$

$$I_d \le WQ_{inv}v_{sat} \quad \text{..... equation} \qquad (2\text{-}2)$$

If $V_{sat} = \frac{E_{sat}\mu_{eff}}{2}$, derive completely the I_{dsat} based on equation (2-1) and equation (2-2).

(12 marks)

(b) Explain the condition if $E_{sat}L << V_g - V_t$

(2 marks)

(c) Explain DIBL by using energy band diagram.

(6 marks)

3. (a) Explain the direct bandgap and indirect bandgap with the energy level band diagram. Give one example of electronic devices application for each type

(2 marks)

(b) Derive the charge density Q_{inv} for p-type silicon at surface at inversion layer. (Assume the V_{FB}, Ψ_B, Ψ_S and C_{ox} are voltage potential, bulk potential, surface potential and oxide capacitance)

(8 marks)

(c) Design the semiconductor doping concentration to yield a specified threshold voltage. Consider aluminium-silicon dioxide-silicon MOS structure. The silicon n type, the oxide thickness is tox = 650 Å, and the trapped charge density $Q'_{ss} = 10^{10}$ cm^{-2}. Determine the doping concentration such that V_{TP} = -1.0 V. (Refer to appendix 1)

(10 marks)

4. (a) Refer to Figure 4(a), explain the following terms :

(i) Interface trapped charges Q_{it}
(ii) Fixed oxide charges Q_f
(iii) Oxide trapped hot- electron Q_{ot}
(iv) Mobile ionic charges Q_m

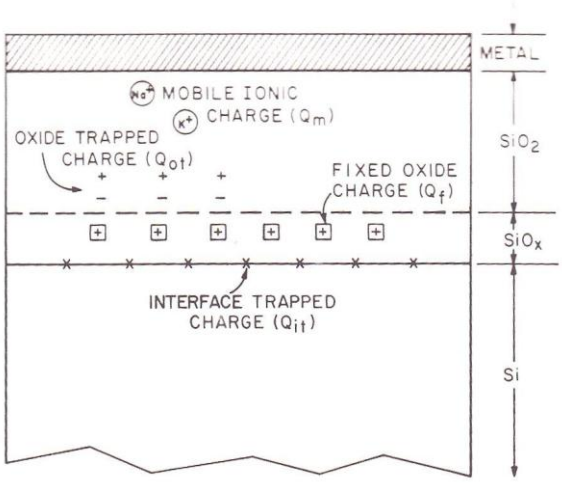

Figure 4(a)

(8 marks)

(b) Tamm, Shockley and others have studied the interface trapped charge Q_{it} and have shown that Q_{it} exits within the forbidden gap due to the interruption of the periodic lattice structure at the surface of a crystal. Thus, when voltage is applied, the interface-traps levels move up or down with the valence and conductance bands while the Fermi levels remains fixed. A change of charge in the interface trap occurs when it crosses the Fermi level. This change contributes to the MOS capacitance and alters the MOS ideal curve

(i) Sketch the equivalent circuit including interface-trap effect

(6 marks)

(ii) Sketch the capacitance–voltage due to interface trapped charges and explain the graph

(6 marks)

5. (a) Refer to Figure 5(a), explain what do you understand about this modeling image in CMOS fabrication technique. In your explanation, you need to relate with LOCOS process (Local Oxidation of Silicon)

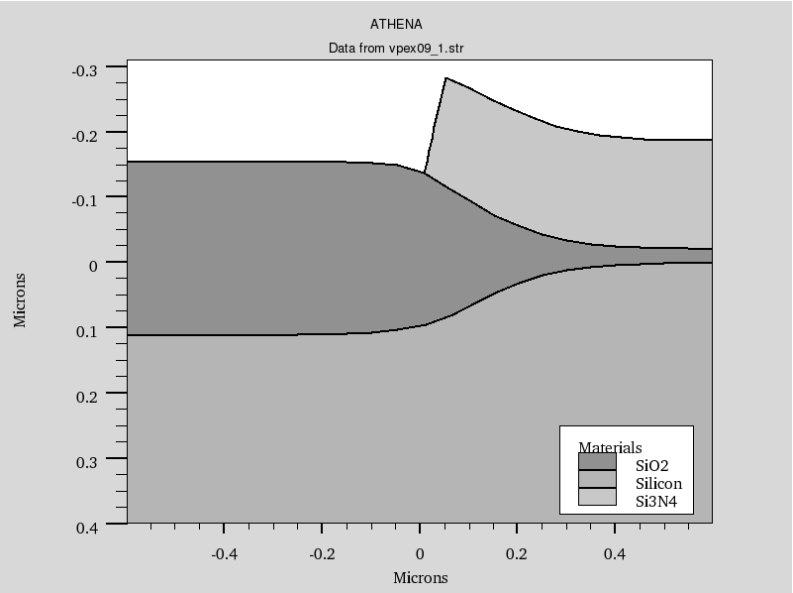

Figure 5(a)

(4 marks)

(b) Refer to Figure 5(b), explain the function of Ar gas for sputtering process and how this gas effect the deposition of target material on the silicon wafer.

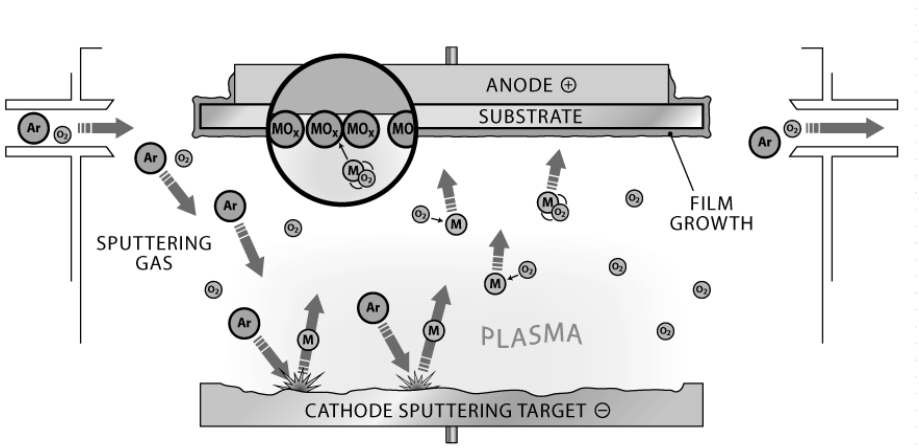

Figure 5(b)

(4 marks)

(c) Prove that the scaling electric field and current are 1 and 1/k, respectively.

(2 marks)

(d) A 28-pin dual in-line package (DIP) failed electrical testing after 500 temperature cycles of condition C (-65 ^{o}C to 150 ^{o}C). The DIP was decapped and the die was inspected. A result of Figure 5(c) is obtained

(i) What is the suitable measurement used to identify the problem.

(4 marks)

(ii) Describe briefly, the basic operation of the tools used in question d(i).

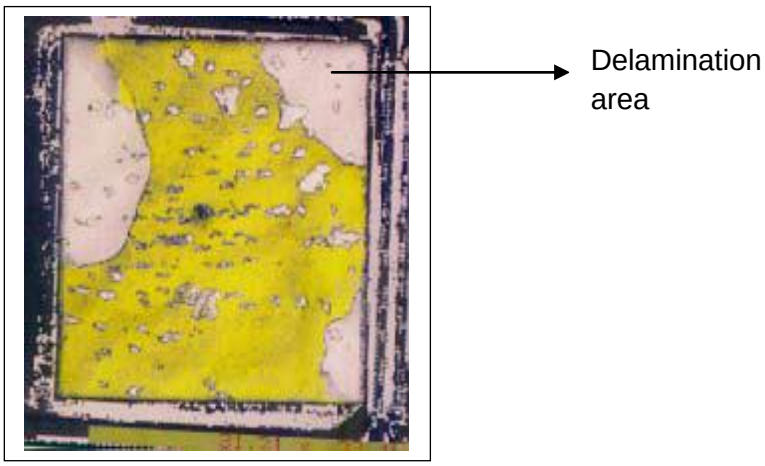

Figure 5(d)

(6 marks)

6. (a) A wire bond BGA (ball-grid array) device failed the electrical continuity test for open contacts after it was subjected to 500 temperature cycles of -55 ^{o}C to 125 ^{o}C. The visual inspection after decapping revealed multiple gold ball bonds lifted from the aluminum bond metal pad.

(i) Draw and label a basic packaging structure of wire bond BGA.

(6 marks)

(ii) Briefly explain the reasons you choose the techniques to identify the problem in Figure 6.

(6 marks)

(iii) Suggests what is the possible cause of the lifted ball bonds.

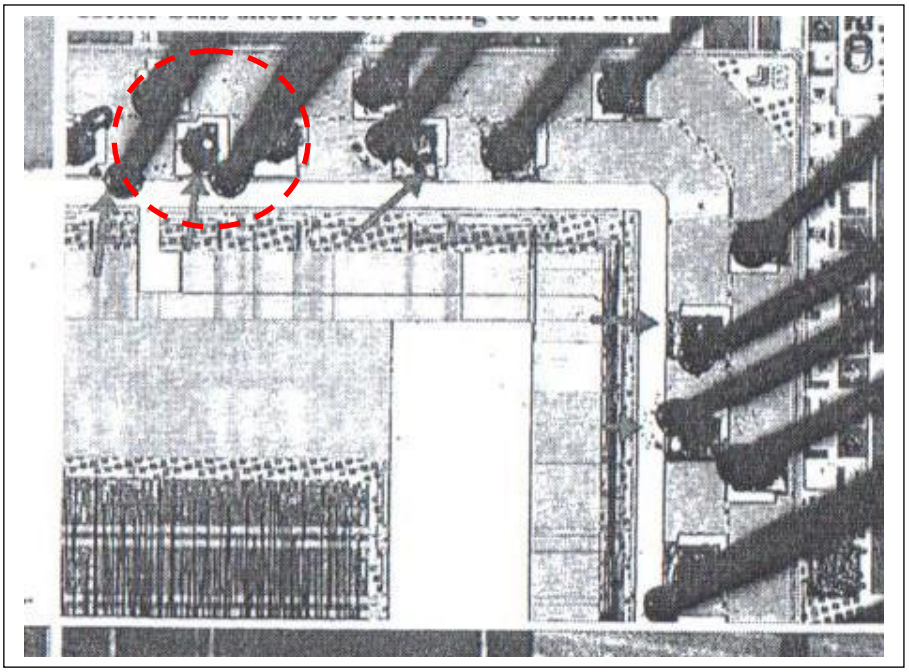

Figure 6

(8 marks)

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