UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013 & January 2014

EEE 552/4 – Signal Integrity for High Speed Digital Design

Duration : 3 hours

Please check that this examination paper consists of **TEN (10)** pages printed material and **THREE (3)** pages of Appendix before you begin the examination.

Instructions: This question paper consists **SEVEN (7)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. For the 2 input NAND gate circuit given in Figure 1, you will be estimating the delay of the device. Following are the assumptions – Both the inputs of the device (A and B) are switching from low to high. Also, assume the source of NMOS with input A and drain of NMOS with input B are merged. The NAND gate is driving 3 similar NAND gates.

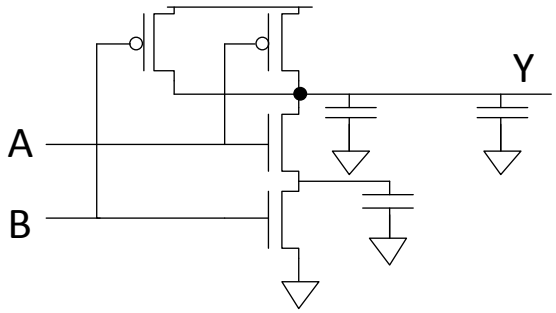


Figure 1: 2 input NAND Circuit

(a) Draw the circuit in Figure 1 on your answer sheet and label the width of all the MOSFETs and write down the capacitance for all gate, source, and drain nodes of the circuit.

(4 marks)

(b) Draw the simplified RC equivalent circuit for the device when the inputs AB are switching from low to high and mark the resistance and capacitor values (in terms of R and C).

(5 marks)

(c) Calculate the overall RC delay for the circuit.

(8 marks)

(d) Explain how the capacitance at the junction between the two NMOS transistors connected in series can be reduced.

(3 marks)

2. (a) FR4 substrate in a board is made up of resin with embedded glass fibers, (shown in Figure 2(a)). Calculate the capacitance per unit length of the trace on the left, considering the inhomogeneous dielectric material under the capacitor.

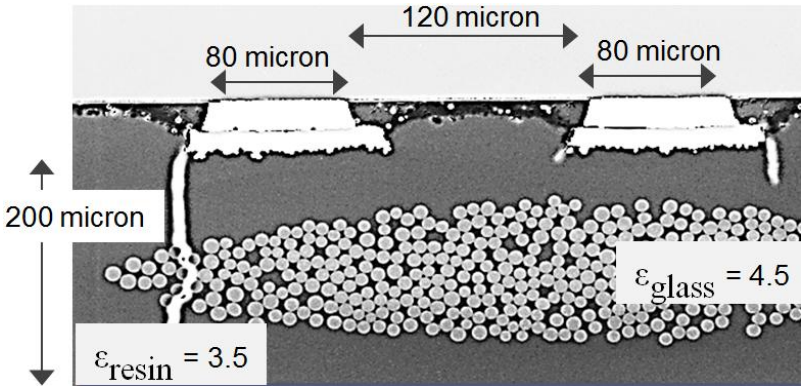


Figure 2(a) : FR4 board Cross Section

(6 marks)

(b) A surface mount component is used for a resistor in a 3 GHz data transmission line. The component is 2 mm long and 1mm wide and 1 mm tall. Given that the wavelength of a 1 GHz signal is 30 cm, determine if the component is seen as a lumped component by the signal – explain your answer.

(7 marks)

(c) The differential impedance of high speed interconnects built on 6000 FR4 boards have a normal distribution with a mean of 92 Ohms and standard deviation of 2 Ohms. Design requirement states that boards with differential impedance within +/- 3 sigma of the target specifications are acceptable.

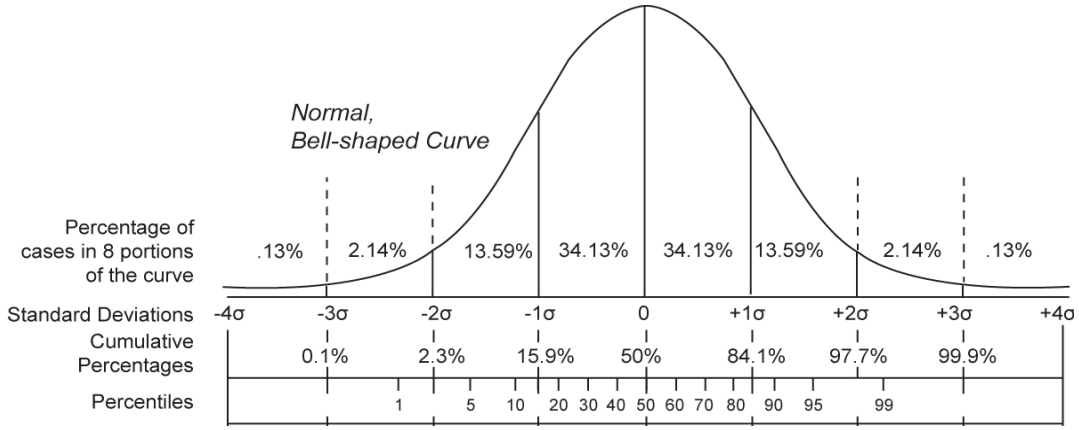


Figure 2(c) : Normal Statistical Distribution

(i) What is the range of the acceptable differential impedance? Explain.
(3 marks)

(ii) Of the 6000 boards built, how many boards built will have a good probability of being within specification of the differential impedance?
(4 marks)

3. The frequency domain plot in Figure 3 shows the impedance, Z, of the power distribution network of a circuit. Note that PDN impedance is given by $Z = \Delta V/\Delta I$. In the plot it is shown that the package capacitor is added to improve the impedance.

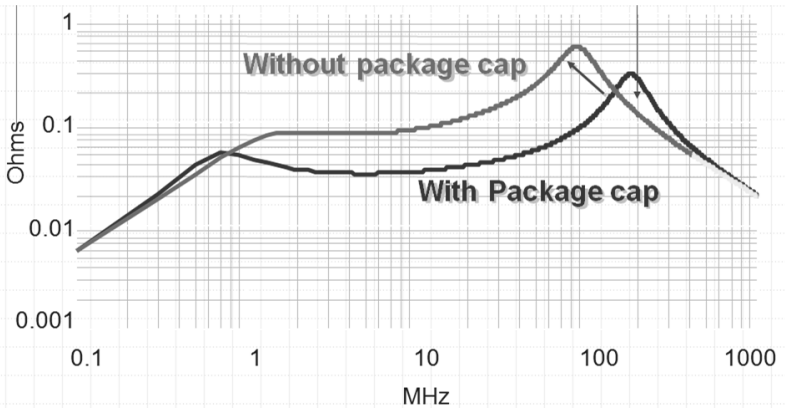


Figure 3: Frequency domain response of PDN

(a) Calculate the improvement in voltage droop at 100 MHz due to the added package capacitance. Consider that the current step rise at 100MHz is 10A.

(6 marks)

(b) From the plot in Figure 3, explain why adding the package capacitor may not have improved power delivery across all frequencies. Use data from the plot in Figure 3 to explain your answer. For a 200 MHz interconnect, is the package cap a good choice? Explain.

(6 marks)

(c) Why two diodes (one to Vdd and another to Gnd) are necessary to design the ESD circuit for IOs?

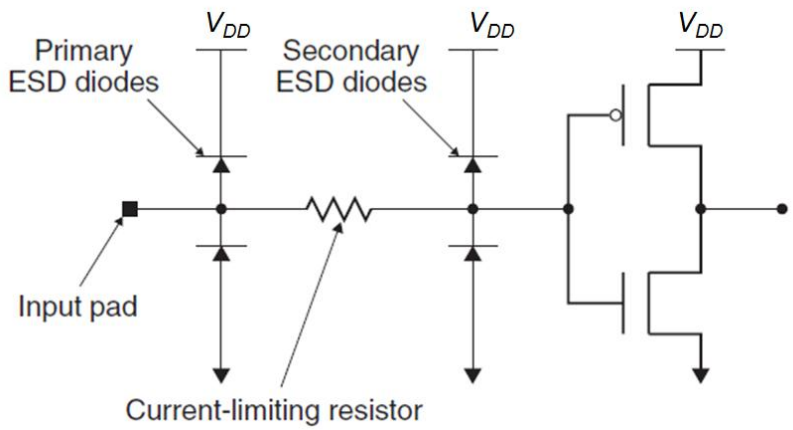


Figure 3(c) : ESD Protection Circuit

(4 marks)

(d) In the ESD circuit in Figure 3(c), the diodes will limit the voltage at the input of the inverter within a certain range. Given the V_{dd} and diode drop, what is that range? Assume the biasing drop for each of the diode is 0.2 V and the rail voltage (V_{dd}) is 1.25 V.

(4 marks)

4.

Figure 4: Microstrip Cross Section

(a) A cross-section of a microstrip line is shown in Figure 4. First draw the microstrip line on your answer sheet. Then plot the electric and magnetic fields for a microstrip line on your drawing.

(5 marks)

(b) Explain why a microstrip line cannot support a pure TEM mode of propagation.

(5 marks)

(c) Explain how the attenuation of the waves in a conductor results in a change in the resistance as the operating frequency is varied.

(5 marks)

(d) Transmission lines are designed to carry digital signals. Encodings schemes such as 8B/10B are widely used in high speed signaling. Explain why no more than 5 consecutive zeroes or ones are allowed in 8B/10B encoding.

(5 marks)

5. (a) Two different transmission lines in series are connected to a load of 50 Ohms, as shown in Figure 5(a). Find Z_{in}. You may use the transmission line equations or the Smith Chart.

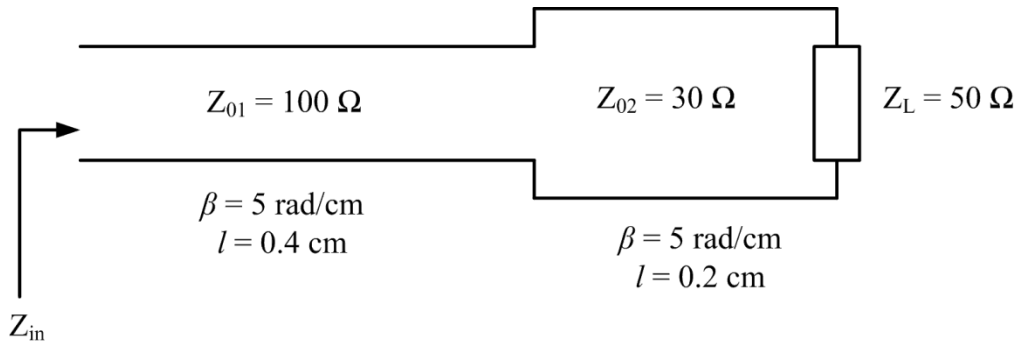


Figure 5(a) : Unmatched Transmission Line and Load

(8 marks)

(b) For the circuit in Figure 5(b), given that Z_{in} is to be matched to a 50 Ω transmission line, calculate the required characteristic impedance, Z_0.

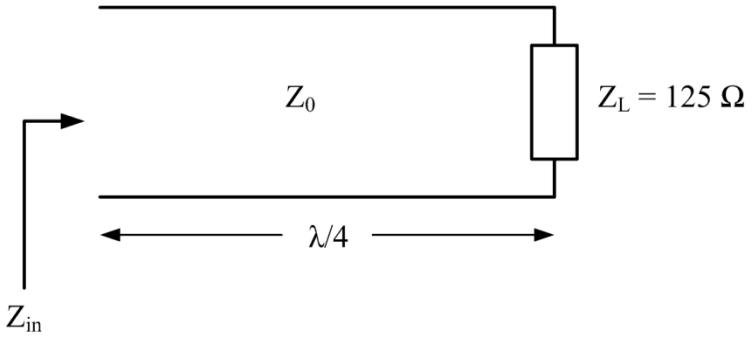


Figure 5(b) : Impedance Matching

(4 marks)

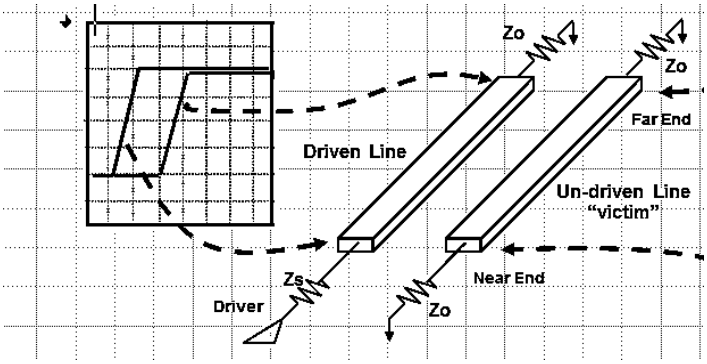
(c) At the operating frequency of interest, you find that the length *λ/4* for the circuit in Figure 5(b) to be 1 mm. This length is too short to be physically realizable. Propose another solution whereby Z_{in} can still be matched to 50 Ω at the operating frequency. Comment on any weaknesses of your proposed solution.

(4 marks)

(d) Explain why large value electrolytic capacitors will not be good choices for placement on packages, even if the packages sizes were ignored.

(4 marks)

6. Two transmission lines are located close to each other. A high speed signal is propagating on the line to the left. You will estimate the crosstalk on the other line (the Un-driven line).



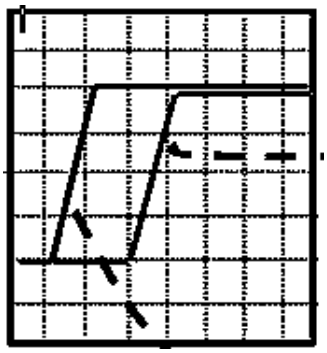


Figure 6: (left) Crosstalk in adjacent lines, (right) Draw this on your answer sheet.

(a) Draw the expected FEXT (Far End Crosstalk) and NEXT (Near End Crosstalk) from transmission line in Figure 6 (left) and label them in the graph on your answer sheet. (Draw the plot similar to the one shown in Figure 6(right) on your answer sheet and plot answer on it).

(5 marks)

(b) Which parameters in the inductance matrix shown below indicate Self-inductance and Mutual inductance? (Explain each in 2-3 lines)

$$\text{Inductance Matrix} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1N} \\ L_{21} & L_{22} & & \\ \vdots & & & \\ L_{N1} & \cdots & & L_{NN} \end{bmatrix}$$

(5 marks)

(c) Using Figure 6(c), show that: $L_{odd} = L_{11} - L_m = L_{11} - L_{12}$

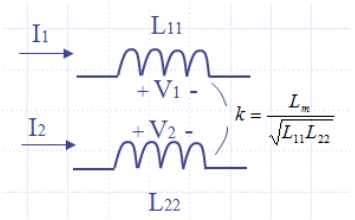


Figure 6(c) 3: Coupling between Inductors

(5 marks)

(d) A DOE experiment will be done to determine the impact of critical variables in the impedance of board decoupling capacitors on PDN impedance. Name 3 variables (decoupling capacitor design factors) that should be included as factors in the experiment and explain in 2-3 lines for each factor why they are important.

(5 marks)

7. Equalization in a high speed circuit is implemented as shown in the circuit in Figure 7.

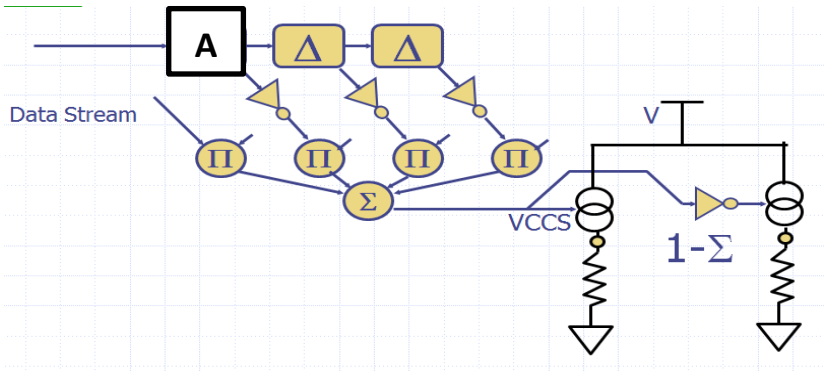


Figure 7 : Equalization

(a) Describe the main purpose of block A – explain in 3-5 lines.

(4 marks)

(b) Describe two advantages of continuous time linear equalizer over discrete time linear equalizer.

(3 marks)

(c) Describe one advantage and drawback of DFE.

(3 marks)

(d) Data is transmitted from Tx to Rx through the Channel as shown in Figure 7(d). There is jitter in the data. Answer the following.

Figure 7(d) : Transmitter and Receiver

(i) What is the predominant source of the two types of jitter, R_J and D_J?

(3 marks)

(ii) Total jitter T_J comprises R_J and D_J

(1) Describe T_J of the whole system in terms of R_J and D_J?

(2) How do we budget system jitter in terms of channel, Tx and Rx?

(4 marks)

(iii) PCIe Gen3 UI (Unit Interval) is 200 ps, T_J of the system 0.55 UI, how much is the expected max timing margin possible in ps? Show how you derived the answer.

(3 marks)

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