UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013 / January 2014

EEE 520/4 – Embedded Microprocessor Systems

Duration : 3 hours

Please check that this examination paper consists of **SEVEN (7)** pages printed material before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) Describe the characteristics of Real Time System (RTS) and Real-Time Operating System (RTOS) and comparison with the conventional general processor system.

(20 marks)

(b) Describe the following tests that must be conducted as part of the Rate Monotonic Analysis (RMA) approach.
(i) Utilisation Test
(ii) Completion Time Test
(iii) Response Time Test.

(30 marks)

(c) For real-time system scheduling it is important to know the maximum (worst-case) execution time of each task a priori? However, if this information is given, there are several other problems that may be encountered during the design of a scheduling algorithm for a real-time system. Can you think of some difficulties? What are possible solutions? How can we compare different scheduling algorithms?

(30 marks)

(d) Evaluate, by using appropriate test methods, if the given task-set in Table 1(d) is schedulable using the Rate Monotonic (RM) method.

Table 1(d)

	τ_1	τ_2	τ_3
C_i	1	3	2
T_i	3	8	9

(20 marks)

2. (a) Describe the "*Testing Steps*" needed to be done on the Host Machine for debugging purpose.

(20 marks)

(b) Describe the use of the following debugging methods, with suitable diagrams;
(i) ROM Emulator
(ii) Background Debug Mode (BDM)
(iii) In-Circuit Emulator (ICE)
(iv) Logic Analyzer

(20 marks)

(c) What is a "boundary scan" technique utilized in debugging process? Explain the technique with appropriate diagram.

(20 marks)

(d) The following Figure Q2(d) shows part of the PIC1684A internal architecture. Study the figure and answer the following questions.

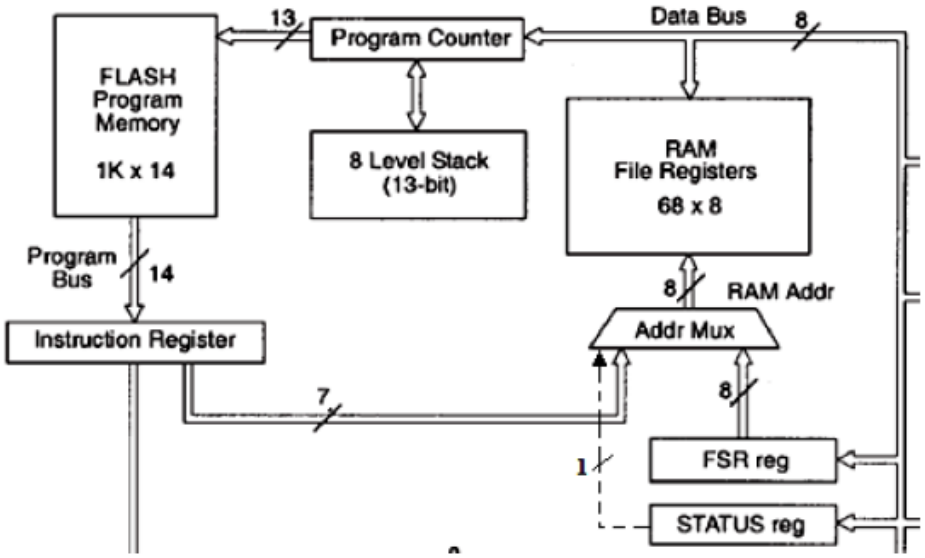

Figure Q2(d)

(i) What is the purpose of the Stack block?
(ii) What is the size of each memory location in the Program Memory? Can you tell why?
(iii) What is the purpose of the 1-bit dashed wire?
(iv) Explain why the Program Counter is connected to the Data Bus?

(40 marks)

3. (a) Why is optimization needed for an embedded system design and development stage? Give examples of optimization methods usually employed for this purpose.

(20 marks)

(b) Provide comparison between the *"cyclic executive"* and *"round robin with interrupt"* programming approach in the software development aspect of an embedded system development.

(20 marks)

(c) Describe what is meant by the term "V-model" to represent software or hardware development process.

(20 marks)

(d) Refer to Figure Q3(d) and uses an appropriate example, describe the requirements and processes needed in implementing the hardware and software co-design approach for an embedded system application design and development.

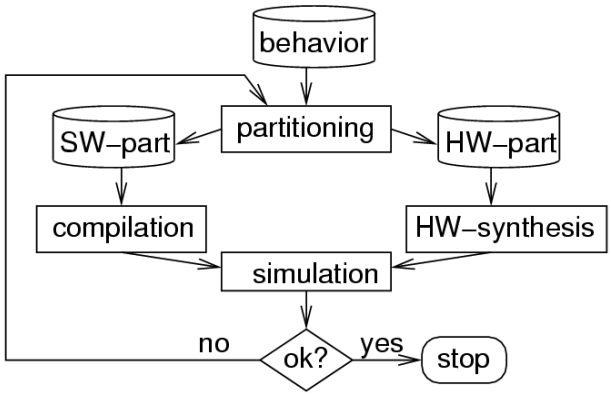

Figure Q3(d)

(40 marks)

4. (a) Sequential circuits are also called finite state machine (FSM). State a difference between synchronous sequential circuit and asynchronous sequential circuit.

(5 marks)

(b) FPGA is used in the realization of an embedded hardware system designed to perform fast control for an atomic force microscope (AFM). Traditional implementation of control algorithm for AFMs either PC based of DSP based, where it does not meet the high speed scanning requirement. Discuss about the advantages (3 advantages) of FPGA to meet the high speed scanning requirement in this application.

(45 marks)

(c) Design a system to detect the previous two values of input (w) were 00 or 11. When the input (w) were 00 or 11, the output (z) will be 1, otherwise output (z) will be 0. Alarm will be triggered when output (z) is 1. Explain your design using block diagram, state diagram, state table and verilog code. Use Moore circuit in your design.

(50 marks)

5. (a) State the communication scheme in Figure 5(a) and Figure 5(b).

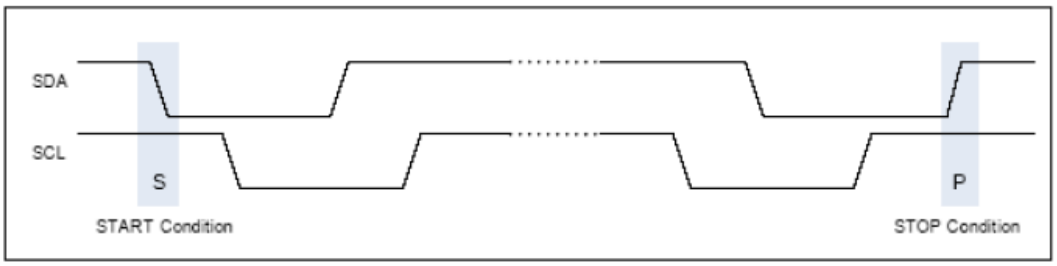

Figure 5(a)

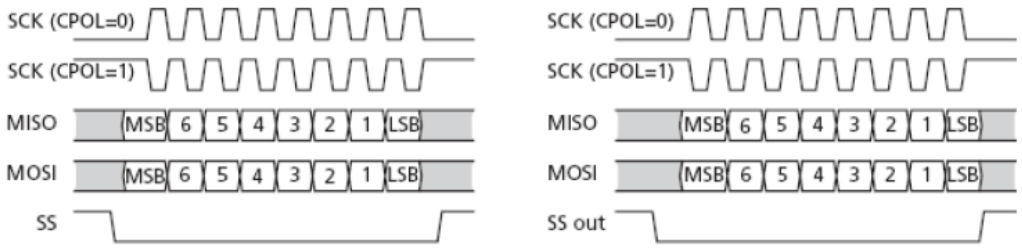

Figure 5(b)

(10 marks)

(b) What is advantage and disadvantage of SPI compared to I2C communication scheme?

(20 marks)

(c) Figure 5(c) indicates a typical direct memory access controller interface. Show and explain the timing diagram when the DMA controller needs to access the memory.

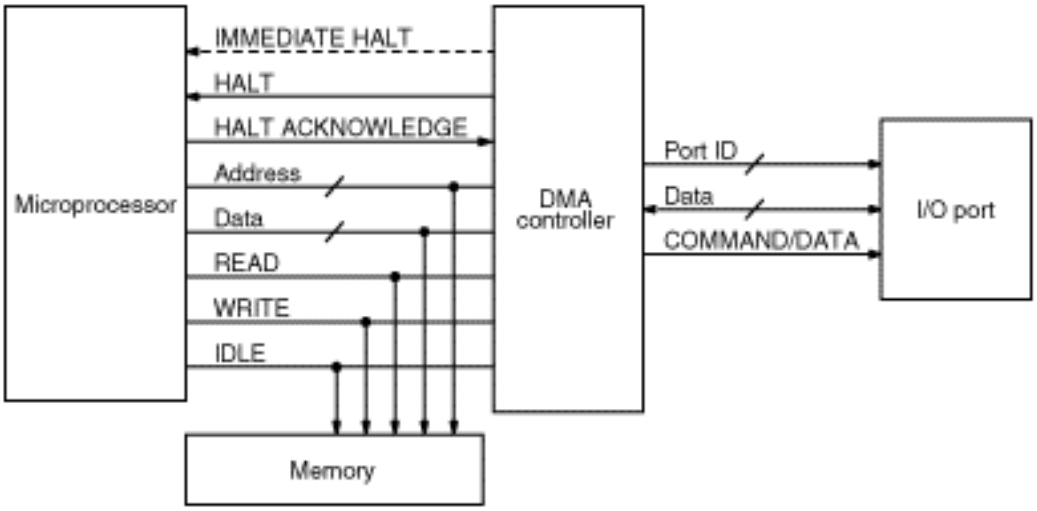

Figure 5(c) : Direct memory access controller interface

(40 marks)

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(d) State one application of DMA in embedded system design

(10 marks)

(e) State 2 advantages of DMA in embedded system design.

(20 marks)

6. (a) Polling is a synchronous mechanism, by which devices are serviced in sequential order. It is the most common and simplest method of I/O control. It requires no special hardware and all I/O transfers are controlled by the CPU programme. The polling technique however has some limitations. Give 4 limitations of polling technique.

(20 marks)

(b) Diagram in Figure 6(b) shows the Daisy Chain Interrupt. Discuss about interrupt priority for the Daisy Chain Interrupt.

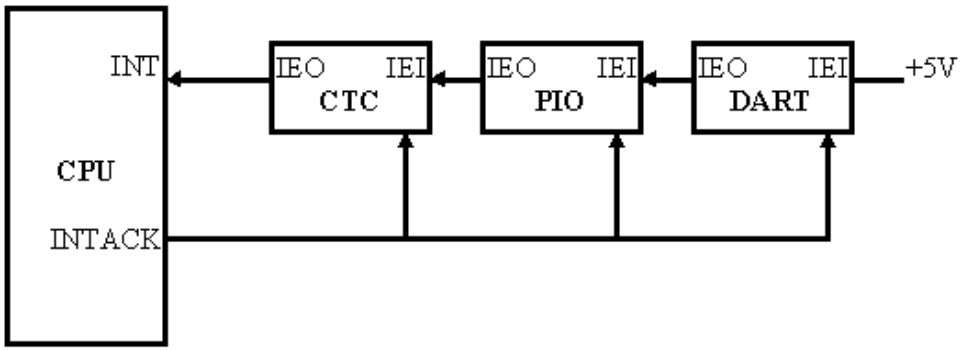

Figure 6(b) : Daisy chain interrupt

(30 marks)

(c) Explain about the interrupt vector.

Figure 6(c) shows the pin diagram of interrupt controller. There are 8 interrupt input request lines named IR0 until IR7 or called as vectored interrupt.

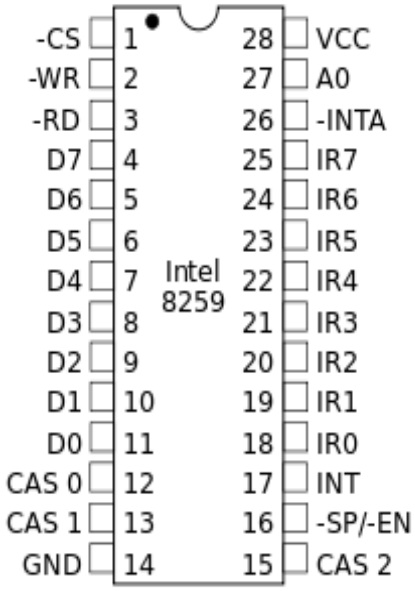

Figure 6(c) : Pin Diagram of interrupt controller interface to CPU

(20 marks)

(i) What is a difference between this interrupt compared to daisy chain interrupt.

(ii) Give one advantage and 4 disadvantages of this type of interrupt.

(30 marks)

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