
UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013 & January 2014

EEE 510/4 – Advanced Analogue Circuit Design

Duration : 3 hours

Please check that this examination paper consists of **SEVEN (7)** pages of printed material before you begin the examination.

Instructions: Answer **FIVE (5)** questions. Answer **TWO (2)** questions in Part A and **TWO (2)** questions from Part B and **ONE (1)** question from any section.

Use two-book answers for **Part A** and **Part B**.

All questions carry the same marks.

Part A : Answer TWO question

1. Figure 1 shows M1 and M2 having back to back connections. The output resistance is 1 k Ω . Current I and I_B are 100 μ A. V_{TH} is 0.6 V, μnC_{OX} is 194 μ A/V² and λ is 0.

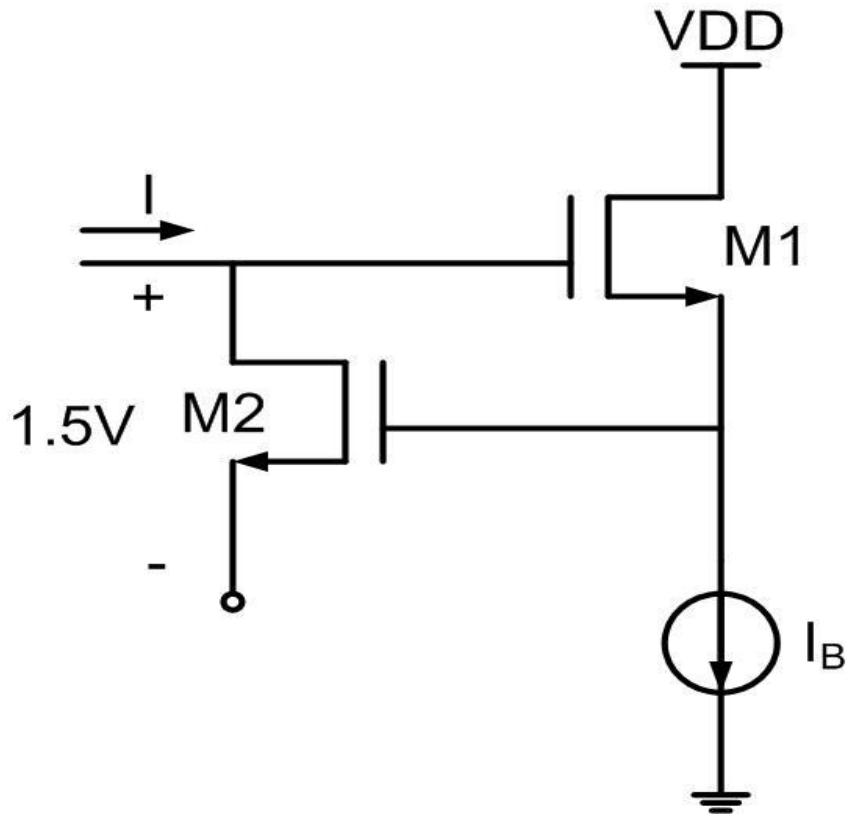


Figure 1

- (a) Find value of V_{GS1} and V_{GS2} .

(10 marks)

- (b) Find value of $\left(\frac{W_1}{L_1}\right)$ and $\left(\frac{W_2}{L_2}\right)$.

(10 marks)

2. Figure 2 refer to folded cascade OTA with bias currents $I = 150 \text{ uA}$ and $I_b = 150 \text{ uA}$. All transistors operated at the overdrive voltages of 0.2 V .

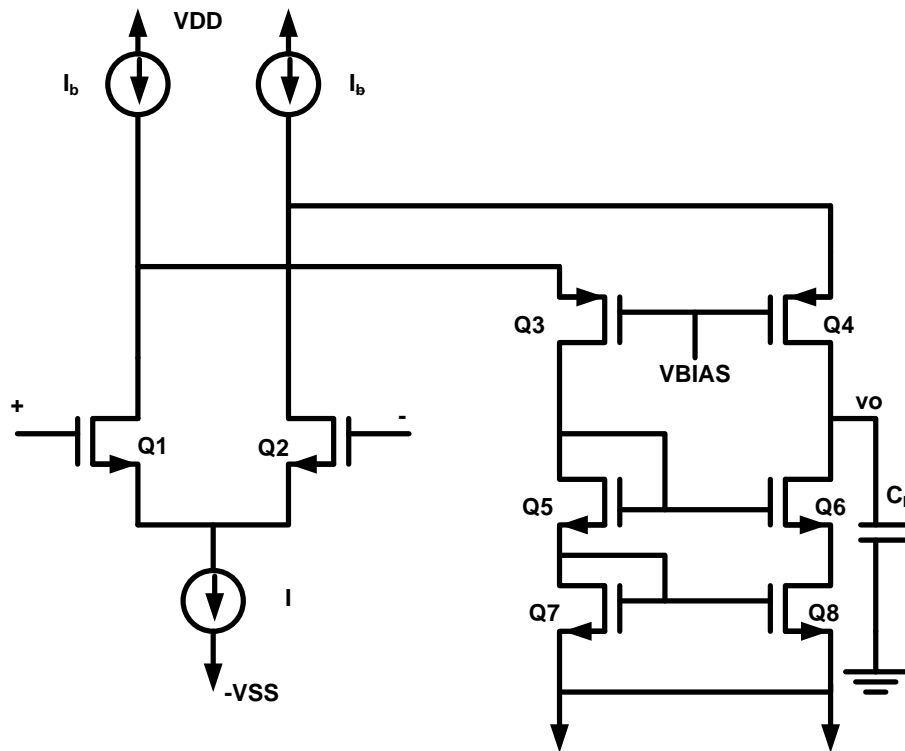


Figure 2

- (a) What is the expression of output resistance. (5 marks)
- (b) Based on the specification given if C_L is 350 f, what would be the OTA Gainbandwidth (GBW). (15 marks)

3. Figure 3 shows the cascade configuration of M1 and M2. The gate of M1 is driven by the drain of M3.

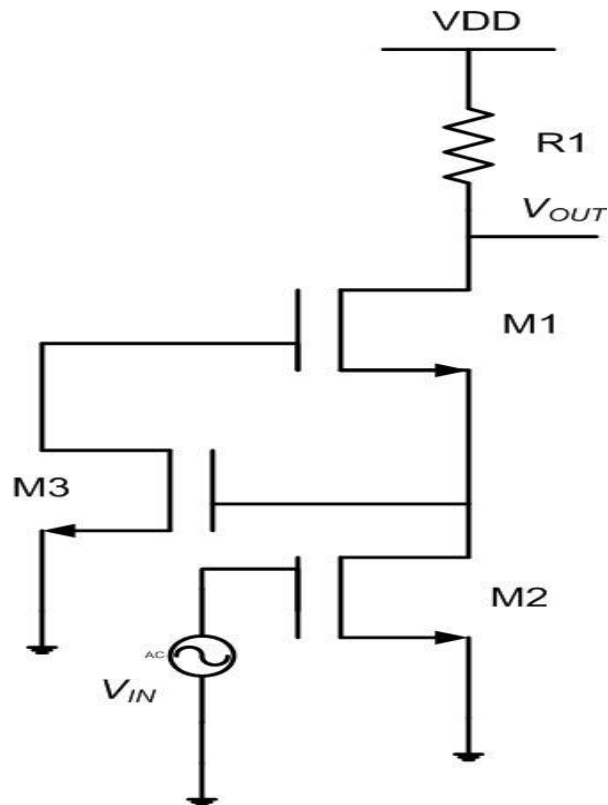


Figure 3

- (a) Draw a small signal configuration of the circuitry in figure 3.

(5 marks)

- (b) Derive the output resistance of the circuit.

(15 marks)

Part B : Answer TWO question

4. (a) By using a 3-bit example of DAC, explain the concept of LSB and DNL. (8 marks)
- (b) Explain how a 5-bit weighted current source design can be developed based on a basic current source. Derive relevant equations to support your design. What are the advantages and disadvantages of this design? (12 marks)
5. (a) Based on Figure 5(a), derive a simplified 8-bit DAC mathematical model. Explain the 8-bit model based on this topology with the help of suitable schematic drawing. Explain the functions of all components in the schematic.

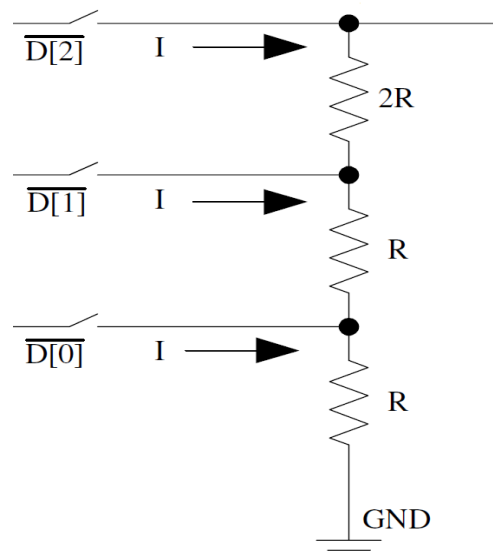


Figure 5(a) : 3-bit DAC

- (10 marks)
- (b) Design a 13-bit DAC based on the combination of the topology given in Question 5(a) and the thermometer coded topology. The model should have a combination of 8-bit LSB (binary-weighted resistor) and 5-bit MSB (thermometer coding). Explain the model based on the function of each component using an appropriate schematic drawing and then, derive the equations for 13-bit DAC. (10marks)

6. (a) By using appropriate graphs, explain briefly the concepts of CTAT and PTAT.
(4 marks)
- (b) The circuits in Figure 6(b) are used to develop a bandgap reference or BGR. Explain how the BGR can be developed using a combination of both circuits. Provide the relevant mathematical equations to support your explanation.

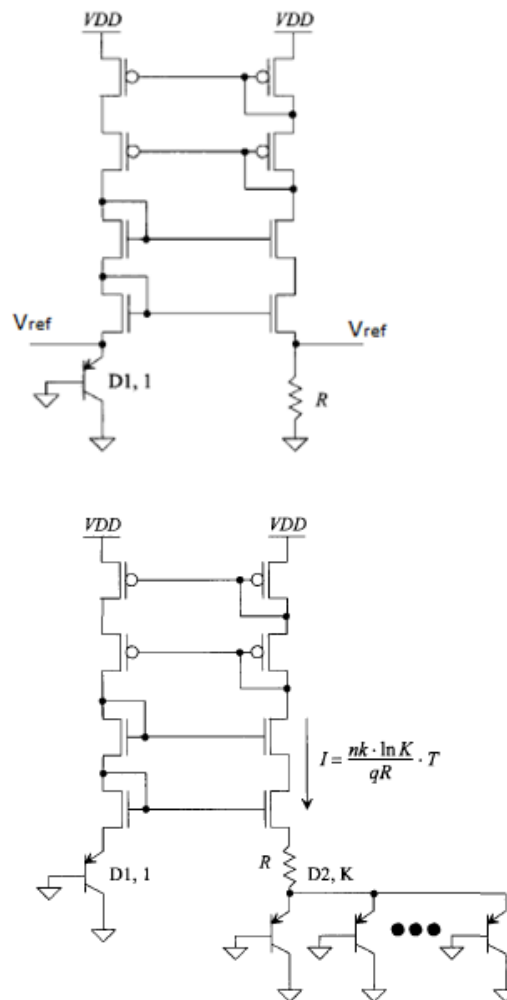


Figure 6(b)

(12 marks)

- (c) Figure 6(c) shows the alternate topology of the BGR based on the topology discussed in Question 6(c). Briefly explain the merit and demerit of this architecture.

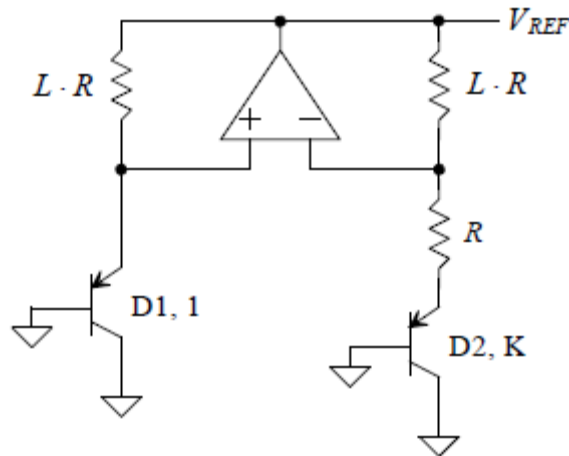


Figure 6(c) : Alternate BGR Circuit

(4 marks)

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