
UNIVERSITI SAINS MALAYSIA

First Semester Examination
2013/2014 Academic Session

December 2013/January 2014

EEE 241 – ANALOG ELECTRONIC I
[ELEKTRONIK ANALOG I]

Duration : 3 hours

[Masa : 3 jam]

Please check that this examination paper consists of **NINE (9)** pages printed material and **TWO (2)** pages of Appendices before you begin the examination.

*[Sila pastikan bahawa kertas peperiksaan ini mengandungi **SEMBILAN (9)** mukasurat bercetak beserta Lampiran **DUA (2)** muka surat bercetak sebelum anda memulakan peperiksaan ini.]*

Instructions: Answer **FIVE (5)** questions. Answer **TWO (2)** questions in Section A and **TWO (2)** questions from Section B and **ONE (1)** question from any section.

Arahan: Jawab **LIMA (5)** soalan. Jawab **DUA (2)** soalan dalam Bahagian A dan **DUA (2)** soalan dalam Bahagian B dan **SATU (1)** soalan daripada mana-mana Bahagian.]

Use separate answer booklets for **Section A** and **Section B**.

*[Gunakan dua buku jawapan yang berasingan bagi **Bahagian A** dan **Bahagian B**.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

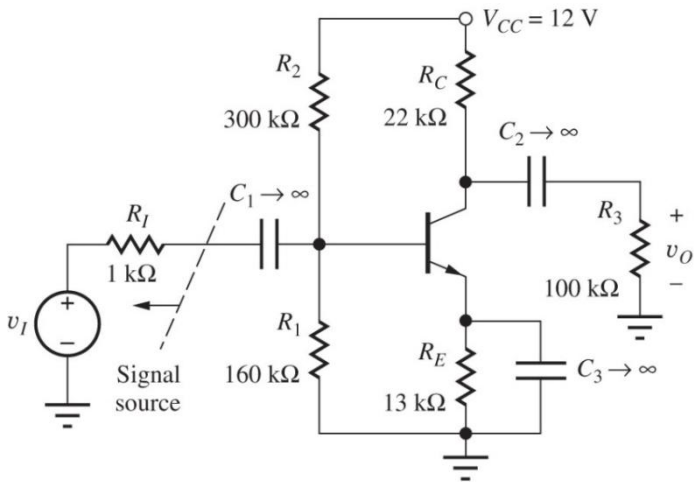
Bahagian A

Section A

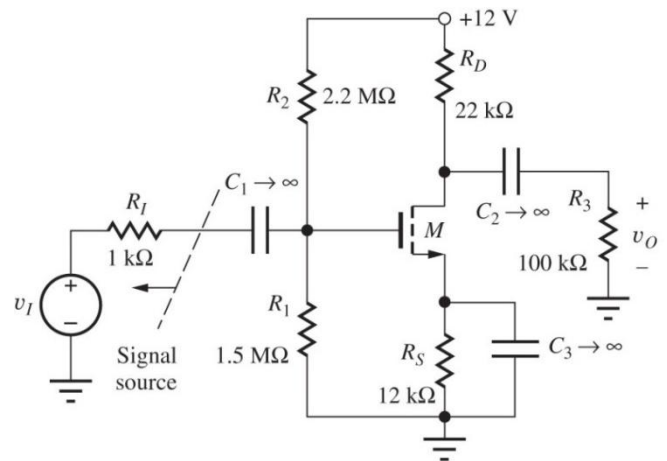
1. (a) Lukis model penuh isyarat-kecil bagi litar-litar Rajah 1 (a)(i) dan Rajah 1 (a)(ii).

Draw the complete small-signal model for the circuits in Figure 1 (a)(i) and Figure 1 (a)(ii).

(6markah/marks)



Rajah 1(a)(i)
Figure 1(a)(i)



Rajah 1(a)(i)
Figure 1(a)(i)

- (b) Kirakan gandaan voltan bagi penguat pemancar- sepunya dalam Rajah 1(a)(i) jika transistor mempunyai $\beta_o = 150$, $V_A = 100$ V dan Q-point = (0.25 mA, 3.5 V). Apakah nilai maksimum V_I bagi memenuhi andaian-andaian isyarat-kecil.

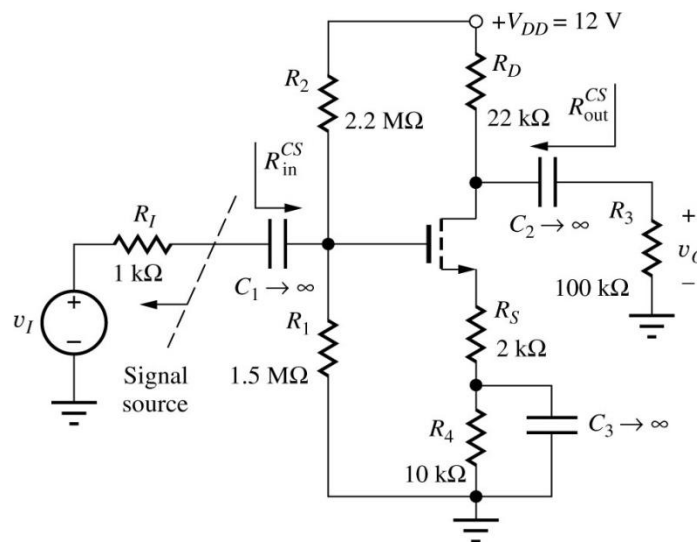
Calculate the voltage gain of the common-emitter amplifier in Figure 1(a) if the transistor has $\beta_o = 150$, $V_A = 100$ V and Q-point = (0.25 mA, 3.5 V). What is maximum value of V_I that satisfies the small-signal assumptions?

(14 markah/marks)

2. (a) Kirakan gandaan, rintangan masukan dan keluaran bagi penguat CS dalam Rajah 2(a) jika transistor mempunyai $K_n = 0.500 \text{ mA/V}^2$, $V_{TN} = 1.5 \text{ V}$ dan $\lambda = 0.0133 \text{ V}^{-1}$, dan Q-point = (0.25 mA, 3.5 V). Apakah nilai maksimum V_i supaya andaian-andaian isyarat-kecil terguna-pakai?

Calculate the gain, input and output resistance of the common-source amplifier in Figure 2(a) if the transistor has $K_n = 0.500 \text{ mA/V}^2$, $V_{TN} = 1.5 \text{ V}$ and $\lambda = 0.0133 \text{ V}^{-1}$, and the Q-point = (0.25 mA, 3.9 V). What is the largest value of V_i that does not violate the small-signal assumptions?

(12 markah/marks)



Rajah 2(a)
Figure 2(a)

- (b) Ulang bahagian (a) jika kapasitor C_3 diletakkan antara terminal punca dan juga bumi bagi transistor tersebut.

Repeat part (a) if by pass capacitor C_3 is placed between the source terminal of the transistor and ground.

(8 markah/marks)

3. (a) Merujuk kepada Rajah 3, nyatakan samaada C_1, C_2 dan C_3 adalah kapasitor gandingan atau pirau. Apakah kegunaan kapasitor-kapasitor ini?

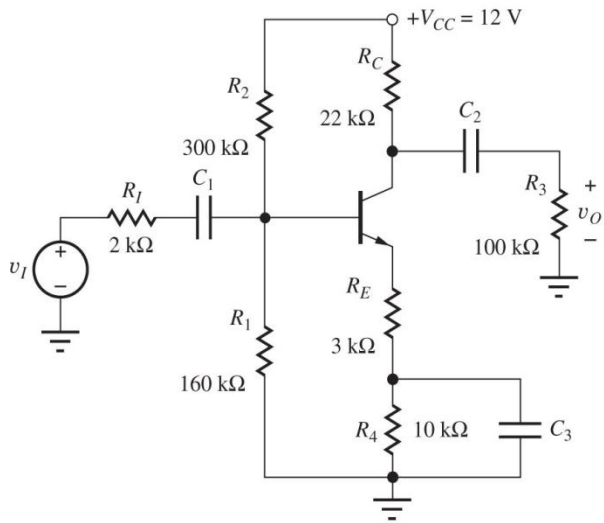
Referring to Figure 2, state whether C_1, C_2 and C_3 are coupling or by pass capacitors. What are the application of these capacitors?

(6 markah/ marks)

- (b) Kirakan nilai kapasitor – kapasitor C_1, C_2 dan C_3 bagi kedua – dua litar seperti di dalam Rajah 3(a) dan Rajah 3(b) supaya nilai kapasitor – kapasitor tersebut tidak mempengaruhi fungsi litar pada frekuensi 1.5 kHz. Kemudian, berdasarkan nilai-nilai tersebut, pilih nilai yang terdekat daripada Apendik A.

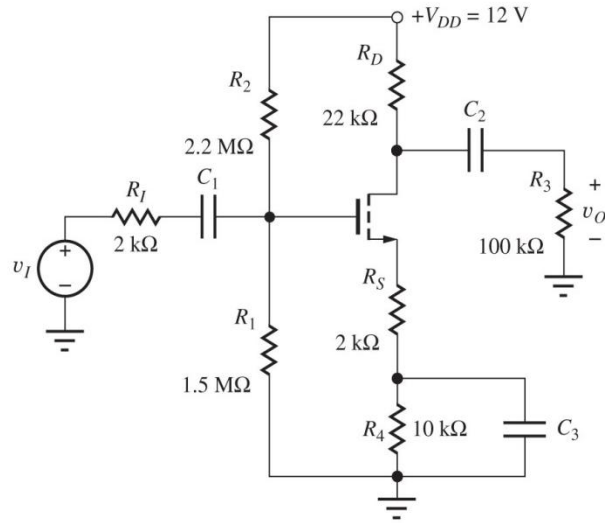
Find the values for capacitors C_1, C_2 and C_3 for both circuits as in Figure 3(a) and Figure 3(b) so that the presence of these capacitors can be neglected at a frequency of 1.5 kHz. Then, based on the values calculated, choose the nearest values of the capasitors from Appendix A.

(14 markah/marks)



Rajah 3(a)

Figure 3(a)



Rajah 3(b)

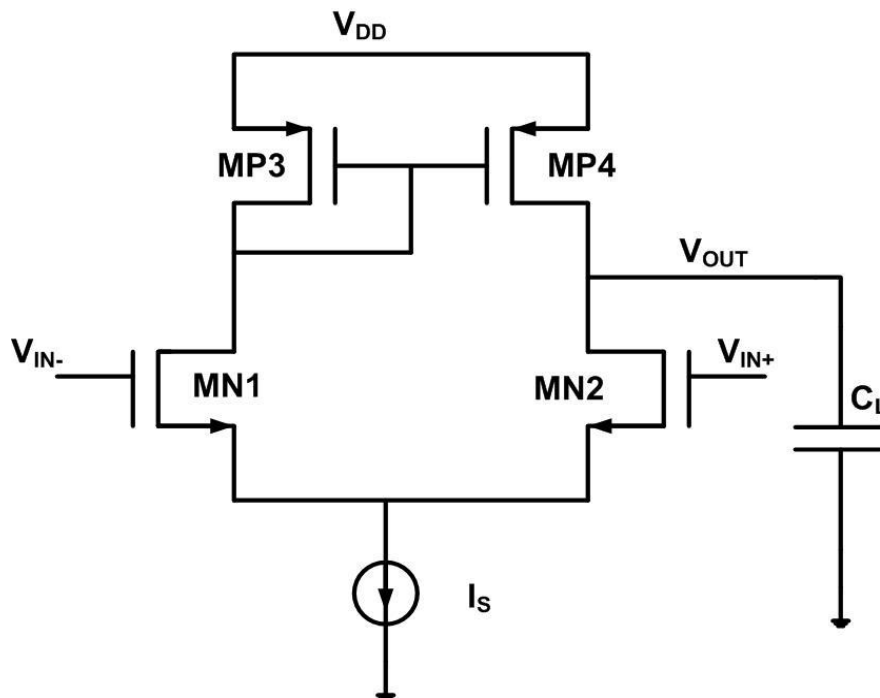
Figure 3(b)

Bahagian B

Section B

4. (a) Rajah 4(a) adalah satu CMOS OTA mudah. K_n adalah $20 \frac{\mu A^2}{V}$, K_p adalah $10 \frac{\mu A^2}{V}$, lebar MN1(W1) dan MN2(W2) adalah masing-masing bernilai 50 μm . Lebar MP3(W3) dan MP4(W4) beserta panjang semua transistor adalah masing-masing 5 μm . I_S ialah 100 μA , λ adalah 0.1 dan VDD adalah 10V.

Figure 4(a) is Simple CMOS OTA. K_n is $20 \frac{\mu A^2}{V}$, K_p is $10 \frac{\mu A^2}{V}$, the width of MN1(W1) and M2(W2) is 50 μm each. The width of MP3(W3) and MP4(W4) and the length of each transistor is 5 μm . I_S is 100 μA , λ is 0.1 and VDD is 10V.



Rajah 4(a)
Figure 4(a)

- (i) Kira Trankonduktur g_{m1} .
Calculate Transconductance g_{m1} .

(5 markah/marks)

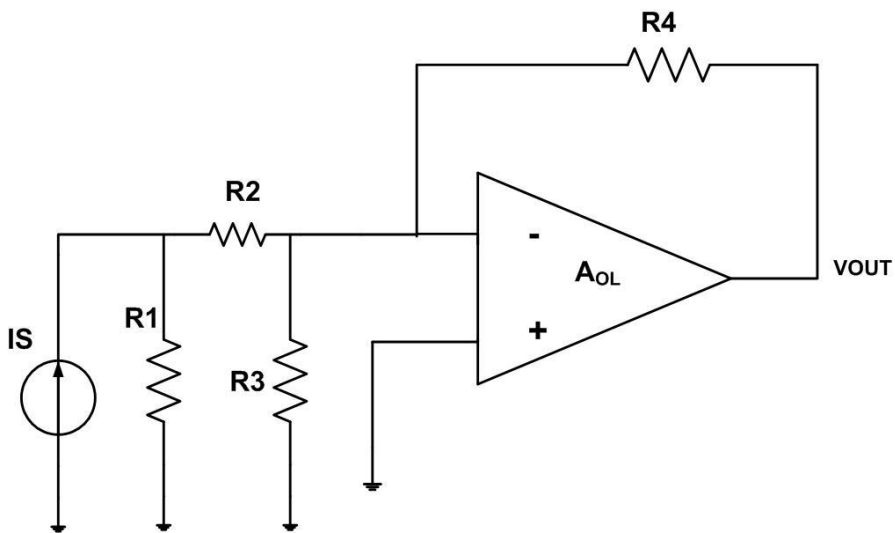
- (ii) Kira frekuensi tiang dominan.
Calculate dominant pole frequency.

(10 markah/marks)

- (iii) Kira gandaan DC.
Calculate the DC Gain.

(5 markah/marks)

5. Kirakan yang berikut:
Calculate the following:.



Rajah 5
Figure 5

- (a) Gandaan konfigurasi ialah 4 . IS adalah 100uA , R1 adalah 0.1 M Ω , R2 adalah 0.1M Ω , R3 adalah 0.2 M Ω dan R4 = 10 M Ω .

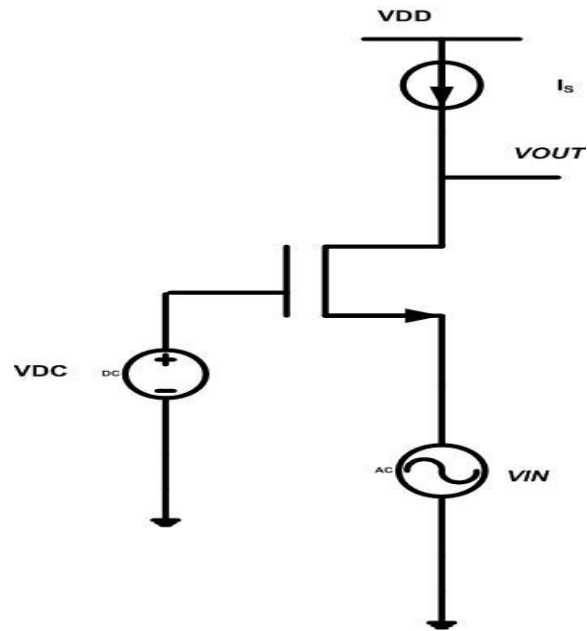
Gain of configuration is 4 . IS is 100uA , R1 is 0.1 M Ω , R2 is 0.1 M Ω , R3 is 0.2 M Ω and R4 = 10 M Ω .

(10 markah/marks)

- (b) Jika A_{OL} adalah 60dB, apakah peratusan ralat dalam gandaan litar tertutup.

If the open loop gain A_{OL} is equal to 60dB, what is the percentage of error of the closed loop gain.

(10 markah/marks)



Rajah 6

Figure 6

6. Terbitkan:

Derive:

(a) Rintangan keluaran konfigurasi get sama seperti didalam Rajah 6.

The output resistance of common gate configuration as in Figure 6.

(10 markah/marks)

(b) Transkoaduktans G_m bagi konfigurasi get sama seperti didalam Rajah 6.

Transconductance G_m of the common gate configuration as in Figure 6.

(10 markah/marks)

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