UNIVERSITI SAINS MALAYSIA

First Semester Examination
2012/2013 Academic Session

January 2013

EEE 241 – ANALOG ELECTRONIC I
[ELEKTRONIK ANALOG I]

Duration : 3 hours
[Masa : 3 jam]

Please check that this examination paper consists of NINE (9) pages of printed material before you begin the examination.
[Sila pastikan bahawa kertas peperiksaan ini mengandungi SEMBILAN (9) mukasurat bercetak sebelum anda memulakan peperiksaan ini.]

Instructions: This question paper consists SIX (6) questions. Answer **FIVE** (5) questions. All questions carry the same marks.
[***Arahan:*** *Kertas soalan ini mengandungi ENAM (6) soalan. Jawab **LIMA** (5) soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.
[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. Lukis model isyarat-kecil bagi transistor NMOS dengan nilai-nilai I_D = 150 µA, V_{SB} = 1 V, V_{DS} = 2.5 V. Parameter-parameter peranti diberikan: ϕ_f = 0.3 V, W = 20 µm, L = 1.5 µm, γ = 0.5 $V^{1/2}$, k' = 200 µA/V^2, λ = 0.02 V^{-1}, t_{ox} = 100 angstroms, ψ_o = 0.6 V, C_{sb0} = C_{db0} = 10 fF. Kapasitan bertindih daripada *gate to source* dan *gate to drain* bernilai 1 fF. Anggarkan C_{gb} = 5 fF.

Draw the complete small-signal model for an NMOS transistor with I_D = 150 µA, V_{SB} = 1 V, V_{DS} = 2.5 V. *Device parameters are:* ϕ_f = 0.3 V, W = 20 µm, L = 1.5 µm, γ = 0.5 $V^{1/2}$, k' = 200 µA/V^2, λ = 0.02 V^{-1}, t_{ox} = 100 angstroms, ψ_o = 0.6 V, C_{sb0} = C_{db0} = 10 fF. *Overlap capacitance from gate to source and gate to drain is 1 fF. Assume* C_{gb} = 5 fF.

(20 markah/*marks*)

2. (a) Merujuk kepada Rajah 1, nyatakan sama ada C_1,C_2 dan C_3 adalah kapasitor gandingan atau pirau. Apakah kegunaan kapasitor-kapasitor ini?

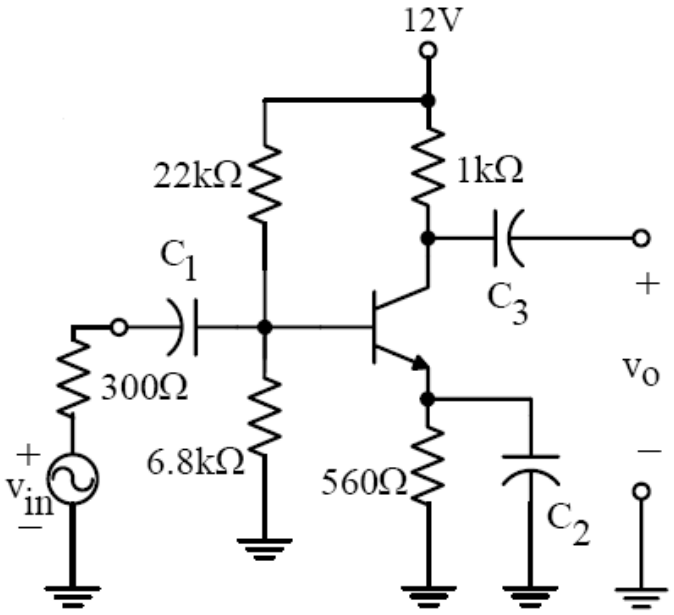
Referring to Figure 1, state whether C_1, C_2 *and* C_3 *are coupling or bypass capacitors. What are the applications of these capacitors?*

(6 markah/*marks*)

(b) Kirakan gandaan voltan bagi penguat pemancar- sepunya dalam Rajah 1 dengan dan tanpa kapasitor C_2, jika transistor mempunyai β_o = 150, β_F = 160, V_T = 26 mV dan V_{BE} = 0.7 V.

Calculate the voltage gain of the common-emitter amplifier in Figure 1 with and without capacitor C_2, *if the transistor has* β_o = 150, β_F = 160, V_T = 26 mV *and* V_{BE} = 0.7 V.

(14 markah/*marks*)

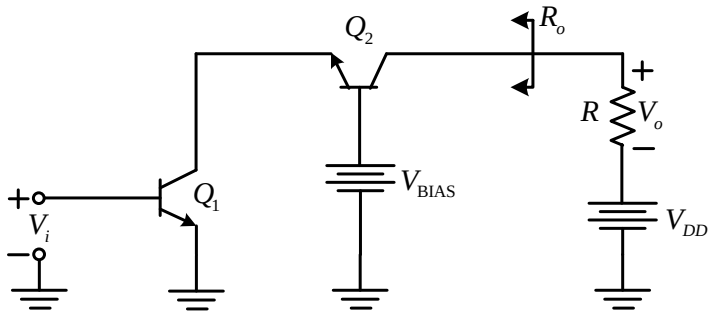


Rajah 1

Figure 1

3. Merujuk kepada Rajah 2, transistor dwikutub kaskod yang mengandungi pemancar-sepunya menjana tapak-sepunya diberikan. Ciri-ciri penting di dalam menganalisa litar ini adalah rintangan masukan R_i, rintangan keluaran R_o, kealiran pindah G_m, dan gandaan voltan A_v. Andaikan rintangan tapak r_b diabaikan.

In Figure 2, the bipolar cascode transistor that constitutes the common-emitter driving the common-base is shown. The key characteristics in analyzing this circuit are the input resistance R_i, output resistance R_o, system transconductance G_m, and the voltage gain A_v. Assume that base resistance r_b is negligible.



Rajah 2

Figure 2

(a) Lukis litar setara isyarat kecil menggunakan model π. Tandakan litar sepenuhnya.

Draw the small signal equivalent circuit using π-model. Label the circuit completely.

(5 markah/*marks*)

(b) Cari rintangan masukan R_i , dan sistem kealiran pindah G_m.

Find input resistance R_i, and the system transconductance G_m.

(10 markah/*marks*)

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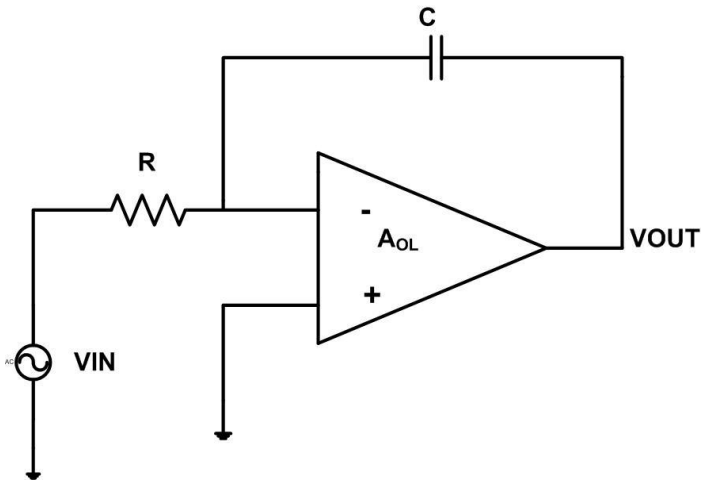
(c) Cari gandaan voltan A_v.

Find the voltage gain A_v.

(*5* markah/*marks*)

4.



Rajah 3

Figure 3

Rajah 3 menunjukkan pengkamil dengan gandaan operasi bergadaan A_{OL}.

Figure 3 shows integrator with operational amplifier has the gain of A_{OL}.

(a) Hasilkan pengkamil persamaan pindah dengan A_{OL}.

Derive integrator transfer function with finite A_{OL}.

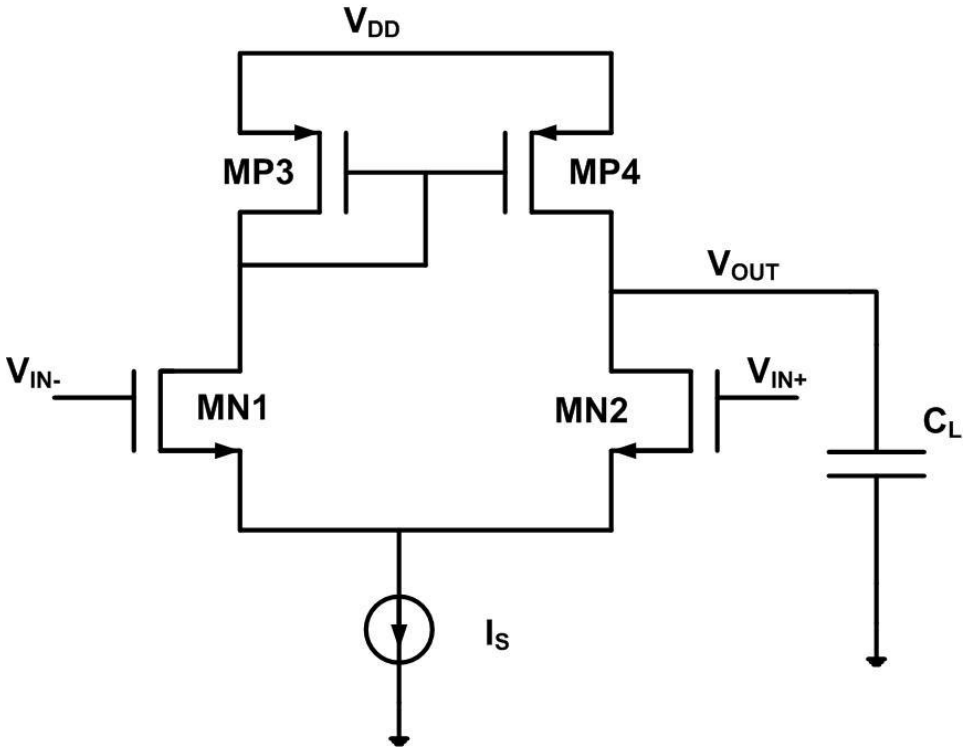
(5 markah/*marks*)

(b) Jika R adalah 1kΩ and 1μF kirakan peratus perbezaan keluaran magnitude jika A_{OL} adalah 10 dan 100.

If R is 1kΩ and C is 1μF calculate percentage deviation of the output magnitude if A_{OL} is 10 and 100.

(15 markah/*marks*)

5.



Rajah 4

Figure 4

Diagram di dalam Rajah 4 menunjukkan CMOS OTA. Jika kn adalah $\mathbf{20}\frac{\boldsymbol{uA^2}}{\boldsymbol{V}}$, Kp adalah $\mathbf{20}\frac{\boldsymbol{uA^2}}{\boldsymbol{V}}$, W1,W2 is 50um, W3,W4,L1,L2,L3,L4 = 5um. $\boldsymbol{I_S}$ adalah $\mathbf{10}\boldsymbol{uA}, \boldsymbol{\lambda} = \mathbf{0.1}\ \mathbf{CL} = \mathbf{1pf.}$

Diagram in Figure 4 is Simple CMOS OTA. If Kn is $\mathbf{20}\frac{\boldsymbol{uA^2}}{\boldsymbol{V}}$ *, Kp is* $\mathbf{20}\frac{\boldsymbol{uA^2}}{\boldsymbol{V}}$*, W1,W2 is 50um, W3,W4,L1,L2,L3,L4 = 5um.* $\boldsymbol{I_S}$ *is* $\mathbf{10}\boldsymbol{uA}, \boldsymbol{\lambda} = \mathbf{0.1}\ \boldsymbol{CL} = \mathbf{1}\boldsymbol{pf}$*.*

…8/-

(a) Cari nilai trankonduktan gm1.

Find transconductance gm1.

(5 markah/*marks*)

(b) Hitungkan frekuensi tiang dominan

Calculate dominant pole frequency.

(10 markah/*marks*)

(c) Kira gadaan jalur lebar.

Calculate the Gainbandwidth.

(5 markah/*marks*)

6. Rajah 5 menunjukkan MN1 pintu dihubungkan ke parit.

Figure 5 shown MN1 has gate connected to the drain.

(a) Lukis isyarat kecil litar.

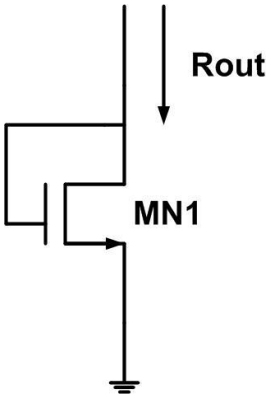
Draw small signal equivalent circuit.

(10 markah/*marks*)

(b) Dapatkan persamaan R_{out}.

Derive the expression of R_{out}.

(10 markah/*marks*)



Rajah 5

Figure 5

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