UNIVERSITI SAINS MALAYSIA

Peperiksaan Kursus Semasa Cuti Panjang
Sidang Akademik 1994/5

Jun 1995

CSS201 - Rekabentuk Logik Berdigit

Masa: [3 jam]

ARAHAN KEPADA CALON:

- Sila pastikan bahawa kertas peperiksaan ini mengandungi **LIMA** soalan di dalam **ENAM** muka surat (termasuk lampiran) yang bercetak sebelum anda memulakan peperiksaan ini.
- Jawab **SEMUA** soalan.

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1. Permudahkan fungsi-fungsi berikut dengan menggunakan peta-K.

   (a) $F(a,b,c,d) = \Pi (0,2,5,7, 8, 10, 12,14)$

   (b) $F(w, x, y, z) = \Sigma (0, 5, 6, 12, 15)$
   $d = (8, 9, 10, 11, 14)$

   (c) $F(A, B, C, D) = (A + B + D')(C + D)(B + C + D)(A' + B' + D')(A' + B + C + D) (A' + B + C' + D)$

   (d) $F(v, w, x, y, z) = \Sigma (0, 2, 4, 6, 8, 10, 12, 13, 14, 22, 24, 28, 29, 30)$

(20 markah)

2. Gunakan 1 decoder dan 4 MUX 4x1 untuk membangunkan 1 MUX 16x1.

(20 markah)

3. Implementasikan fungsi di bawah dengan kaedah-kaedah berikut:

$$F = ABC + \bar{A}\bar{C} + \bar{A}BC + A\bar{C}$$

   (a) K-Map

   (b) Persamaan yang dipermudahkan

   (c) Gambarajah Logic.

   (d) Gambarajah Hardware.

(20 markah)

4. Bina suatu carta ASM untuk suatu sistem berdigit yang mengira bilangan peserta di dalam sebuah bilik. Peserta memasuki bilik daripada satu pintu yang mempunyai selfoto ("photocell") yang menukarkan isyarat x daripada 1 kepada 0 apabila terdapat gangguan cahaya. Mereka meninggalkan bilik tersebut melalui pintu kedua, yang mempunyai fotosel dengan isyarat y. Kedua-dua x dan y disegerakkan dengan jam, tetapi ia boleh dibiarkan hidup atau mati lebih daripada satu denyutan-jam ("Both x and y are synchronized with the clock, but they may stay on or off for more than one clock-pulse period").

(20 markah)

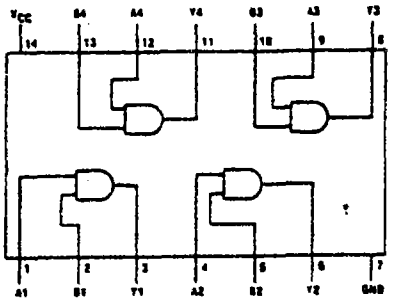
5. Anda dikehendaki membina satu litar pembilang yang akan membilang berulang-ulang dari 0 ke 10, balik ke 0 hingga 10 dan seterusnya. Gunakan cip pengira 74193. Selesaikan sehingga peringkat gambarajah logik sahaja. (Semua input dan output bagi cip pengira 74193 mesti ditunjukkan.)

(20 markah)

Connection Diagram

7432

Dual-In-Line Package

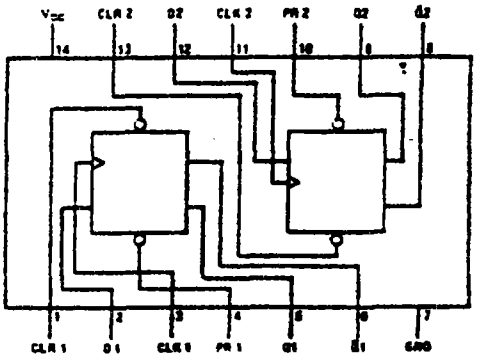


Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N
See NS Package Number J14A, N14A or W14B

Connection Diagram

7474

Dual-In-Line Package



Order Number 5474DMQB, 5474FMQB, DM5474J, DM5474W, DM7474M or DM7474N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going transition of the clock.
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

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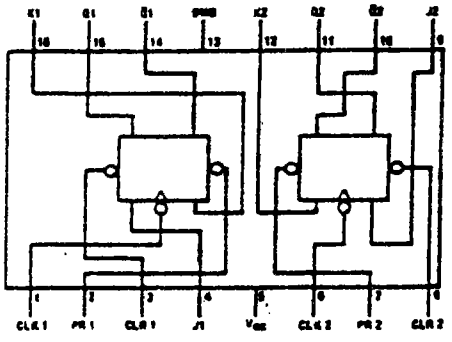
Connection Diagram 7476

Dual-In-Line Package



Order Number 5476DMQB, 5476FMQB,
DM5476J, DM5476W or DM7476N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

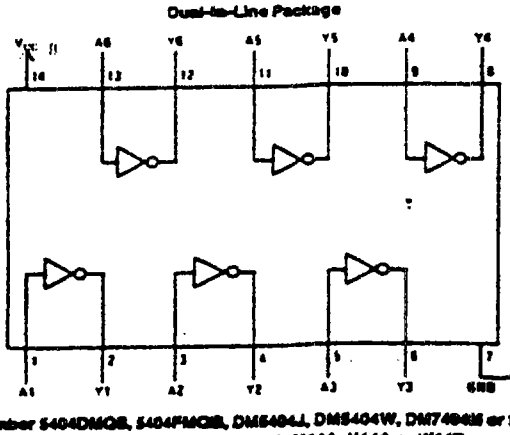
* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Connection Diagram

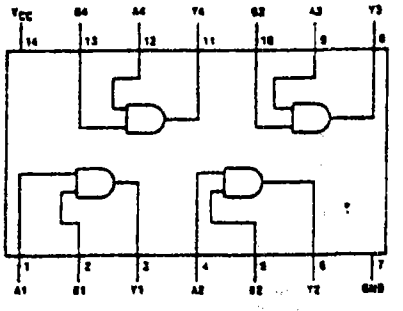
Dual-In-Line Package



Order Number 5404DMQB, 5404FMQB, DM5404J, DM5404W, DM7404M or DM7404N
See NS Package Number J14A, M14A, N14A or W14B

Connection Diagram

Dual-In-Line Package

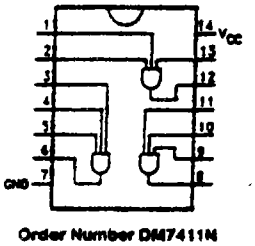


TL/F/6488–1

Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N
See NS Package Number J14A, N14A or W14B

Connection Diagram

Dual-In-Line Package



TL/F/6774–1

Order Number DM7411N
NS Package Number N14A

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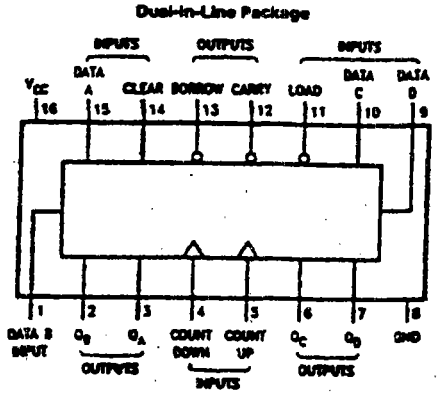
Connection Diagram

Dual-In-Line Package



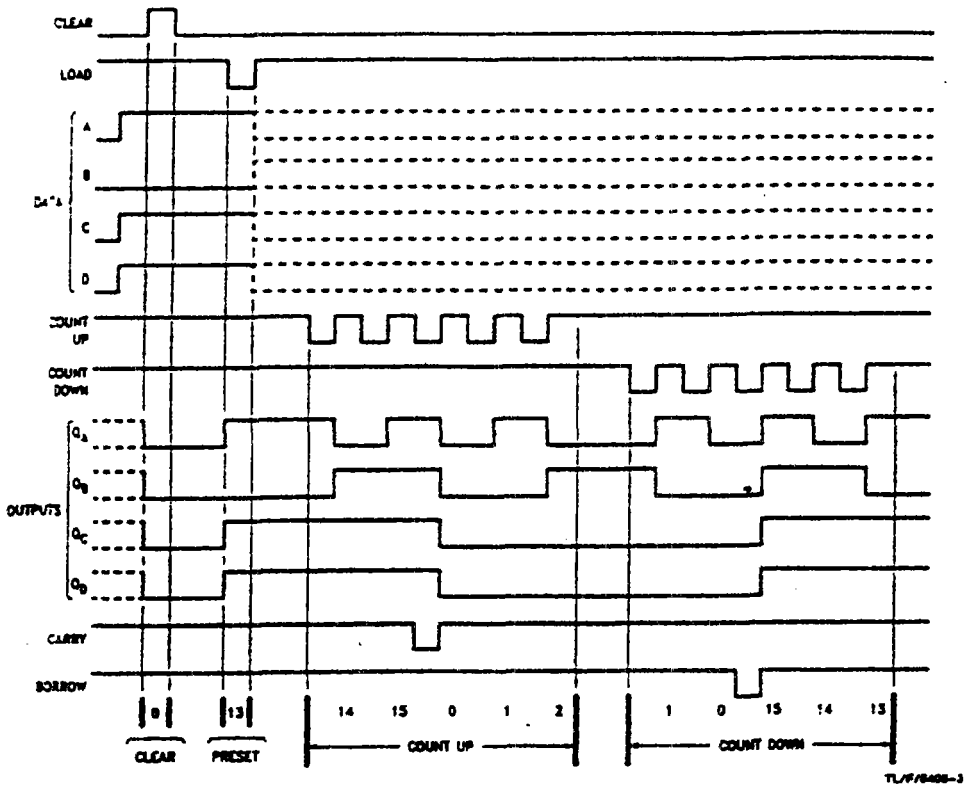
TL/F/6408–1

Order Number 54LS193DMQB, 54LS193FMQB, 54LS193LMQB, DM54LS193J, DM54LS193W, DM74LS193M or DM74LS193N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Timing Diagrams

74193

Typical Clear, Load, and Count Sequences



TL/F/6408–3

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

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