UNIVERSITI SAINS MALAYSIA

First Semester Examination

Academic Session 2003/2004

September/October 2003

EEE 510 – ANALOG INTEGRATED CIRCUIT DESIGN

Time : 3 Hours

INSTRUCTION TO CANDIDATE:-

Please ensure that this examination paper contains **SIXTEEN (16)** printed pages with **6 Appendix** and **SIX (6)** question before answering..

Answer **FIVE (5)** questions.

Distribution of marks for each question is given accordingly.

All questions must be answered in English.

...2/-

1.

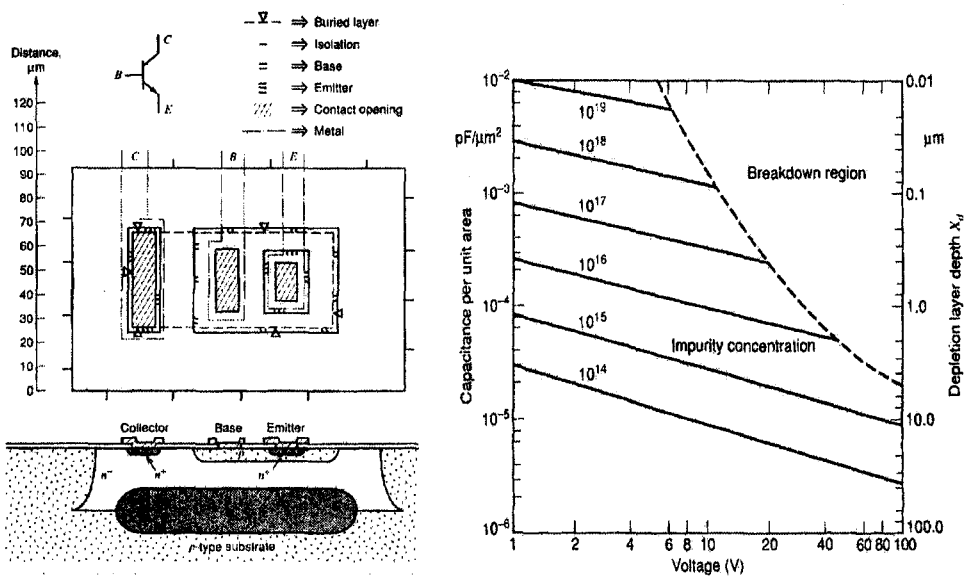


Figure 1

The structure of a high-voltage integrated-circuit npn transistor is shown in plan view and cross section in Figure 1 above. The Emitter Diffusion is 20um X 25um, the Base diffusion is 45um X 60um, and the Base-isolation spacing is 25um. The Collector-Base junction is formed by the diffusion of Boron into an n-type uniformly doped 17um epitaxial material, with resistivity of 5Ω-cm corresponding to an impurity concentration of 10^{15} atoms/cm^3

For Saturation current I_s, where

$$I_S = \frac{qA\bar{D}_n n_i^2}{Q_B} \quad \text{and} \quad \frac{Q_B}{\bar{D}_n} = A\frac{qn_i^2}{I_C}\exp\frac{V_{BE}}{V_T}$$

Q_B is the total number of impurity atoms per unit area in the Base, n_i is the intrinsic carrier concentration, and $\bar{D}_n$ is effective diffusion constant for electrons in the Base of the transistor.

(a) Calculate the Collector-Base capacitance of the device.

(8%)

...3/-

(b) Calculate the zero-bias, Emitter-Base junction capacitance of the device. (7%)

(c) A Base-Emitter voltage of 550mV is measured at a collector current of 10uA on a transistor under test with a 100um X 100um Emitter area. Determine Q_B at 27°C for $n_i = 1.5X10^{10}cm^{-3}$ and the electron diffusivity is $13cm^2s^{-1}$.

(5%)

2. Derive the complete small signal model as shown in Figure 2 for NMOS transistor with I_D= 100uA, V_{SB} = 1V, V_{DS}= 2V. Device parameters are φ_f = 0.3V, W = 10um, L = 1um, γ = $0.5V^{1/2}$, k' = $200uA/V^2$, λ = $0.02V^{-1}$, t_{ox} = 100angstroms, ψ_o = 0.6V, C_{sbo} = C_{dbo}, = 10fF. Overlap capacitance from gate to source and gate to drain is 1fF. Assume C_{gb} = 5fF. Also determine the frequency response of the model.

(20%)

MOSFET Parameters

Text Symbol	Description
V_t	Threshold voltage with zero source-substrate voltage
$k' = \mu C_{ox}$	Transconductance parameter
$\gamma = \frac{\sqrt{2q\epsilon N_A}}{C_{ox}}$	Threshold voltage parameter
$2\phi_f$	Surface potential
$\lambda = \frac{1}{L_{\text{eff}}}\frac{dX_d}{dV_{DS}}$	Channel-length modulation parameter
C_{ol}	Gate-source overlap capacitance per unit channel width
C_{ol}	Gate-drain overlap capacitance per unit channel width

...4/-

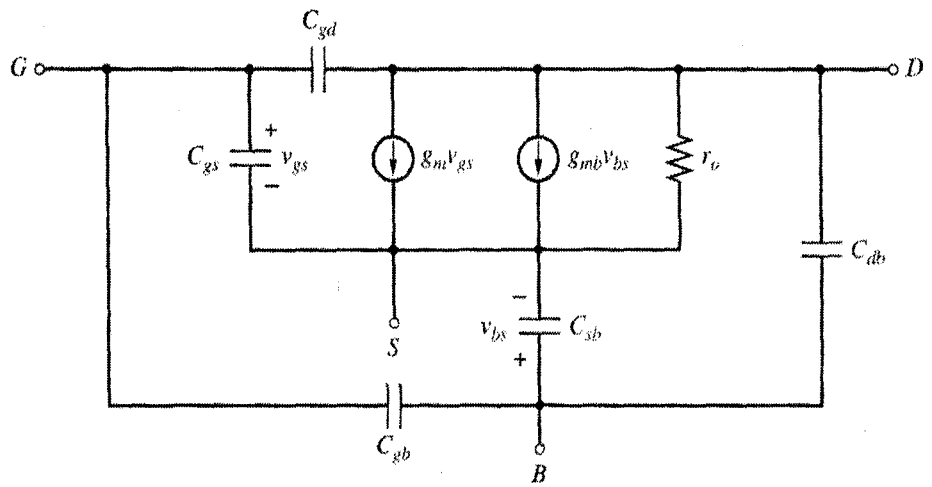


Figure 2

3.

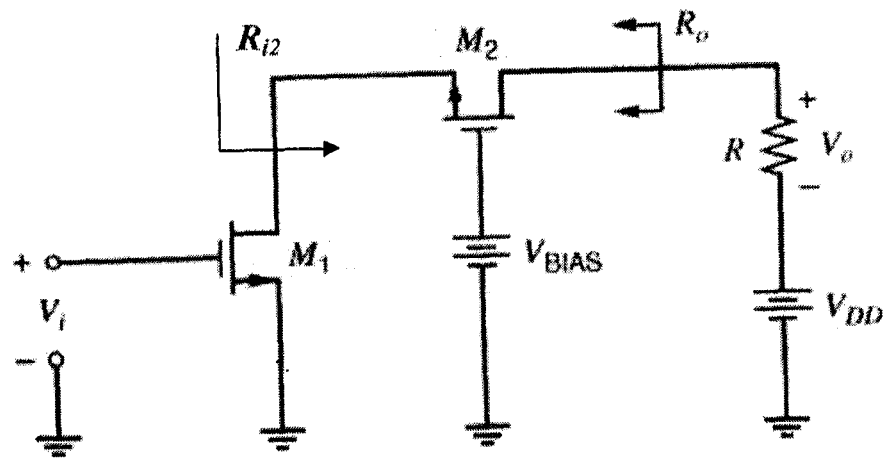


Figure 3

Figure 3 above shows a cascode amplifier of CS-CG configuration,

(a) [i] Find the small signal equivalent circuit for the MOS transistor cascode connection.

(5%)

...5/-

[ii] Derive and show that the circuit transconductance $G_m \approx g_m$ and $R_o \approx (g_{m2}+g_{mb2}) r_{01} r_{02}$.

(5%)

[iii] Show and explain that for R_{i2}, the resistance looking in the source of M_2 can be defined as,

$$R_{i2} \approx \frac{1}{g_{m2} + g_{mb2}} + \frac{R}{(g_{m2} + g_{mb2})\, r_{o2}}$$

(5%)

(b) Calculate the transconductance and output resistance of the circuit with assumption that both transistors operate in the active region with g_m = 1mA/V, internal gain $\chi = g_{mb}/g_m = 0.1$, and r_o = 20KΩ. What do you find by comparing between the results and the approximation made in (b)?

(5%)

...6/-

4.

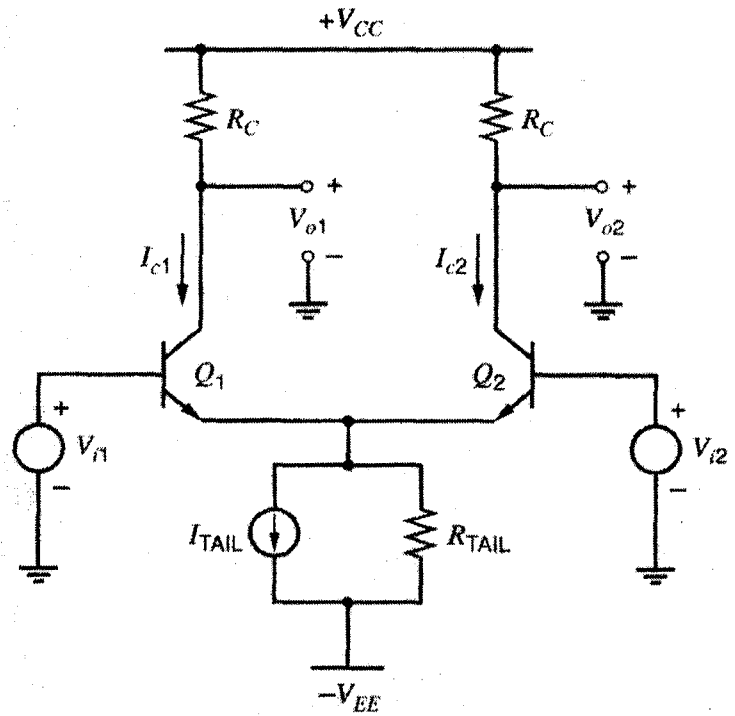


Figure 4

For the small-signal analysis of differential amplifier in Figure 4, show that for given voltage gains,

...7/-

$$A_{11} = \left.\frac{v_{o1}}{v_{i1}}\right|_{v_{i2}=0}$$

$$A_{12} = \left.\frac{v_{o1}}{v_{i2}}\right|_{v_{i1}=0}$$

$$A_{21} = \left.\frac{v_{o2}}{v_{i1}}\right|_{v_{i2}=0}$$

$$A_{22} = \left.\frac{v_{o2}}{v_{i2}}\right|_{v_{i1}=0}$$

(a) Define and derive: the differential-mode gain A_{dm}, common-mode gain A_{cm}, differential-mode-to-common-mode gain $A_{dm\text{-}cm}$, common-mode-to-differential-mode gain $A_{cm\text{-}dm}$.

(10%)

(b) Show that the common-mode rejection ratio CMRR is define by;

$$\frac{A_{11} - A_{12} - A_{21} + A_{22}}{A_{11} + A_{12} + A_{21} + A_{22}}$$

(3%)

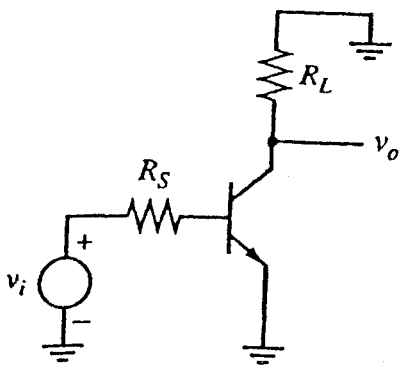
(c) Explain the reason for designing a ***Perfect Symmetry Balanced Differential Amplifier*** by giving a quantitative representation of its figure of merit.

(7%)

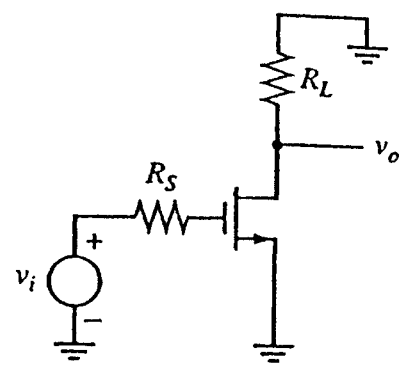
...8/-

5. (a) Use the Miller approximation to calculate the – 3-dB frequency of the small-signal voltage gain of a common-emitter transistor stage as shown in Figure 5(a) using $R_S = 5k\Omega$, $R_L = 3k\Omega$, and the following transistor parameters:

$r_b = 300\,\Omega$, $I_C = 0.5mA$, $\beta = 200$, $f_T = 500MHz$ (*at* $I_C = 0.5mA$),
$C_\mu = 0.3pF$, $C_{CS} = 0$, *and* $V_A = \infty$



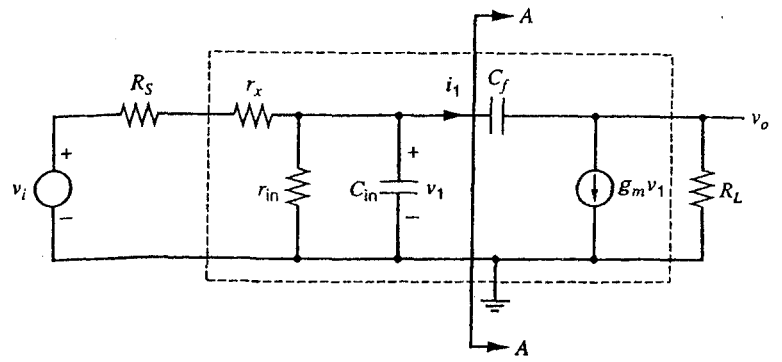
(a) An ac schematic of a common-emitter amplifier



(b) An ac schematic of a common-source amplifier

(8 %)

...9/-



(c) A general model for both amplifiers

(b) The ac schematic of a shunt-shunt feed-back amplifier is shown in Figure 6. All transistors have $I_D = 1\,mA, W/L = 100, k' = 60\mu A/V^2$, and $\lambda = 1/(50\,V)$.

(6 %)

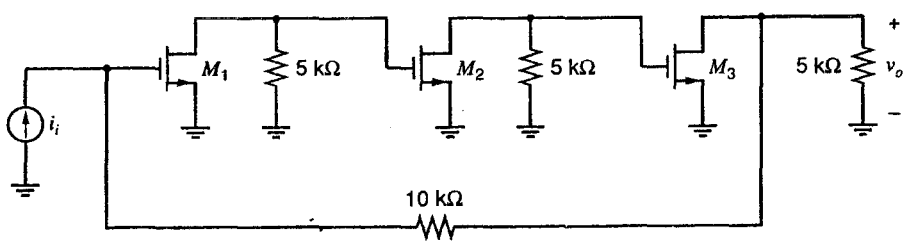


Figure 6 : An ac schematic of a shunt-shunt feedback amplifier

(c) Calculate the overall gain v_o/i_i, the loop transmission, the input impedance, and the output impedance at low frequencies. Use the formulas from two-port analysis (see Appendix).

(6 %)

...10/-

6. An amplifier has a low-frequency forward gain of 5000 and its transfer function has three negative real poles with magnitudes 300 kHz, 2 MHz, and 25 MHz.

(a) Calculate the dominant-pole magnitude required to give unity-gain compensation of this amplifier with a 45° phase margin if the original amplifier poles remain fixed. What is the resulting bandwidth of the circuit with the feedback applied?

(10%)

(b) Repeat (a) for compensation in a feedback loop with a forward gain of 20 dB and 45° phase margin.

(10%)

- oo0oo -

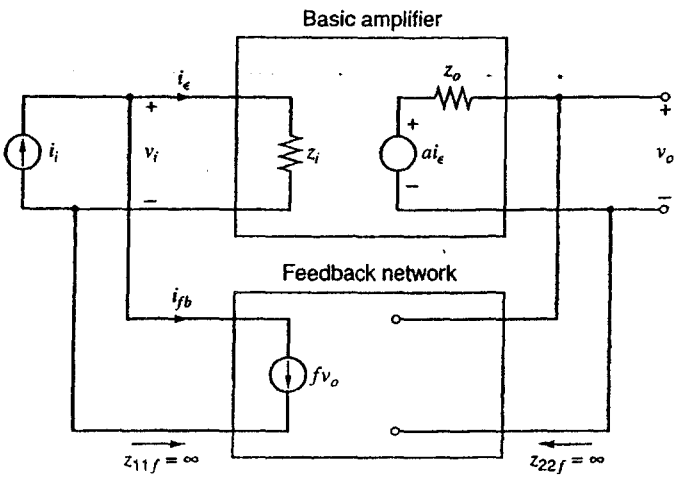


Figure 8.9 Shunt-shunt feedback configuration.

8.5 Practical Configurations and the Effect of Loading

In practical feedback amplifiers, the feedback network causes loading at the input and output of the basic amplifier, and the division into basic amplifier and feedback network is not as obvious as the above treatment implies. In such cases, the circuit can always be analyzed by writing circuit equations for the whole amplifier and solving for the transfer function and terminal impedances. However, this procedure becomes very tedious and difficult in most practical cases, and the equations so complex that one loses sight of the important aspects of circuit performance. Thus it is profitable to identify a basic amplifier and feedback network in such cases and then to use the ideal feedback equations derived above. In general it will be necessary to include the loading effect of the feedback network on the basic amplifier, and methods of including this loading in the calculations are now considered. The *method* will be developed through the use of two-port representations of the circuits involved, although this method of representation is not necessary for practical calculations, as we will see.

8.5.1 Shunt-Shunt Feedback

Consider the shunt-shunt feedback amplifier of Fig. 8.9. The effect of nonideal networks may be included as shown in Fig. 8.13*a*, where finite input and output admittances are assumed in both forward and feedback paths, as well as reverse transmission in each. Finite source and load admittances y_S and y_L are assumed. The most convenient two-port

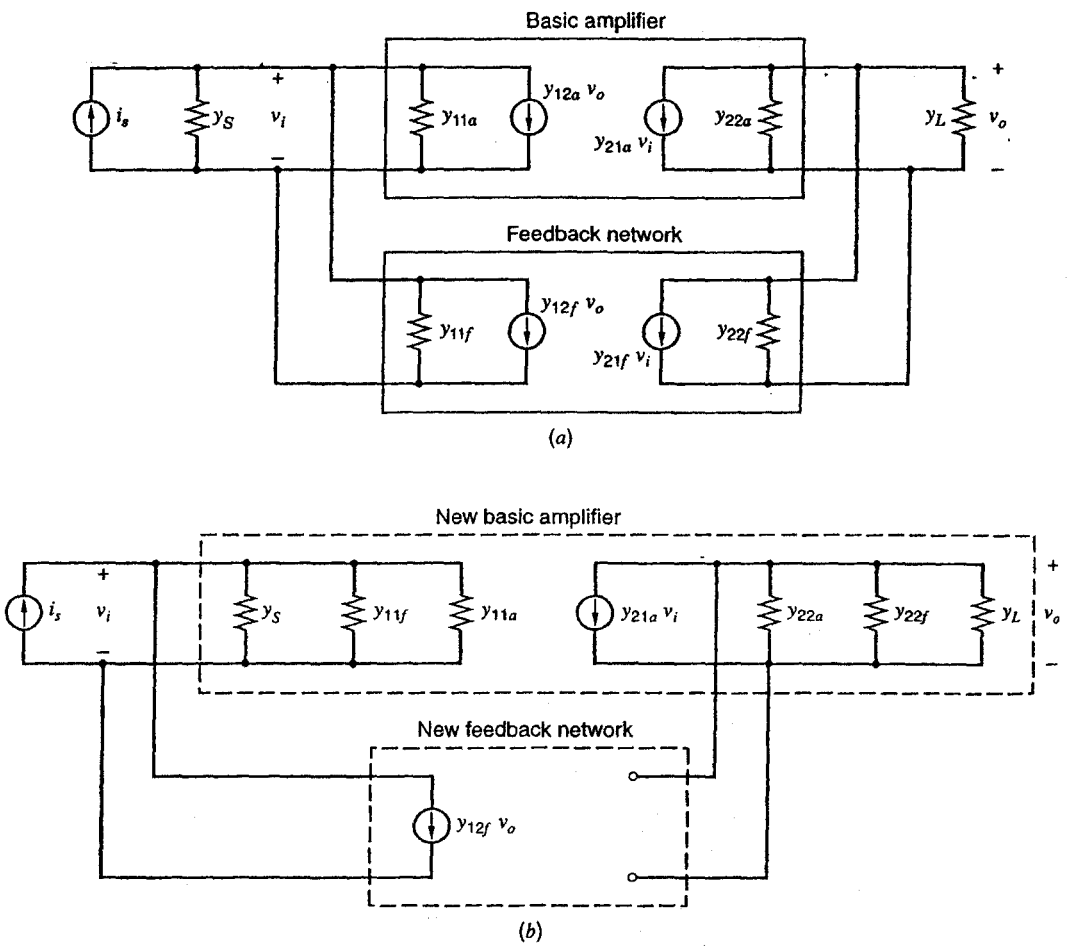


Figure 8.13 (*a*) Shunt-shunt feedback configuration using the *y*-parameter representation. (*b*) Circuit of (*a*) redrawn with generators $y_{21f}v_i$ and $y_{12a}v_o$ omitted.

representation in this case is the short-circuit admittance parameters or *y* parameters,[1] as used in Fig. 8.13*a*. The reason for this is that the basic amplifier and the feedback network are connected in parallel at input and output, and thus have identical *voltages* at their terminals. The *y* parameters specify the response of a network by expressing the terminal currents in terms of the terminal voltages, and this results in very simple calculations when two networks have identical terminal voltages. This will be evident in the circuit calculations to follow. The *y*-parameter representation is illustrated in Fig. 8.14.

From Fig. 8.13*a*, at the input

$$i_s = (y_S + y_{11a} + y_{11f})v_i + (y_{12a} + y_{12f})v_o \tag{8.46}$$

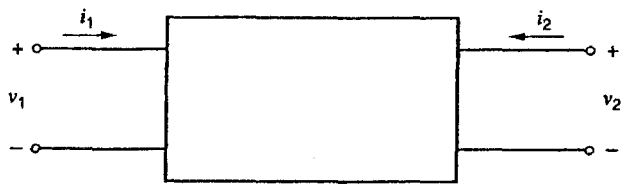
Summation of currents at the output gives

$$0 = (y_{21a} + y_{21f})v_i + (y_L + y_{22a} + y_{22f})v_o \tag{8.47}$$

It is useful to define

$$y_i = y_S + y_{11a} + y_{11f} \tag{8.48}$$

$$y_o = y_L + y_{22a} + y_{22f} \tag{8.49}$$



$$i_1 = y_{11} v_1 + y_{12} v_2$$
$$i_2 = y_{21} v_1 + y_{22} v_2$$

$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2 = 0} \qquad y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1 = 0}$$

$$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2 = 0} \qquad y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1 = 0}$$

Figure 8.14 The y-parameter representation of a two-port.

Solving (8.46) and (8.47) by using (8.48) and (8.49) gives

$$\frac{v_o}{i_s} = \frac{-(y_{21a} + y_{21f})}{y_i y_o - (y_{21a} + y_{21f})(y_{12a} + y_{12f})} \tag{8.50}$$

The equation can be put in the form of the ideal feedback equation of (8.35) by dividing by $y_i y_o$ to give

$$\frac{v_o}{i_s} = \frac{\dfrac{-(y_{21a} + y_{21f})}{y_i y_o}}{1 + \dfrac{-(y_{21a} + y_{21f})}{y_i y_o}(y_{12a} + y_{12f})} \tag{8.51}$$

Comparing (8.51) with (8.35) gives

$$a = -\frac{y_{21a} + y_{21f}}{y_i y_o} \tag{8.52}$$

$$f = y_{12a} + y_{12f} \tag{8.53}$$

At this point, a number of approximations can be made that greatly simplify the calculations. First, we assume that the signal transmitted by the basic amplifier is much greater than the signal fed forward by the feedback network. Since the former has gain (usually large) while the latter has loss, this is almost invariably a valid assumption. This means that

$$|y_{21a}| \gg |y_{21f}| \tag{8.54}$$

Second, we assume that the signal fed back by the feedback network is much greater than the signal fed back through the basic amplifier. Since most active devices have very small reverse transmission, the basic amplifier has a similar characteristic, and this assumption is almost invariably quite accurate. This assumption means that

$$|y_{12a}| \ll |y_{12f}| \tag{8.55}$$

Using (8.54) and (8.55) in (8.51) gives

$$\frac{v_o}{i_s} = A \simeq \frac{\dfrac{-y_{21a}}{y_i y_o}}{1 + \left(\dfrac{-y_{21a}}{y_i y_o}\right) y_{12f}} \tag{8.56}$$

Comparing (8.56) with (8.35) gives

$$a = -\frac{y_{21a}}{y_i y_o} \tag{8.57}$$

$$f = y_{12f} \tag{8.58}$$

A circuit representation of (8.57) and (8.58) can be found as follows. Equations 8.54 and 8.55 mean that in Fig. 8.13*a* the feedback generator of the basic amplifier and the forward-transmission generator of the feedback network may be neglected. If this is done the circuit may be redrawn as in Fig. 8.13*b*, where the terminal admittances y_{11f} and y_{22f} of the feedback network have been absorbed into the basic amplifier, together with source and load impedances y_S and y_L. The new basic amplifier thus *includes the loading effect* of the original feedback network, and the new feedback network is an ideal one as used in Fig. 8.9. If the transfer function of the basic amplifier of Fig. 8.13*b* is calculated (by first removing the feedback network), the result given in (8.57) is obtained. Similarly, the transfer function of the feedback network of Fig. 8.13*b* is given by (8.58). Thus Fig. 8.13*b* is a *circuit representation* of (8.57) and (8.58).

Since Fig. 8.13*b* has a direct correspondence with Fig. 8.9, all the results derived in Section 8.4.2 for Fig. 8.9 can now be used. The loading effect of the feedback network on the basic amplifier is now included by simply shunting input and output with y_{11f} and y_{22f}, respectively. As shown in Fig. 8.14, these terminal admittances of the feedback network are calculated with the other port of the network short-circuited. In practice, loading term y_{11f} is simply obtained by shorting the output node of the amplifier and calculating the feedback circuit input admittance. Similarly, term y_{22f} is calculated by shorting the input node in the amplifier and calculating the feedback circuit output admittance. The feedback transfer function f given by (8.58) is the short-circuit reverse transfer admittance of the feedback network and is defined in Fig. 8.14. This is readily calculated in practice and is often obtained by inspection. Note that the use of y parameters in further calculations is *not* necessary. Once the circuit of Fig. 8.13*b* is established, any convenient network analysis method may be used to calculate gain a of the basic amplifier. We have simply used the two-port representation as a general means of illustrating how loading effects may be included in the calculations.

For example, consider the common shunt-shunt feedback circuit using an op amp as shown in Fig. 8.15*a*. The equivalent circuit is shown in Fig. 8.15*b* and is redrawn in 8.15*c* to allow for loading of the feedback network on the basic amplifier. The y parameters of the feedback network can be found from Fig. 8.15*d*.

$$y_{11f} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = \frac{1}{R_F} \tag{8.59}$$

$$y_{22f} = \left.\frac{i_2}{v_2}\right|_{v_1=0} = \frac{1}{R_F} \tag{8.60}$$

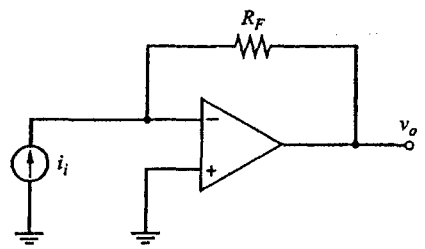
$$y_{12f} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = -\frac{1}{R_F} = f \tag{8.61}$$

Using (8.54), we neglect y_{21f}.

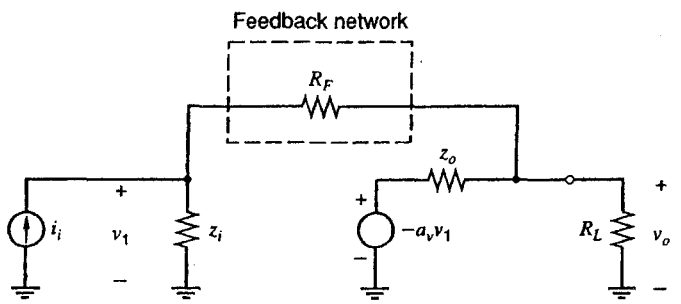
The basic-amplifier gain a can be calculated from Fig. 8.15*c* by putting $i_{fb} = 0$ to give

$$v_1 = \frac{z_i R_F}{z_i + R_F} i_i \tag{8.62}$$

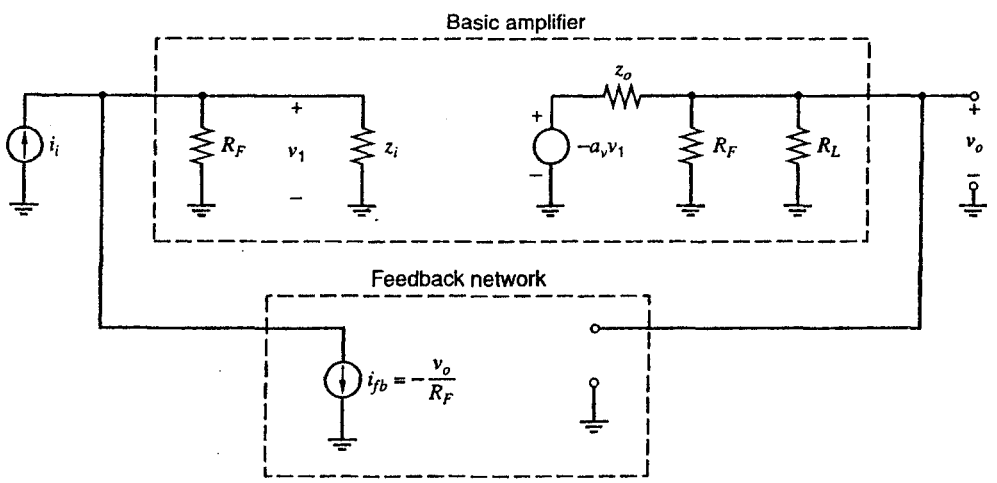
$$v_o = -\frac{R}{R + z_o} a_v v_1 \tag{8.63}$$



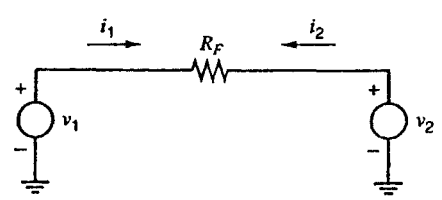
(a)



(b)



(c)



(d)

Figure 8.15 (*a*) Shunt-shunt feedback circuit using an op amp as the gain element. (*b*) Equivalent circuit of (*a*). (*c*) Division of the circuit in (*b*) into forward and feedback paths. (*d*) Circuit for the calculation of the *y* parameters of the feedback network of the circuit in (*b*).

where

$$R = R_F \| R_L \tag{8.64}$$

Substituting (8.62) in (8.63) gives

$$\frac{v_o}{i_i} = a = -\frac{R}{R + z_o} a_v \frac{z_i R_F}{z_i + R_F} \tag{8.65}$$

Using the formulas derived in Section 8.4.2 we can now calculate all parameters of the feedback circuit. The input and output impedances of the basic amplifier now *include* the effect of feedback loading, and it is *these impedances* that are divided by $(1 + T)$ as described in Section 8.4.2. Thus the input impedance of the basic amplifier of Fig. 8.15*c* is

$$z_{ia} = R_F \| z_i = \frac{R_F z_i}{R_F + z_i} \tag{8.66}$$

When feedback is applied, the input impedance is

$$Z_i = \frac{z_{ia}}{1 + T} \tag{8.67}$$

Similarly for the output impedance of the basic amplifier

$$z_{oa} = z_o \| R_F \| R_L \tag{8.68}$$

When feedback is applied, this becomes

$$Z_o = \frac{z_o \| R_F \| R_L}{1 + T} \tag{8.69}$$

Note that these calculations can be made using the circuit of Fig. 8.15*c* *without* further need of two-port y parameters.

Since the loop gain T is of considerable interest, this is now calculated using (8.61) and (8.65):

$$T = af = \frac{R_F R_L}{R_F R_L + z_o R_F + z_o R_L} a_v \frac{z_i}{z_i + R_F} \tag{8.70}$$

230a