
UNIVERSITI SAINS MALAYSIA

Semester I Examination
Academic Session 2005/2006

November 2005

EEE 510 – ADVANCED ANALOGUE CIRCUIT DESIGN

Time : 3 hours

INSTRUCTION TO CANDIDATE:

Please ensure that this examination paper contains **NINE (9)** printed pages including Appendices (8 pages) and **ONE (1)** page **FINAL ANSWERING FORMAT (FOJA)** and **SIX (6)** questions before answering.

This question paper has two sections, **Section A** and **Section B**.

Answer **TWO (2)** questions in **Section A** and **TWO (2)** questions in **Section B** and **ONE (1)** question from any **Section**. Answer **FIVE (5)** questions.

The **Answering Format** for this examination is

- [i] You are required to show all the working solution in **Answer Booklet**.
- [ii] All the final answers to each questions [**B4, B5, B6**] must be fulfilled in final answer format paper (FOJA) which is provided and **must be enclosed together with your Answer Booklet**.

Use two separate answer booklets which are provided for answering questions in **Section A** and **Section B** respectively.

Distribution of marks for each question is given accordingly.

All questions must be answered in English.

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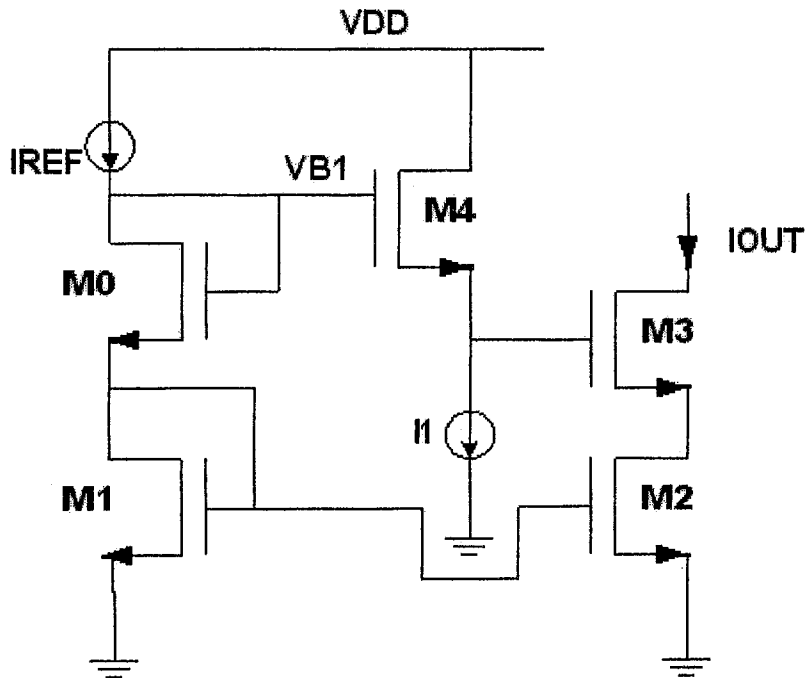


Figure 3

A2. In the circuit shown in Figure 3 a source follower using a wide transistor and a small bias current is inserted in series with the gate of M3 so as to bias M2 at the edge of saturation region. Assuming M0-M3 are identical and $\lambda \neq 0$, estimate the mismatch between I_{OUT} and I_{REF} if

- (a) $\gamma = 0$ (50%)
- (b) $\gamma \neq 0$ (50%)

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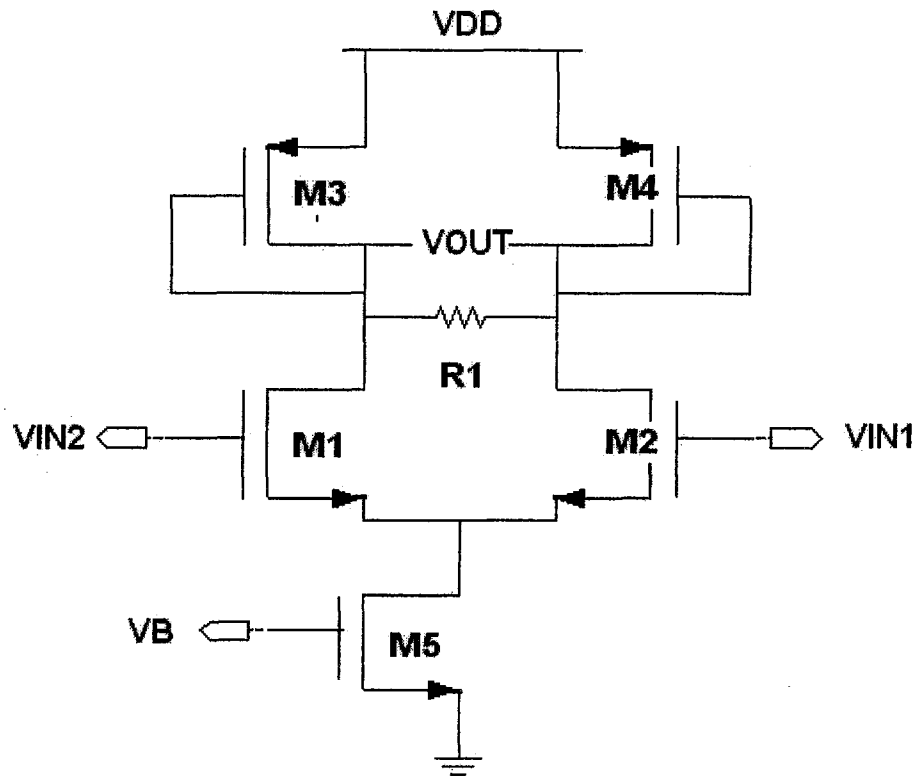


Figure 4

A3. Assuming all of the circuits shown in Figure 3 are symmetric sketch V_{OUT} :

(a) V_{IN1} and V_{IN2} vary differentially from zero to V_{DD} (50%)

(b) V_{IN1} and V_{IN2} are equal and vary from zero to V_{DD} (50%)

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Section B: Answer TWO (2) question

B4. If there are no dominant zeros in the circuit transfer function and if there is a dominant pole p_1 , then ω_{-3dB} frequency is given by

$$\omega_{-3dB} \approx |p_1| \approx \frac{1}{b_1} = \frac{1}{\sum T_{0}}$$

where $\sum T_{0}$ is the sum of the zero value time constants. (see Appendix A for details). Calculate the -3 -dB frequency of the circuit of Figure 4, assuming the following parameter values:

$R_S = 10k\Omega$	$R_{L1} = 10k\Omega$	$R_{L2} = 5k\Omega$
$C_{gs1} = 5 \text{ pF}$	$C_{gs2} = 10 \text{ pF}$	$C_{gd1} = C_{gd2} = 1 \text{ pF}$
$C_{db1} = C_{db2} = 2 \text{ pF}$	$g_{m1} = 3 \text{ mA/V}$	$g_{m2} = 6 \text{ mA/V}$

Ignore C_{gb} (which is in parallel with C_{gs} and is much smaller than C_{gs}). The small-signal equivalent circuit of Figure 4(a) is shown in Figure 4(b). Use the zero-value time constants method in your calculation.

(100%)

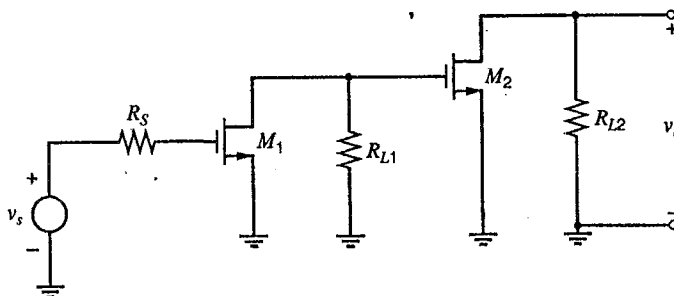


Figure 4(a) Two-stage, common-source cascade amplifier.

Figure 4(a)

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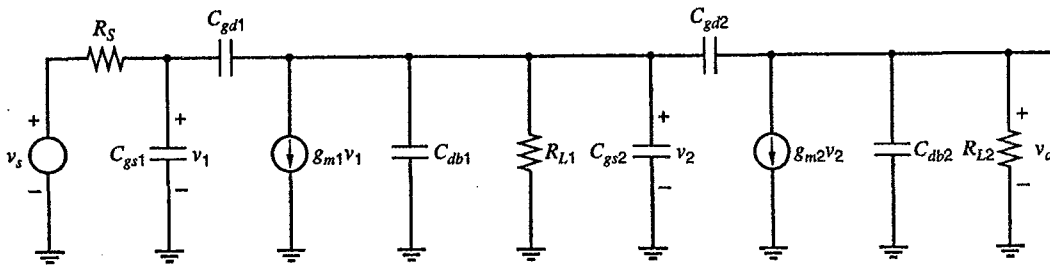


Figure 4(b)

- B5. (a) Figure 5(a) is a single-stage feedback circuit. Its small-signal model is shown in Figure 5(b), which includes a dependent current source. Find the return ratio.

Use the following parameter values.

$$r_{\pi} = 5 \text{ k}\Omega$$

$$R_F = 19.5 \text{ k}\Omega$$

$$R_C = 10 \text{ k}\Omega$$

$$g_m = 40 \frac{\text{mA}}{\text{V}}$$

$$r_o = 1 \text{ M}\Omega$$

(50%)

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- B6. The simplest and the most common method of compensation is to reduce the bandwidth of the amplifier which is often called narrow banding (see Appendix B).

The low-frequency gain of the 702 op amp is $a_0=3600$ and the circuit has poles at $-(p_1/2\pi) = 1$ mHZ, $-(p_2/2\pi) = 4$ mHz and $-(p_3/2\pi) = 40$ mHZ. Calculate the dominant-pole magnitude required to give unity-gain compensation for this 702 op amp with a phase margin of 45° .

(100%)

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7.3 Multistage Amplifier Frequency Response

The above analysis of the frequency behavior of single-stage circuits indicates the complexity that can arise even with simple circuits. The complete analysis of the frequency response of multistage circuits with many capacitive elements rapidly becomes very difficult and the answers become so complicated that little use can be made of the results. For this reason approximate methods of analysis have been developed to aid in the circuit design phase, and computer simulation is used to verify the final design. One such method of analysis is the *zero-value time constant* analysis that will now be described. First some ideas regarding dominant poles are developed.

7.3.1 Dominant-Pole Approximation

For any electronic circuit we can derive a transfer function $A(s)$ by small-signal analysis to give

$$A(s) = \frac{N(s)}{D(s)} = \frac{a_0 + a_1s + a_2s^2 + \cdots + a_ms^m}{1 + b_1s + b_2s^2 + \cdots + b_ns^n} \quad (7.83)$$

where a_0, a_1, \dots, a_m , and b_1, b_2, \dots, b_n are constants. Very often the transfer function contains poles only (or the zeros are unimportant). In this case we can factor the denominator of (7.83) to give

$$A(s) = \frac{K}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)\cdots\left(1 - \frac{s}{p_n}\right)} \quad (7.84)$$

where K is a constant and p_1, p_2, \dots, p_n are the poles of the transfer function. It is apparent from (7.84) that

$$b_1 = \sum_{i=1}^n \left(-\frac{1}{p_i}\right) \quad (7.85)$$

An important practical case occurs when one pole is dominant. That is, when

$$|p_1| \ll |p_2|, |p_3|, \dots \quad \text{so that} \quad \left|\frac{1}{p_1}\right| \gg \left|\sum_{i=2}^n \left(-\frac{1}{p_i}\right)\right|$$

This situation is shown in the s plane in Fig. 7.23 and in this case it follows from (7.85) that

$$b_1 \approx \left|\frac{1}{p_1}\right| \quad (7.86)$$

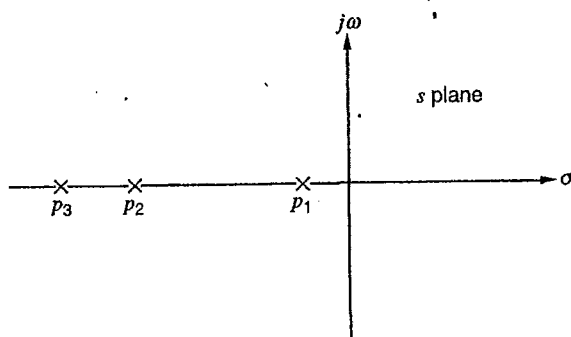


Figure 7.23 Pole diagram for a circuit with a dominant pole.

If we return now to (7.84) and calculate the gain magnitude in the frequency domain, we obtain

$$|A(j\omega)| = \frac{K}{\sqrt{\left[1 + \left(\frac{\omega}{p_1}\right)^2\right] \left[1 + \left(\frac{\omega}{p_2}\right)^2\right] \cdots \left[1 + \left(\frac{\omega}{p_n}\right)^2\right]}} \quad (7.87)$$

If a dominant pole exists, then (7.87) can be approximated by

$$|A(j\omega)| \approx \frac{K}{\sqrt{1 + \left(\frac{\omega}{p_1}\right)^2}} \quad (7.88)$$

This approximation will be quite accurate at least until $\omega \approx |p_1|$, and thus (7.88) will accurately predict the -3-dB frequency and we can write

$$\omega_{-3dB} \approx |p_1| \quad (7.89)$$

Use of (7.86) in (7.89) gives

$$\omega_{-3dB} \approx \frac{1}{b_1} \quad (7.90)$$

for a dominant-pole situation.

7.3.2 Zero-Value Time Constant Analysis

This is an approximate method of analysis that allows an estimate to be made of the dominant pole (and thus the -3-dB frequency) of complex circuits. Considerable saving in computational effort is achieved because a full analysis of the circuit is not required. The method will be developed by considering a practical example.

Consider the equivalent circuit shown in Fig. 7.24. This is a single-stage bipolar transistor amplifier with resistive source and load impedances. The feedback capacitance is split into two parts (C_x and C_μ) as shown. This is a slightly better approximation to the actual situation than the single collector-base capacitor we have been using, but is rarely used in hand calculations because of the analysis complexity. For purposes of analysis, the

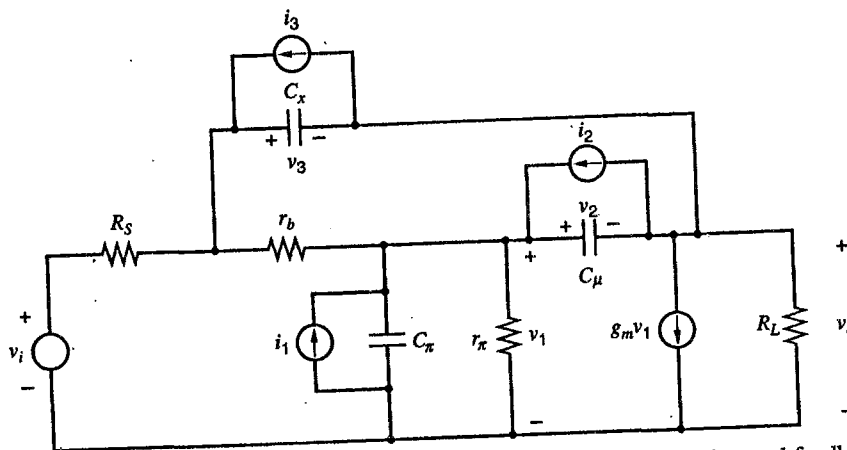


Figure 7.24 Small-signal equivalent circuit of a common-emitter stage with internal feedback capacitors C_μ and C_x .

capacitor voltages v_1 , v_2 , and v_3 are chosen as variables. The external input v_i is removed and the circuit excited with three independent current sources i_1 , i_2 , and i_3 across the capacitors, as shown in Fig. 7.24. We can show that with this choice of variables the circuit equations are of the form

$$i_1 = (g_{11} + sC_\pi)v_1 + g_{12}v_2 + g_{13}v_3 \quad (7.91)$$

$$i_2 = g_{21}v_1 + (g_{22} + sC_\mu)v_2 + g_{23}v_3 \quad (7.92)$$

$$i_3 = g_{31}v_1 + g_{32}v_2 + (g_{33} + sC_x)v_3 \quad (7.93)$$

where the g terms are conductances. Note that the terms involving s contributed by the capacitors are associated only with their respective capacitor voltage variables and only appear on the diagonal of the system determinant.

The poles of the circuit transfer function are the zeros of the determinant Δ of the circuit equations, which can be written in the form

$$\Delta(s) = K_3s^3 + K_2s^2 + K_1s + K_0 \quad (7.94)$$

where the coefficients K are composed of terms from the above equations. For example, K_3 is the sum of the coefficients of all terms involving s^3 in the expansion of the determinant. Equation 7.94 can be expressed as

$$\Delta(s) = K_0(1 + b_1s + b_2s^2 + b_3s^3) \quad (7.95)$$

where this form corresponds to (7.83). Note that this is a third-order determinant because there are three capacitors in the circuit. The term K_0 in (7.94) is the value of $\Delta(s)$ if all capacitors are zero ($C_x = C_\mu = C_\pi = 0$). This can be seen from (7.91), (7.92), and (7.93). Thus

$$K_0 = \Delta|_{C_\pi=C_\mu=C_x=0}$$

and it is useful to define

$$K_0 \triangleq \Delta_0 \quad (7.96)$$

Consider now the term K_1s in (7.94). This is the sum of all the terms involving s that are obtained when the system determinant is evaluated. However, from (7.91) to (7.93) it is apparent that s only occurs when associated with a capacitance. Thus the term K_1s can be written as

$$K_1s = h_1sC_\pi + h_2sC_\mu + h_3sC_x \quad (7.97)$$

where the h terms are constants. The term h_1 can be evaluated by expanding the determinant of (7.91) to (7.93) about the first row:

$$\Delta(s) = (g_{11} + sC_\pi)\Delta_{11} + g_{12}\Delta_{12} + g_{13}\Delta_{13} \quad (7.98)$$

where Δ_{11} , Δ_{12} , and Δ_{13} are cofactors of the determinant. Inspection of (7.91), (7.92), and (7.93) shows that C_π occurs only in the first term of (7.98). Thus the coefficient of $C_\pi s$ in (7.98) is found by evaluating Δ_{11} with $C_\mu = C_x = 0$, which will eliminate the other capacitive terms in Δ_{11} . But this coefficient of $C_\pi s$ is just h_1 in (7.97), and so

$$h_1 = \Delta_{11}|_{C_\mu=C_x=0} \quad (7.99)$$

Now consider expansion of the determinant about the second row. This must give the same value for the determinant, and thus

$$\Delta(s) = g_{21}\Delta_{21} + (g_{22} + sC_\mu)\Delta_{22} + g_{23}\Delta_{23} \quad (7.100)$$

In this case C_μ occurs only in the second term of (7.100). Thus the coefficient of $C_\mu s$ in this equation is found by evaluating Δ_{22} with $C_\pi = C_x = 0$, which will eliminate the other capacitive terms. This coefficient of $C_\mu s$ is just h_2 in (7.97), and thus

$$h_2 = \Delta_{22}|_{C_\pi=C_x=0} \quad (7.101)$$

Similarly by expanding about the third row it follows that

$$h_3 = \Delta_{33}|_{C_\pi=C_\mu=0} \quad (7.102)$$

Combining (7.97) with (7.99), (7.101), and (7.102) gives

$$K_1 = (\Delta_{11}|_{C_\mu=C_x=0} \times C_\pi) + (\Delta_{22}|_{C_\pi=C_x=0} \times C_\mu) + (\Delta_{33}|_{C_\mu=C_\pi=0} \times C_x) \quad (7.103)$$

and

$$b_1 = \frac{K_1}{K_0} = \frac{\Delta_{11}|_{C_\mu=C_x=0}}{\Delta_0} \times C_\pi + \frac{\Delta_{22}|_{C_\pi=C_x=0}}{\Delta_0} \times C_\mu + \frac{\Delta_{33}|_{C_\mu=C_\pi=0}}{\Delta_0} \times C_x \quad (7.104)$$

where the boundary conditions on the determinants are the same as in (7.103). Now consider putting $i_2 = i_3 = 0$ in Fig. 7.24. Solving (7.91) to (7.93) for v_1 gives

$$v_1 = \frac{\Delta_{11} i_1}{\Delta(s)}$$

and thus

$$\frac{v_1}{i_1} = \frac{\Delta_{11}}{\Delta(s)} \quad (7.105)$$

Equation 7.105 is an expression for the driving-point impedance at the C_π node pair. Thus

$$\frac{\Delta_{11}|_{C_\mu=C_x=0}}{\Delta_0}$$

is the driving-point *resistance* at the C_π node pair with *all* capacitors equal to zero because

$$\frac{\Delta_{11}|_{C_\mu=C_x=0}}{\Delta_0} = \frac{\Delta_{11}}{\Delta} \Big|_{C_\mu=C_x=C_\pi=0} \quad (7.106)$$

We now define

$$R_{\pi 0} = \frac{\Delta_{11}}{\Delta_0} \Big|_{C_\mu=C_x=0} \quad (7.107)$$

Similarly,

$$\frac{\Delta_{22}|_{C_\pi=C_x=0}}{\Delta_0}$$

is the driving-point *resistance* at the C_μ node pair with all capacitors put equal to zero and is represented by $R_{\mu 0}$. Thus we can write from (7.104)

$$b_1 = R_{\pi 0} C_\pi + R_{\mu 0} C_\mu + R_{x 0} C_x \quad (7.108)$$

The time constants in (7.108) are called *zero-value time constants* because all capacitors are set equal to zero to perform the calculation. Although derived in terms of a specific

9.4 Compensation

9.4.1 Theory of Compensation

Consider again the amplifier whose gain and phase is shown in Fig. 9.8. For the feedback circuit in which this was assumed to be connected, the forward gain was A_0 , as shown in Fig. 9.8, and the phase margin was positive. Thus the circuit was stable. It is apparent, however, that if the amount of feedback is increased by making f larger (and thus A_0 smaller), oscillation will eventually occur. This is shown in Fig. 9.11, where f_1 is chosen to give a zero phase margin and the corresponding overall gain is $A_1 \approx 1/f_1$. If the feedback

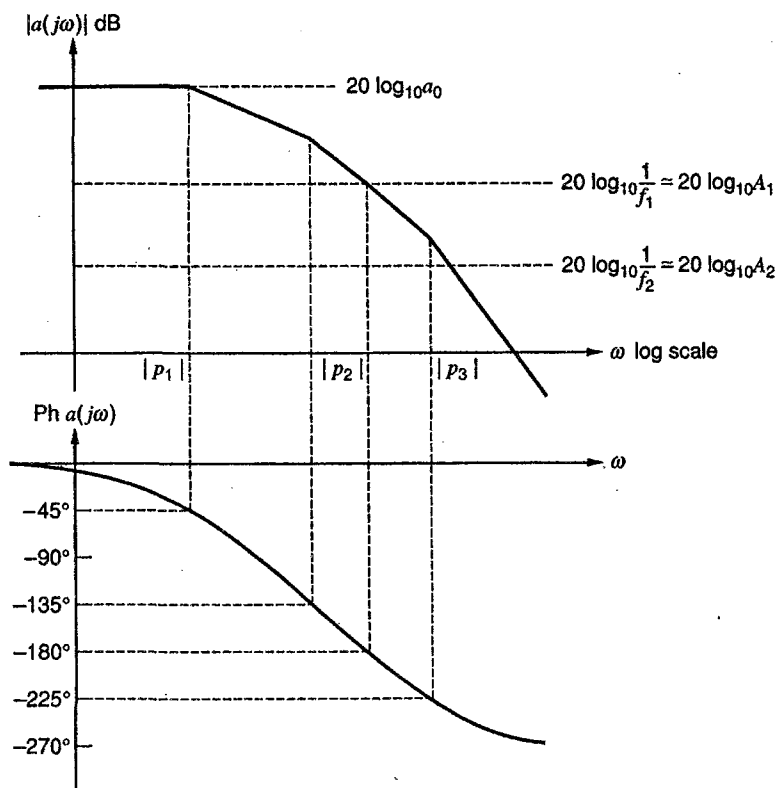


Figure 9.11 Gain and phase versus frequency for a three-pole basic amplifier. Feedback factor f_1 gives a zero phase margin and factor f_2 gives a negative phase margin.

is increased to f_2 (and $A_2 \approx 1/f_2$ is the overall gain), the phase margin is negative and the circuit will oscillate. Thus if this amplifier is to be used in a feedback loop with loop gain larger than $a_0 f_1$, efforts must be made to increase the phase margin. This process is known as *compensation*. Note that without compensation, the forward gain of the feedback amplifier cannot be made less than $A_1 \approx 1/f_1$ because of the oscillation problem.

The simplest and most common method of compensation is to reduce the bandwidth of the amplifier (often called *narrowbanding*). That is, a dominant pole is deliberately introduced into the amplifier to force the phase shift to be less than -180° when the loop gain is unity. This involves a direct sacrifice of the frequency capability of the amplifier.

If f is constant, the most difficult case to compensate is $f = 1$, which is a unity-gain feedback configuration. In this case the loop-gain curve is identical to the gain curve of the basic amplifier. Consider this situation and assume that the basic amplifier has the same characteristic as in Fig. 9.11. To compensate the amplifier, we introduce a new dominant pole with magnitude $|p_D|$, as shown in Fig. 9.12, and assume that this does not affect the original amplifier poles with magnitudes $|p_1|$, $|p_2|$, and $|p_3|$. This is often not the case but is assumed here for purposes of illustration.

The introduction of the dominant pole with magnitude $|p_D|$ into the amplifier gain function causes the gain magnitude to decrease at 6 dB/octave until frequency $|p_1|$ is reached, and over this region the amplifier phase shift asymptotes to -90° . If frequency $|p_D|$ is chosen so that the gain $|a(j\omega)|$ is unity at frequency $|p_1|$ as shown, then the loop gain is also unity at frequency $|p_1|$ for the assumed case of unity feedback with $f = 1$. The phase margin in this case is then 45° , which means that the amplifier is stable. The original amplifier would have been *unstable* in such a feedback connection.

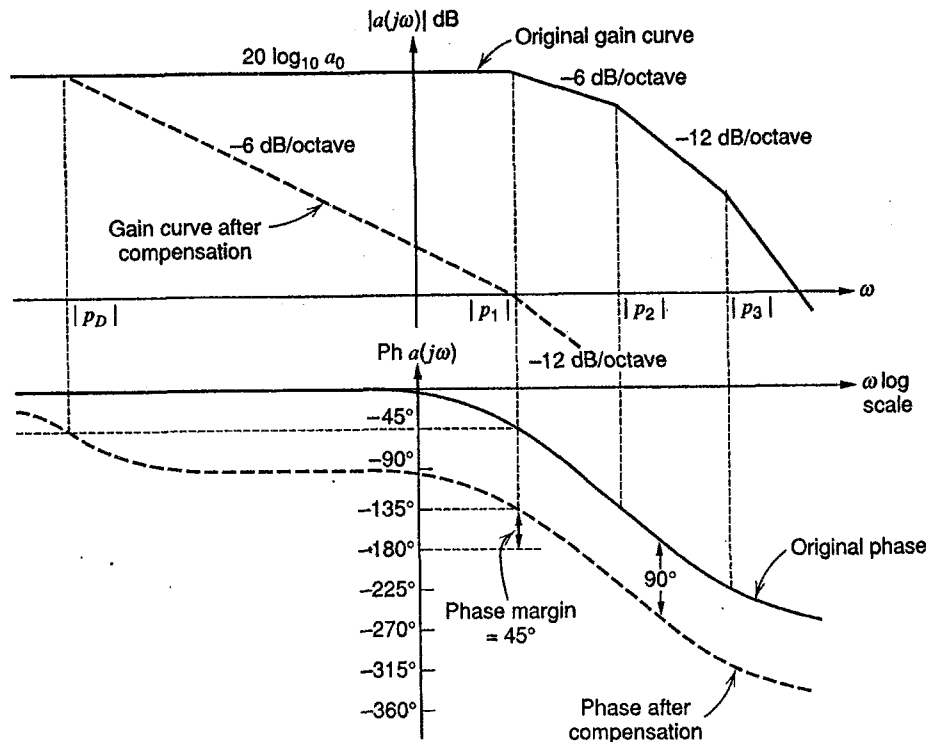


Figure 9.12 Gain and phase versus frequency for a three-pole basic amplifier. Compensation for unity-gain feedback operation ($f = 1$) is achieved by introduction of a negative real pole with magnitude $|p_D|$.

The price that has been paid for achieving stability in this case is that with the feedback removed, the basic amplifier has a unity-gain bandwidth of only $|p_1|$, which is much less than before. Also, with feedback applied, the loop gain now begins to decrease at a frequency $|p_D|$, and all the benefits of feedback diminish as the loop gain decreases. For example, in Chapter 8 it was shown that shunt feedback at the input or output of an amplifier *reduces* the basic terminal impedance by $[1 + T(j\omega)]$. Since $T(j\omega)$ is frequency dependent, the terminal impedance of a shunt-feedback amplifier will begin to *rise* when $|T(j\omega)|$ begins to decrease. Thus the high-frequency terminal impedance will appear *inductive*, as in the case of z_0 for an emitter follower, which was calculated in Chapter 7.