UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2003/2004

September/Oktober 2003

EEE 348E – PENGANTAR REKABENTUK LITAR BERSEPADU

Masa : 3 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **LAPAN (8)** muka surat bercetak dan **ENAM (6)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah bagi soalan diberikan disut sebelah kanan soalan berkenaan.

Pelajar dibenarkan menjawab semua soalan dalam Bahasa Inggeris **ATAU** Bahasa Malaysia **ATAU** kombinasi kedua-duanya.

...2/-

1. Figure 1 below depicts the generic design flow for both the front-end and back-end approaches.

Rajah 1 di bawah menunjukkan aliran rekabentuk generic bagi kedua pendekatan 'front-end' dan 'back-end'

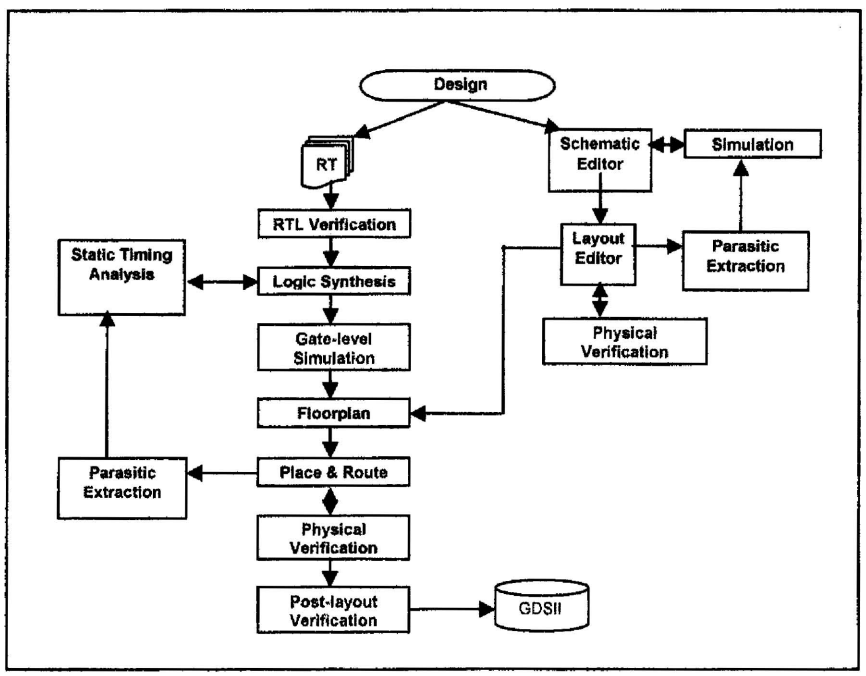

Figure 1: IC design flow

Describe at length both the approaches, with respect to the named blocks in the flowchart which would categorically brings the design from design specifications to tape-out.

Terangkan dengan panjang lebar kedua-dua pendekatan, menerangkan setiap blok bernama dalam carta alir yang akan membawa rekabentuk dari spesifikasi rekabentuk ke 'tape-out'

(20 marks)

...3/-

2 (a) What happens when a process neither has sensitivity list nor a wait statement?

Apa terjadi sekiranya proses tidak mempunyai 'sensitivity list' atau kenyataan 'wait '

(1 marks)

(b) Where should you declare the index that is used in a `for loop'? What is its visibility?

Di manakah indeks perlu dimasukkan yang digunakan bagi suatu 'loop'? Di manakah ianya jelas kelihatan?

(2 marks)

(c) What are the three weak strength values in IEEE 9 valued logic?

Apakah ketiga-tiga nilai kekuatan-kelemahan dalam nilai 9 logic IEEE?

(2 marks)

(d) What is the difference between a transaction and an event?

Apakah perbezaan antara 'transaction' dan 'event'?

(3 marks)

...4/-

(e) What is the value of x at the end of the process statement for (i) & (ii)?
Apakah nilai x pada kesudahan kenyataan proses bagi (i) & (ii)?

(i)
```
architecture one of some is
  begin
  process
    variable x : integer := 0;
    begin
        for i in 1 to 5 loop
    x := x + i;
    end loop;
    wait for 5 ns;
  end process;
  end one;
```
x = _____

(ii)
```
architecture two of same is
  signal x : integer := 0;
  begin
  process
      begin
      for i in 1 to 5 loop
          x <= x + i;
      end loop;
      wait for 5 ns;
  end process;
  end two;
```
x = _____

(12 marks)

3. (a) An entity "design1" is described by the following truth table, where b_2-b_0 are inputs and c_1,c_0 are outputs. Write a VHDL description that uses case statement to implement the logic function. Your code should use minimum number of "when" clauses. Name the architecture "arch1".

Suatu entity "design1" diterangkan oleh jadual kebenaran berikut, yang mana b_2-b_0 adalah masukan dan c_1, c_0 adalah keluaran. Tuliskan suatu kenyataan VHDL yang menggunakan kenyataan 'case' bagi mengimplementasikan fungsi logik tersebut. Kod anda harus menggunakan bilangan minimum klaus 'when'. Namakan architecture sebagai 'arch1'.

...5/-

Table 1/Jadual: Design1 truth-table/Jadual kebenaran design1

INPUTS			OUTPUTS	
b_2	b_1	b_0	c_1	c_0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(10 marks)

(b) Write a new architecture description "arch2" that describes the same entity, but rewrite the code using if-then-else statements.

Tuliskan architecture baru 'arch2' yang menerangkan entiti yang sama, tetapi menulis semula kod dalam kenyataan 'if-then-else'.

(10 marks)

...6/-

4. (a) Please give pull up and pull down expression for all logic combination below.

Sila hasilkan ungkapan tarik naik dan tarik bawah melalui gabungan persamaan logik dibawah.

(i) $Z = \overline{A.B.C.D}$

(ii) $Z = \overline{A+B+C+D}$

(iii) $Z = \overline{(A.B.C)+D}$

(6 marks)

(b) From CMOS logic gates expressions please design the corresponding circuits. (i.e pull up and pull down circuit).

Sila lukiskan litar melalui persamaan logic CMOS. (i.e pull up and pull down circuit).

(6 marks)

(c) Please draw the layout in stick diagram form from the designed circuitries.

Sila lukis bentangan dalam bentuk gambarajah lidi daripada ketiga-tiga litar yang dihasilkan di atas.

(8 marks)

5. (a) Please draw a cross section of an inverter.
Sila lukiskan gambarajah pandangan depan bagi inverter.

(5 marks)

...7/-

(b) Please give a latchup definition and from above cross section please explain how latchup occurs.

Terangkan maksud latchup dan daripada gambarajah depan yang dihasilkan di atas, sila terangkan bagaimanakah latchup terjadi.

(10 marks)

(c) Please give two suggestions to overcome or to reduce the latchup problems.

Berikan dua cadangan bagaimana untuk mengatasi/mengurangkan masalah terjadinya latchup tersebut.

(5 marks)

6. (a) Please give ESD definition and why it is important.
Berikan maksud ESD dan kenapa ia perlu.

(5 marks)

(b) Please give a simplest from of CMOS esd circuit and explain its function. (i.e. How its protects the input circuit inside the chip).

Berikan rekaan ringkas litar CMOS esd dan terangkan fungsinya. (Bagaimana ia berfungsi untuk melindungi litar di dalam cip).

(9 marks)

...8/-

(c) Please answer based on layout perspective.
Sila jawab bab c daripada perspektif layout.

(i) Explain antenna rules check.
Terangkan antenna-rules check.

(ii) Why it is important.
Kenapa ia penting.

(iii) Method to overcome antenna problems (ie give example on metal 1 and metal 2 only).

Cara untuk mengatasi masalah antenna.
(ie satu contoh metal 1 dan metal 2 sahaja).

(6 marks)

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