UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2003/2004

September/Oktober 2003

EEE 320 – MIKROPEMPROSES II

Masa : 2 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **ENAM BELAS (16)** muka surat termasuk 6 Lampiran bercetak dan **LIMA (5)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **EMPAT (4)** soalan.

Agihan markah bagi soalan diberikan disut sebelah kanan soalan berkenaan.

Jawab semua soalan di dalam Bahasa Malaysia.

...2/-

1. Rajah 1 adalah satu sistem mikropengawal 8031 dengan beberapa peranti luaran.
Figure 1 is an 8031 microcontroller system with several external devices.

(a) Daripada Rajah 1, terangkan dengan JELAS bagaimana sistem ini dapat direkabentuk bagi menyokong kapasiti ingatan sebanyak 24K x 8 bit RAM.

From Figure 1, explain in DETAIL how the system can be designed to support the memory capacity up to 24K x 8 bits of RAM.

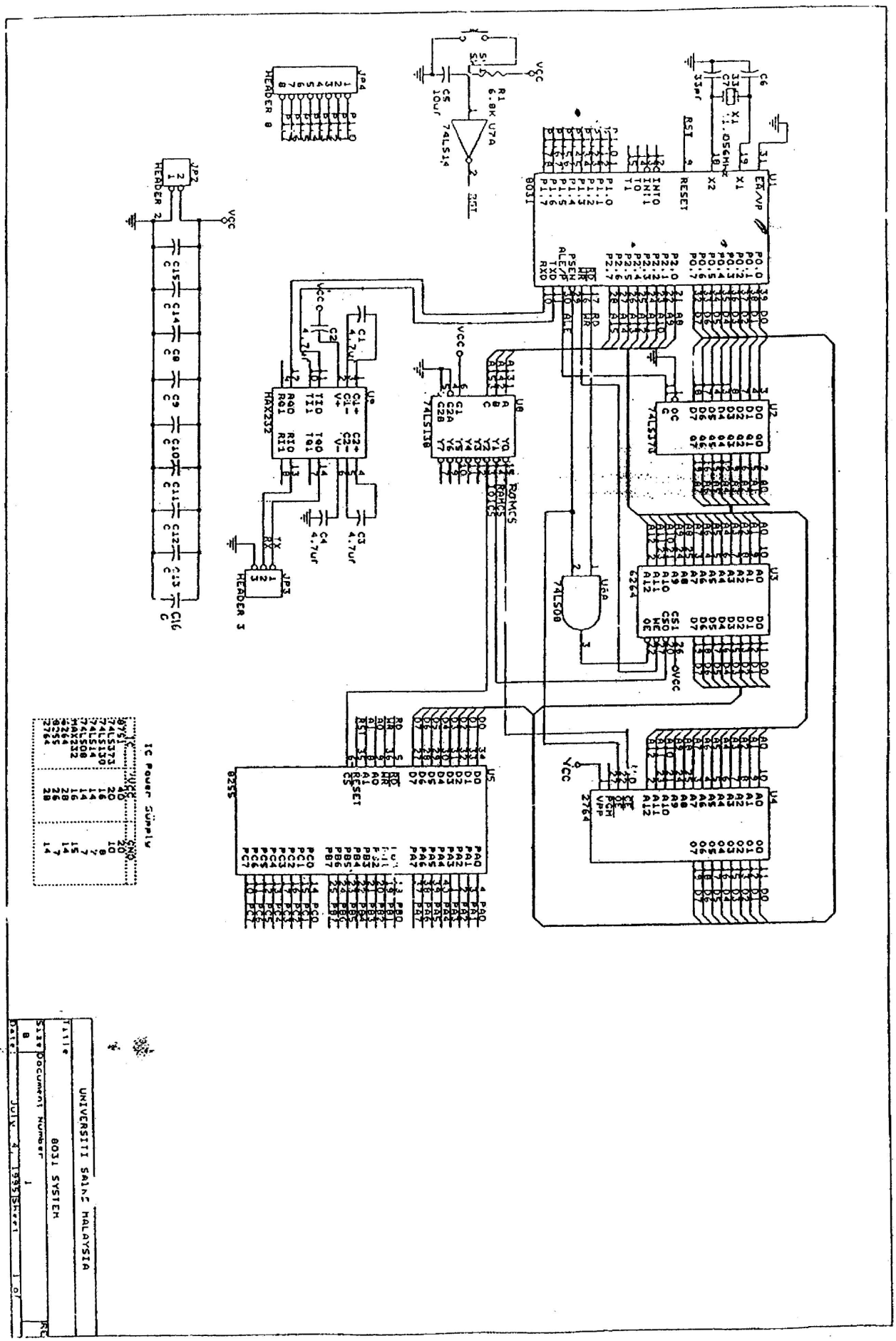
(20%)

(b) Berdasarkan penjelasan yang diberikan dalam 1(a), dengan menggunakan Rajah 1, tambahkan bilangan peranti ingatan yang sesuai. Sila lakarkan sambungan yang lengkap.

Based on the explanation given in 1(a), using Figure 1, add the suitable number of memory. Please sketch the complete connection.

(40%)

...3/-

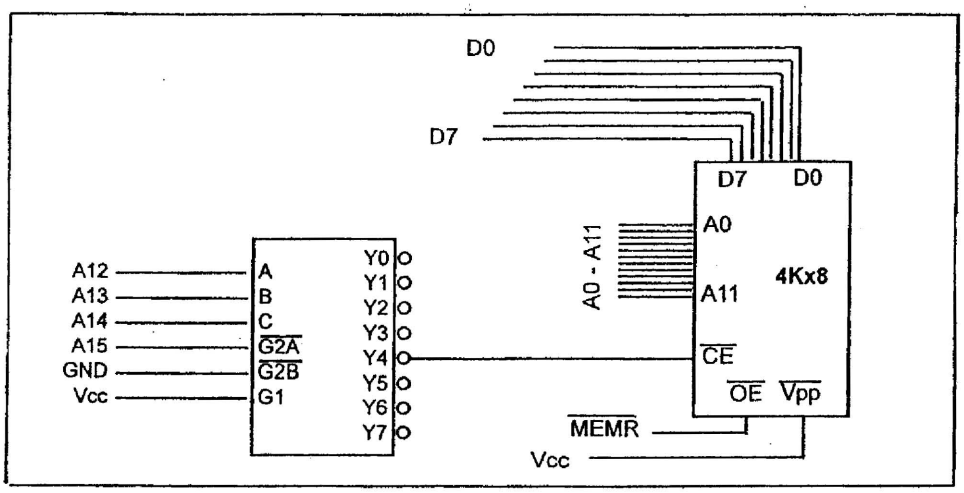


Rajah 1
Figure 1

(c) Berdasarkan Rajah 2, dapatkan julat alamat bagi yang berikut:-
Based on Figure 2, find the address range for the following:-

(i) Y2
(ii) Y4
(iii) Y7

(40%)



Rajah 2
Figure 2

2. (a) Bagi sistem berasaskan 8031 dengan program ROM luaran:
Based on an 8031 system with an external ROM program:

(i) Apabila mikropengawal dihidupkan, nyatakan alamat manakah *8031 akan mula membaca untuk arahan yang pertama.*

When the microcontroller is powered up, state which address the 8031 will start to read for the first instruction.

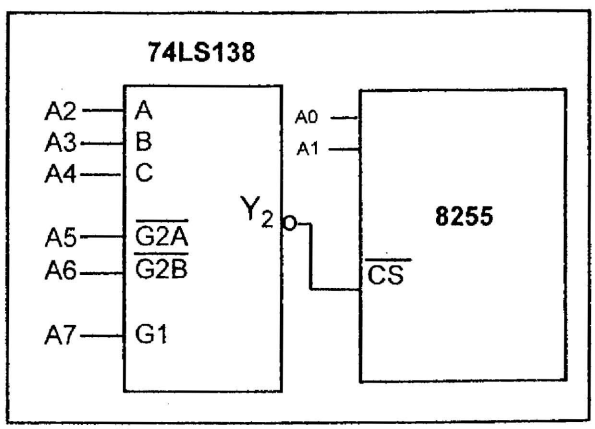
...5/-

(ii) Adakah ianya daripada ROM luaran atau dalaman?
Is it from an external or internal ROM?

(20%)

(b) Daripada Rajah 3, dapatkan alamat asas untuk 8255.
From Figure 3, find the base address for 8255.

(20%)



Rajah 3
Figure 3

(c) Berdasarkan Rajah 4
Based on Figure 4

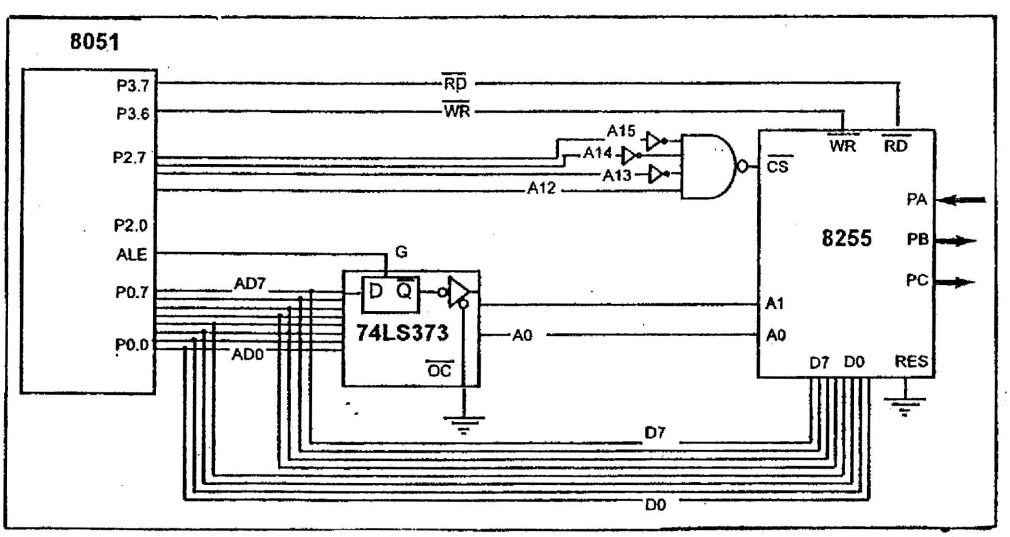
(i) Dapatkan alamat port I/Q yang ditetapkan untuk port A, B, C dan daftar kawalan.
Find the I/Q port addresses assigned to ports A, B, C and the control register.

...6/-

(ii) Dapatkan bait kawalan bagi 8255 jika PA=masukan, PB=keluaran dan PC=keluaran.
Find the control bytes for 8255 if PA=input, PB=output and PC=output.

(iii) Tulis satu aturcara untuk mendapatkan data daripada PA dan menghantar kepada PB dan PC.
Write a program to get the data from PA and send it to PB and PC.

(60%)



Rajah 4
Figure 4

...7/-

3. (a) Dalam merekabentuk sistem terbenam, beberapa langkah perlu diikuti secara sistematik. Huraikan dengan jelas.

In designing an embedded system, several steps are to be followed systematically. Explain in detail.

(30%)

(b) Anda dikehendaki merekabentuk satu sistem pengimbas cap jari menggunakan mikropengawal. Dengan menggunakan langkah-langkah yang anda berikan dalam 3(a), huraikan proses merekabentuk sistem tersebut. Cadangan mestilah mengandungi gambarajah blok, konsep operasi dan carta alir perisian untuk mengawal keseluruhan sistem. Anda bebas untuk membuat sebarang andaian.

You are required to design a fingerprint scanner system using microcontroller. Based on steps given in 3(a), explain the process of designing the system. The proposal should have a block diagram, an operation concept and a software flow chart to control the overall system. You can make any assumptions.

(70%)

4. (a) Nyatakan langkah-langkah yang perlu diambil bagi menghasilkan lengahan masa menggunakan pemasa mode 1.

State the steps that are needed to generate time delay using timer mode 1.

(40%)

...8/-

(b) Rekabentuk satu mesin menjual minuman dengan ciri-ciri berikut:
Design a simple vending machine with the following features:

(i) Mesin tersebut mempunyai mekanisma yang dapat menerima duit berasaskan saiz. Anggap satu isyarat dijanakan apabila syiling dimasukkan.

The vending machine has a coin-in mechanism that can accept coins based on size. Assume a pulse is generated when a coin is inserted.

(ii) Terdapat dua peraga 7-segmen untuk memaparkan jumlah yang telah dimasukkan.

There are two seven-segment LED displays to display the total amount inserted.

(iii) Kos produk ditentukan oleh dua suis untuk memilih 90 sen atau RM1.00.

The cost of the product is determined by two switches to select 90 cents or RM1.00.

(iv) Apabila jumlah yang betul telah dimasukkan, pengguna boleh memilih minuman yang diperlukan menggunakan empat suis.

When the correct amount has been inserted the user can select the required drink using four switches.

...9/-

(v) Sebaik sahaja minuman dipilih, solenoid perlu diaktifkan untuk mengeluarkan minuman dan baki jika ada.

As soon as a selection is made solenoids should be activated to dispense the necessary product and provide any change required.

Anda boleh membuat sebarang andaian yang perlu dan nyatakan sebarang ciri-ciri untuk membuatkan mesin ini adalah mesra pengguna. Rekabentuk anda mesti mengandungi gambarajah blok dan carta alir bagi proses tersebut.

Make any assumptions you think are necessary and provide any additional features to make the machine as user friendly as possible. Your design must have a block diagram and a flow chart of the process.

(60%)

5. Bincangkan masalah-masalah yang terlibat dalam merekabentuk sistem pengawal terbenam untuk persekitaran hingar secara elektrik.

Discuss the problems involved in designing embedded controller systems for electrically noisy environments.

Aspek-aspek berikut mesti dibincangkan secara jelas.
The following aspects must be discussed in detail.

(i) Jenis dan sumber hingar elektrik
Types and sources of electrical noise

(ii) Kesan hingar
Effects of noise

...10/-

(iii) Perlindungan
Shielding

(iv) Bumi
Grounds

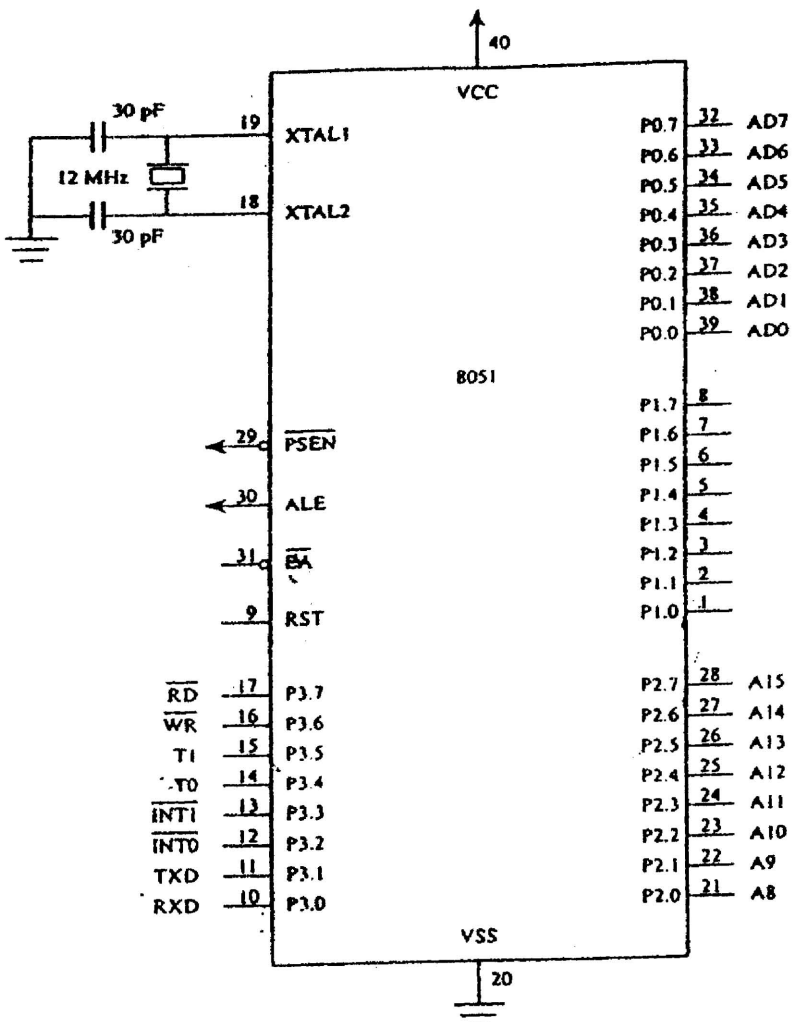
(v) Agihan sumber kuasa dan nyahgandingan
Power supply distribution and decoupling

(vi) Strategi bentangan PCB
PCB layout strategy.

(100%)

ooo0ooo

8051 pinouts



80C51 FAMILY INSTRUCTION SET

Table 7. 80C51 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings[1]

Instruction	Flag C	OV	AC	Instruction	Flag C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

[1]Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn	Register R7-R0 of the currently selected Register Bank.
direct	8-bit internal data location's address. This could be an internal Data RAM location (0-127) or a SFR (i.e., I/O port, control register, status register, etc. (128-255)).
@Ri	8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
#data	8-bit constant included in the instruction.
#data 16	16-bit constant included in the instruction
addr 16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr 11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.
bit	Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC	A,#data	Add immediate data to A_{CC} with carry	2	12
SUBB	A,Rn	Subtract Register from A_{CC} with borrow	1	12
SUBB	A,direct	Subtract direct byte from A_{CC} with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from A_{CC} with borrow	1	12
SUBB	A,#data	Subtract immediate data from A_{CC} with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12

Philips Semiconductors

80C51 Family — 80C51 family programmer's guide and instruction set

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS (Continued)				
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment indirect RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A and B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12
RL	A	Rotate Accumulator left	1	12
RLC	A	Rotate Accumulator left through the carry	1	12
RR	A	Rotate Accumulator right	1	12
RRC	A	Rotate Accumulator right through the carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	bit,rel	Jump if direct bit is set	3	24
JNB	bit,rel	Jump if direct bit is not set	3	24
JBC	bit,rel	Jump if direct bit is set and clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	24
LCALL	addr16	Long subroutine call	3	24
RET		Return from subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute jump	2	24
LJMP	addr16	Long jump	3	24
SJMP	rel	Short jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is zero	2	24
JNZ	rel	Jump if Accumulator is not zero	2	24
CJNE	A,direct,rel	Compare direct byte to A_{CC} and jump if not equal	3	24
CJNE	A,#data,rel	Compare immediate to A_{CC} and jump if not equal	3	24
CJNE	Rn,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ	Rn,rel	Decrement register and jump if not zero	2	24
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	24
NOP		No operation	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Acc	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	RN,#data	Move immediate data to reg	2	12
MOV	direct,A	Move Accumulator to direct b	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct b	2	24
MOV	direct,#data	Move immediate data to direc	3	24
MOV	@Ri,A	Move Accumulator to indirect	1	12
MOV	@Ri,direct	Move direct byte to indirect R	2	24
MOV	@Ri,#data	Move immediate data to indir M	2	12
MOV	DPTR,#data16	Load DataPointer with a 16-b tant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to D Acc	1	24
MOVC	A,@A+PC	Move Code byte relative to P cc	1	24
MOVX	A,@Ri	Move external RAM (8-bit ad cc	1	24
MOVX	A,@DPTR	Move external RAM (16-bit a Acc	1	24
MOVX	A,@Ri,A	Move A_{CC} to external RAM (dr)	1	24
MOVX	@DPTR,A	Move A_{CC} to external RAM (ddr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accu r	1	12
XCH	A,direct	Exchange direct byte with Ac ator	2	12
XCH	A,@Ri	Exchange indirect RAM with ister	1	12
XCHD	A,@Ri	Exchange low-order digit ind AM with A_{CC}	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to carry	2	24
ANL	C,/bit	AND complement of direct b ry	2	24
ORL	C,bit	OR direct bit to carry	2	24
ORL	C,/bit	OR complement of direct bit y	2	24
MOV	C,bit	Move direct bit to carry	2	12
MOV	bit,C	Move carry to direct bit	2	24
JC	rel	Jump if carry is set	2	24
JNC	rel	Jump if carry not set	2	24

HM6264BI Series

8,192-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-492A (Z)
Rev. 1.0
Sep. 5, 1996

Description

The Hitachi HM6264BI is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 μm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

- High speed
  - — Fast access time: 100/120 ns (max)
- Low power
  - — Standby: 10 μW (typ)
  - — Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - — Three state output
- Directly TTL compatible
  - — All inputs and outputs
- Battery backup operation capability
- Operating temperature range
  - — –40°C to +85°C

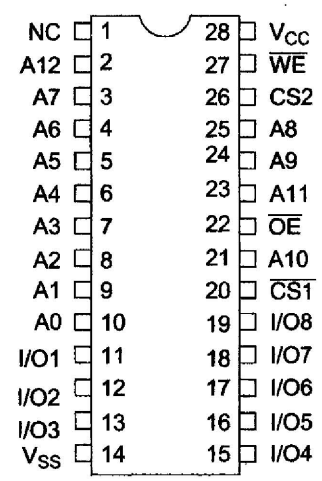
Ordering Information

Type No.	Access time	Package
HM6264BLPI-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264BLPI-12	120 ns	
HM6264BLFPI-10T	100 ns	450-mil, 28-pin plastic SOP(FP-28DA)
HM6264BLFPI-12T	120 ns	

HM6264BI Series

Pin Arrangement

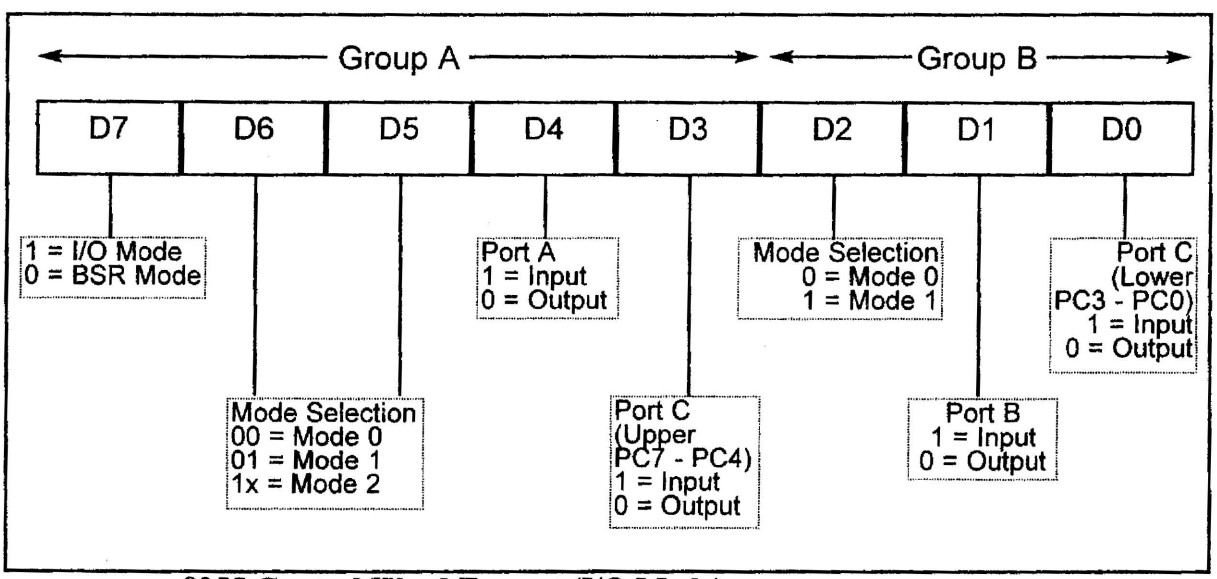
HM6264BLPI/BLFPI Series



(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{cc}	Power supply
V_{ss}	Ground



8255 Control Word Format (I/O Mode)