UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama

Sidang Akademik 2003/2004

September/Oktober 2003

EEE 241 – ELEKTRONIK ANALOG 1

Masa : 3 Jam

ARAHAN KEPADA CALON:-

Sila pastikan kertas peperiksaan ini mengandungi **TUJUH BELAS (17)** muka surat termasuk **3 Lampiran** bercetak dan **ENAM (6)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah diberikan di sut sebelah kanan soalan berkenaan.

Semua soalan hendaklah dijawab di dalam Bahasa Malaysia.

...2/-

1. (a) Transistor Q dalam penguat pemancar sepunya dalam **Rajah 1(a)** mempunyai voltan "Early" V_A = 100 V dan parameter-parameter *h* seperti dalam **Rajah 1(b) – (e)**. Dengan V_{CC} = 10 V, rekabentuk litar untuk mendapatkan arus pincang I_C = 2 mA, arus melalui R_1 and R_2 sama dengan $0.1I_C$, voltan pemungut $V_C \cong 5$ V dan $V_E \cong V_{BE(active)}$.
Gunakan perintang standard yang diberikan dalam Jaduai 1 dalam rekabentuk anda.
Andaikan $V_{BE(active)} = 0.7$ V

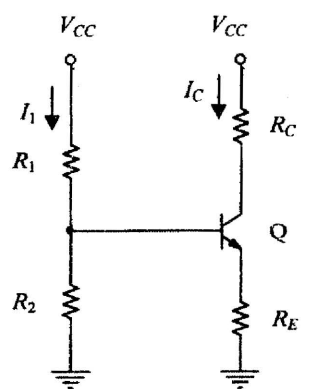
The transistor Q in the common-emitter (C-E) amplifier of ***Figure 1(a)*** *has an Early voltage* V_A = *100 V and h–parameters as shown in* ***Figures 1(b) – (e)****. With* V_{CC} = *10 V, design the circuit for a bias current* I_C *of 2 mA, the current through* R_1 *and* R_2 *equals* $0.1I_C$*, the collector voltage* V_C *of approximately 5 V and* $V_E \cong V_{BE(active)}$.
Use standard resistors given in Table 1 in your design.
Assume $V_{BE(active)} = 0.7$ *V.*

(20%)

(b) Dengan perintang standard yang diperolehi dalam (a) di atas, analisis litar untuk menentukan nilai sebenar I_C, I_E, I_B, V_C, V_E, dan V_B.

With the standard resistors obtained in (a) above, analyse the circuit to determine the actual values of I_C, I_E, I_B, V_C, V_E, *and* V_B.

(30%)

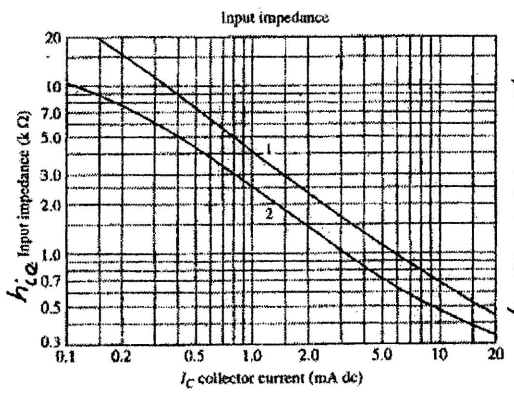


Rajah 1(a)
Figure 1(a)

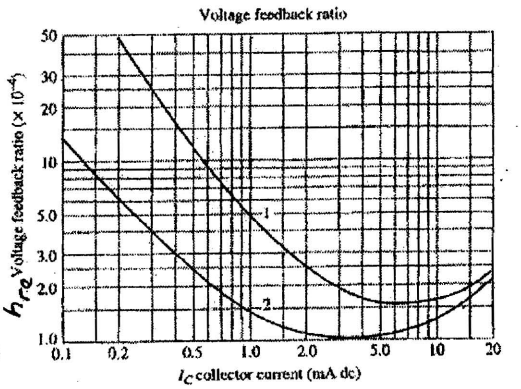
...3/-

Jadual (*Table*) 1
Nilai rintangan standard (x 10^n)
Standard resistance values (x 10^n)

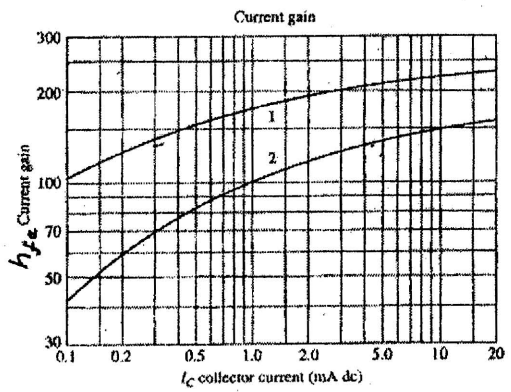
10	16	27	43	68
11	18	30	47	75
12	20	33	51	82
13	22	36	56	91
15	24	39	62	100



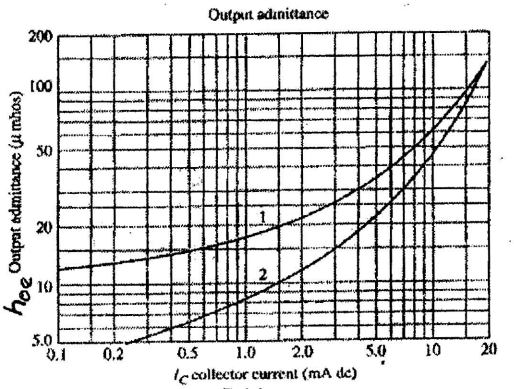
Rajah 1(b)
Figure 1(b)



Rajah 1(c)
Figure 1(c)



Rajah 1(d)
Figure 1(d)



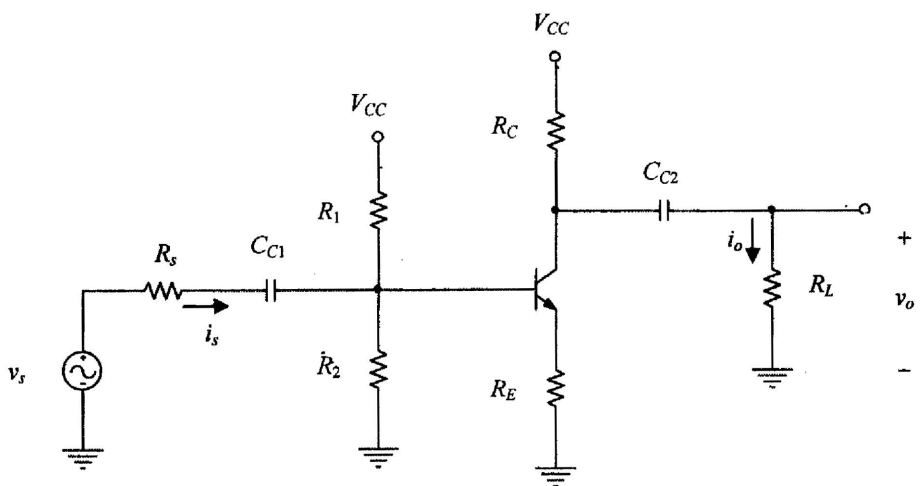
Rajah 1(e)
Figure 1(e)

...4/-

(c) Satu sumber voltan isyarat v_s yang mempunyai rintangan dalam R_s = 1 kΩ dan satu perintang beban R_L = 10 kΩ masing-masing disambung ke terminal masukan dan keluaran penguat seperti dalam **Rajah 1(f)**. Sekiranya v_S diberikan oleh ungkapan $v_s = 10\sin 2000\pi t$ mV; terbitkan ungkapan-ungkapan bagi v_o. i_s dan i_o. Kesan-kesan C_{C1}, C_{C2}, h_{re} and h_{oe} boleh diabaikan.

A signal source v_s with an internal resistance R_s = 1 kΩ and a resistive load R_L = 10 kΩ are connected to the input and output terminals of the amplifier respectively, as shown in ***Figure 1(f)***. *If the expression for v_s is given as $v_s = 10\sin 2000\pi t$ mV; determine the expressions for v_o. i_s and i_o. You may neglect the effects of C_{C1}, C_{C2}, h_{re} and h_{oe} ;*

(50%)



Rajah 1(f)
Figure 1(f)

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2. (a) Transistor MOSFET Q_1 dalam penguat sumber sepunya dalam **Rajah 2** mempunyai parameter-parameter berikut: $k_n' = 20\mu\text{A/V}^2$; $W = 125\mu\text{m}$; $L = 2\mu\text{m}$ dan $V_{tn} = 1\text{V}$. Sekiranya keluaran bagi sumber voltan isyarat v_s diberikan oleh ungkapan $v_s = 20\sin 2000\pi t$ mV, terbitkan ungkapan bagi voltan keluaran v_o. Nyatakan semua andaian yang anda gunakan untuk menerbitkan ungkapan.

The MOSFET transistor Q_1 in the CS amplifier circuit of ***Figure 2*** *has the following parameters:* $k_n' = 20\mu\text{A/V}^2$; $W = 125\mu\text{m}$; $L = 2\mu\text{m}$ dan $V_{tn} = 1\text{V}$. *If output of the signal source v_s is given by the expression* $v_s = 20\sin 2000\pi t$ *mV, determine the expression for the output voltage v_o. State all the assumptions used in determining your expression.*

(50%)

(b) Berikan TIGA kekurangan dalam penguat sumber sepunya dalam **Rajah 2** yang menyebabkannya tidak sesuai untuk kegunaan dalam litar bersepadu (IC).

Give THREE shortcomings in the common-source S amplifier of ***Figure 2*** *which make it unsuitable for implementation in an integrated circuit (IC).*

(10%)

(c) Cadangkan satu sumber arus malar <u>secara konsep</u>, yang boleh digunakan untuk menentukan arus pincang dan juga sebagai beban aktif bagi penguat sumber sepunya. Jelaskan bagaimana litar yang anda cadangkan boleh menentukan nilai arus pincang bagi penguat.

Suggest a <u>conceptual</u> constant current source which may be used to set the bias current and to act as an active load for the CS amplifier. Describe how your proposed circuit establishes the required bias current for the amplifier.

(40%)

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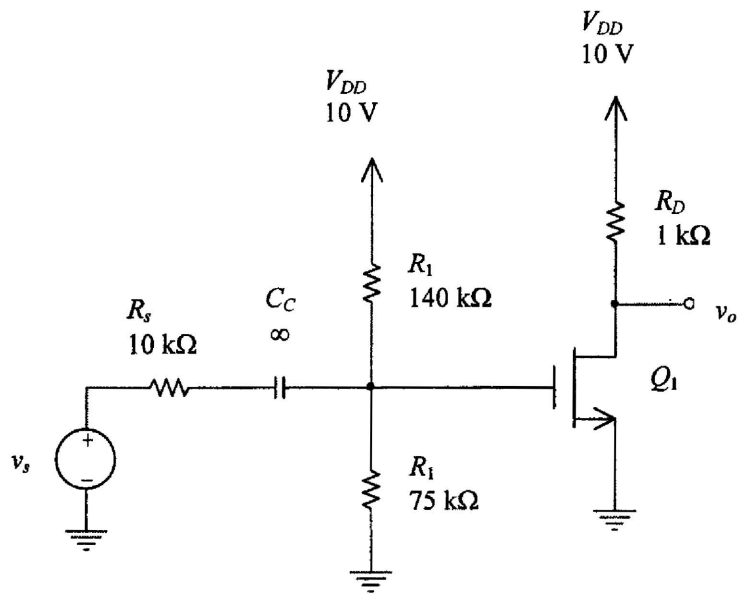


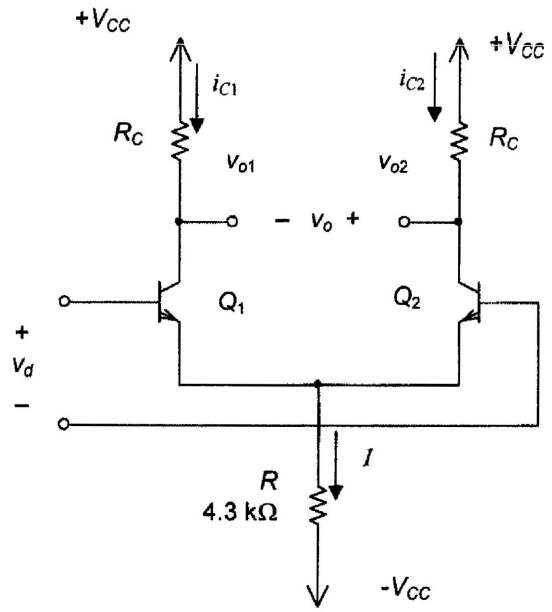
Rajah 2
Figure 2

3. Perintang R dalam penguat pembezaan dalam **Rajah 3** digunakan untuk menentukan arus pincang *I* bagi transistor Q_1 dan Q_2. v_d adalah voltan masukan isyarat kecil merentasi tapak-tapak transistor. Q_1 dan Q_2 adalah sepadan dan mempunyai gandaan arus α di mana;

The resistor R in the differential amplifier of ***Figure 3*** *is used to set the bias current I of the transistors Q_1 and Q_2. v_d is the small-signal input voltage applied across the bases of transistors. Q_1 and Q_2 are matched transistors and each has current gain α where;*

$$\alpha = \frac{i_E}{i_C} \qquad (i_E = I_E + i_e;\ i_C = I_C + i_c)$$

...7/-



Rajah 3
Figure 3

(a) Terbitkan satu ungkapan bagi i_{C1} dan i_{C2} dalam sebutan α, arus pincang I, v_d dan V_T; dan seterusnya buktikan bahawa gandaan pembezaan voltan "*double-ended*" A_d penguat diberikan oleh ungkapan;

Assuming that v_d is small-signal input voltage, derive an expression for i_{C1} and i_{C2} in terms of α, bias current I, v_d and V_T; and hence show that the double-ended differential voltage gain is given by the expression;

$$A_d = -g_m R_C$$

(50%)

(b) Daripada ungkapan yang diperolehi dalam (a) di atas, dapatkan ungkapan bagi gandaan voltan pembezaan "*single-ended*" v_{o1}/v_d;

From the expression derived in (a) above, obtained an expression for single-ended differential voltage gain v_{o1}/v_d;

(10%)

...8/-

(c) Kira gandaan-gandaan voltan pembezaan "*double-ended*" dan "*single-ended*" apabila V_{CC} = 5 V, R_C = 2 kΩ, V_{BE} = 0.7 V dan V_T = 25 mV bagi kedua-dua transistor;

Calculate the double-ended and single-ended differential voltage gains if V_{CC} = 5 V, R_C = 2 kΩ, V_{BE} = 0.7 V *and* V_T = 25 mV *for both transistors;*

(20%)

(d) Berikan ungkapan bagi v_o dan v_{o1} apabila $v_d = 0.02 \sin 2000\pi t$ V.

Give the expressions for v_o *and* v_{o1} *when* $v_d = 0.02 \sin 2000\pi t$ V.

(20%)

4. Bagi penguat berbilang peringkat dalam **Rajah 4(a)**, Q_1, Q_2, Q_3, Q_4 dan Q_6 adalah dari jenis yang sama dan masing-masing mempunyai ciri-ciri berikut: β = 256; V_A = 74 V; V_T = 25 mV; V_{BE} = 700 mV pada nilai I_C = 9.3 mA.
Q_5 mempunyai ciri-ciri berikut: β = 100; V_A = 63 V; V_T = 25 mV; V_{BE} = 650 mV pada nilai I_C = 6 mA; Sumber voltan Vcc = 15 V.

For the multistage amplifier in ***Figure 4(a)****,* Q_1, Q_2, Q_3, Q_4 *and* Q_6 *are identical transistors and each has the following properties:* β = 256; V_A = 74 V; V_T = 25 mV; V_{BE} = 700 mV at I_C = 9.3 mA;
Q_5 *has the following properties:* β = 100; V_A = 63 V; V_T = 25 mV; V_{BE} = 650 mV at I_C = 6 mA; *The voltage supply Vcc = 15 V.*

(a) Cari nilai bezaupaya-bezaupaya pada C_1; C_2; C_4; E_1; E_3; E_5; E_6 dan B_6; dan arus-arus I_{E1}; I_{E2}; I_{E3}; I_{E4}; I_{E5}; I_{E6}; I_{C1}; I_{C2}; I_{C3} dan I_{C4}. Jelaskan andaian-andaian yang anda gunakan.

Find the potentials at C_1; C_2; C_4; E_1; E_3; E_5; E_6 *and* B_6; *and the currents* I_{E1}; I_{E2}; I_{E3}; I_{E4}; I_{E5}; I_{E6}; I_{C1}; I_{C2}; I_{C3} *and* I_{C4}. *State clearly any assumption you make.*

(40%)

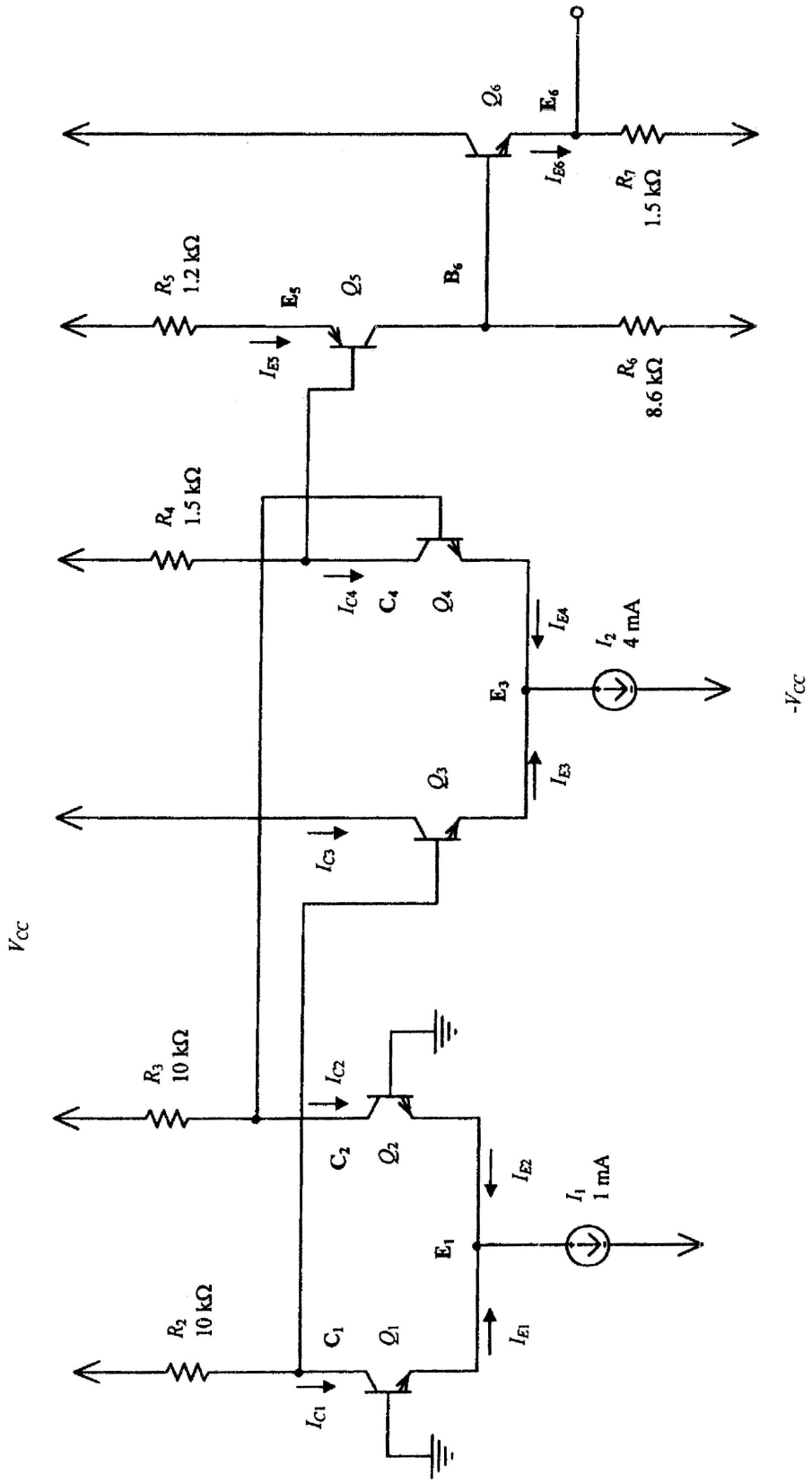
...9/-

(b) Satu isyarat masukan $v_d = 100\sin 2000\pi$ μV dikenakan di antara tapak-tapak Q_1 dan Q_2 seperti dalam **Rajah 4(b)**. Cari gandaan voltan keseluruhan penguat dan berikan ungkapan bagi voltan keluaran v_o pada pemancar Q_6. Jelaskan andaian-andaian yang anda gunakan.

An input signal $v_d = 100\sin 2000\pi$ μV *is applied between the bases of* Q_1 *and* Q_2 *as shown in* ***Figure 4(b)***. *Find the overall gain of the amplifier and hence give an expression for the output signal voltage* v_o *at the emitter of* Q_6. *State clearly any assumption you make.*

(40%)

...10/-



Rajah 4(a)
Figure 4(a)

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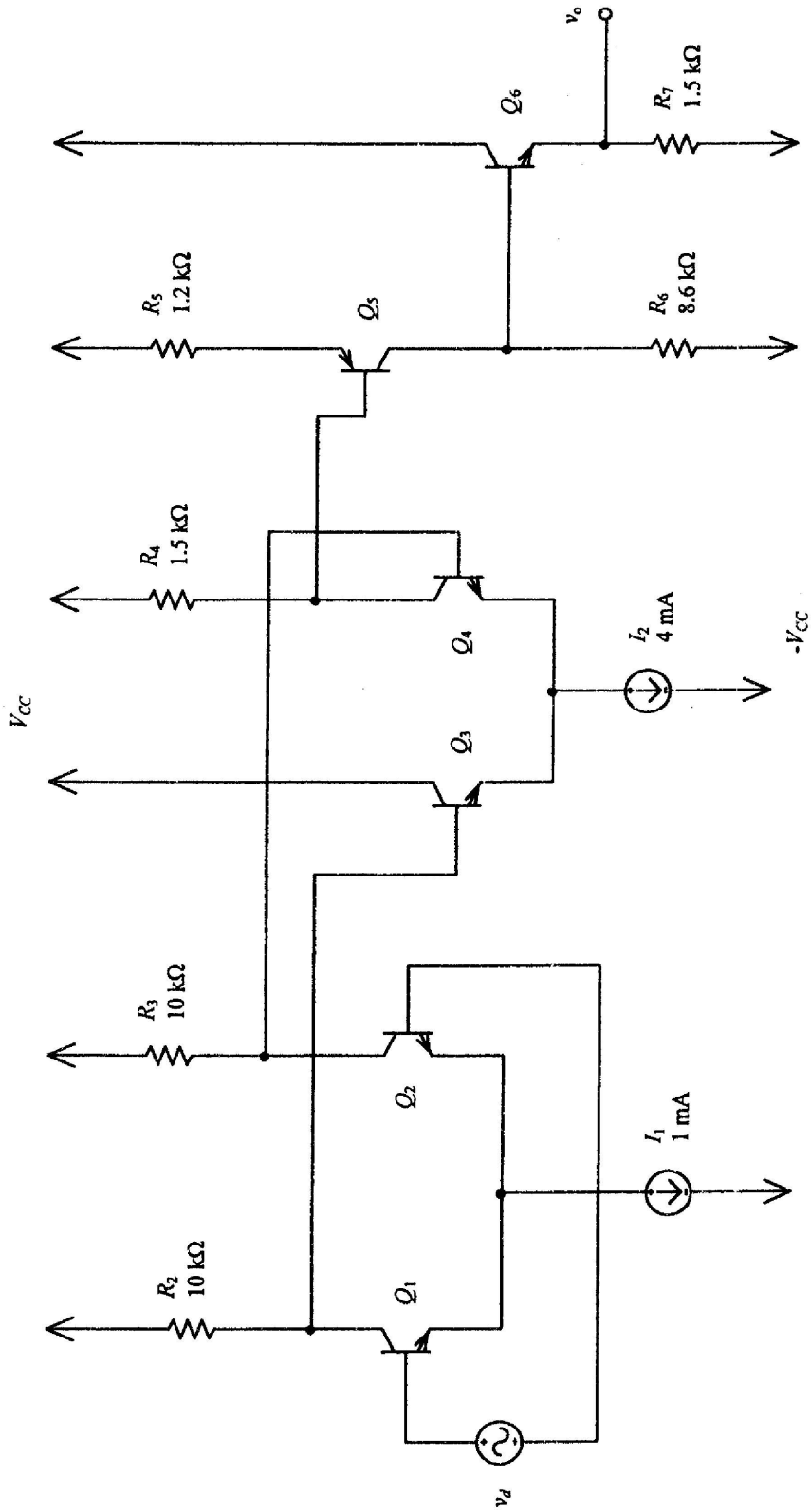

Rajah 4(b)
Figure 4(b)

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(c) Rekabentuk satu sumber arus dan cermin arus yang asas untuk menggantikan sumber arus I1 dan I2 dalam **Rajah 4(a)**. Gunakan transistor-transistor dari jenis yang sama dengan Q1 dan sumber voltan yang sama dengan V_{CC} dalam **Rajah 4(a)** dalam rekabentuk anda. Jelaskan andaian-andaian yang anda gunakan.

*Design a basic transistor current source and current mirror to replace the current sources I1 and I2 in **Figure 4(a)**. Use transistors identical to Q1 and the supply voltage identical to V_{CC} of **Figure 4(a)** in your design. State clearly any assumption you make.*

(20%)

5. (a) Dengan bantuan rajah-rajah yang sesuai, jelaskan secara ringkas maksud "***crossover distortion***" dalam penguat kuasa Kelas B dan terangkan bagaimana ia dapat dielakkan dalam penguat kuasa AB.

*With the aid of suitable diagrams, explain briefly what is meant by **crossover distortion** in Class B power amplifier and describe how it is eliminated in a Class AB power amplifier.*

(40%)

(b) Bagi penguat kuasa Kelas AB dalam **Rajah 5**;
*For the Class AB power amplifier shown in **Figure 5**;*

$\beta_N = \beta_P = 50$; $I_{SQN} = I_{SQP} = 10^{-13}$ A; $I_{SD1} = I_{SD2} = 3\times10^{-14}$ A, $R_L = 8\ \Omega$.

Cari nilai yang sesuai bagi arus pincang I_{bias}, V_{CC} dan amplitud bagi voltan isyarat masukan sinus v_{ip} supaya kuasa purata yang dibekalkan kepada R_L ialah 5 W. Arus minimum melalui D1 dan D2 hendaklah tidak kurang daripada 5 mA dan amplitud bagi voltan isyarat keluaran v_{op} lebihkurang sama dengan $0.75V_{CC}$. Jelaskan andaian-andaian yang anda gunakan.

...13/-

Determine suitable values of I_{bias}, V_{CC} and the amplitude of sinusoidal input signal voltage v_{ip} so that the average power delivered to R_L is 5 W. The minimum current through D1 and D2 shall not be allowed to drop below 5 mA and the amplitude of the output signal voltage v_{op} shall be about $0.75V_{CC}$. State clearly any assumption made in your calculation.

(20%)

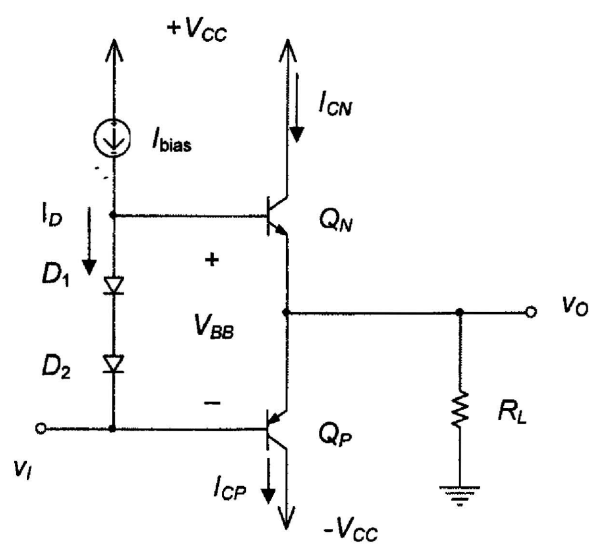
(c) [i] Cari nilai V_{BB} dan arus-arus pemungut I_{CN} dan I_{CP} apabila voltan isyarat masukan $v_i = 0$;

Find V_{BB} and the collector current I_{CN} and I_{CP} when the input signal voltage $v_i = 0$;

[ii] Cari nilai V_{BB} dan arus pemungut I_{CP} apabila voltan isyarat masukan v_i berada pada nilai puncak positif.

Find V_{BB} and collector current I_{CP} when the input signal v_i is at its peak positive value.

(40%)



Rajah 5
Figure 5

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6. Bagi penguat pemancar sepunya dalam **Rajah 6**;
*For the common-emitter amplifier shown in **Figure 6**;*

$R_s = 4$ kΩ; $R_1 = 8$ kΩ; $R_2 = 4$ kΩ; $R_E = 3.3$ kΩ; $R_C = 6$ kΩ; $R_L = 4$ kΩ;
$C_{C1} = C_{C2} = 1$ μF; $C_E = 10$ μF; $V_{CC} = 12$ V.

Pada nilai $I_E = 1$ mA, transistor Q mempunyai parameter-parameter berikut;
At $I_E = 1$ mA, the transistor Q has the following parameters;

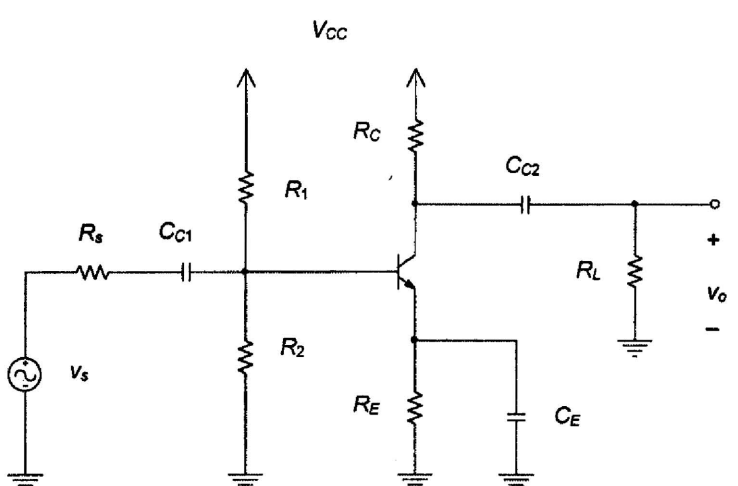
$\beta_o = 100$; $r_x = 50$ Ω; $r_o = 100$ kΩ; $C_\pi = 13.9$ pF; $C_\mu = 2$ pF;

(a) kira gandaan voltan jalur tengah;
calculate the midband voltage gain; (30%)

(b) kira frekuensi potong rendah f_L;
calculate the lower cutoff frequency f_L; (30%)

(c) kira frekuensi potong tinggi f_H;
calculate the upper cutoff frequency f_H; (30%)

(d) kira nilai baru bagi C_{C1}, C_{C2} dan C_E supaya f_L menjadi 100 Hz.
calculate the new values of C_{C1}, C_{C2} and C_E so that f_L becomes 100 Hz. (10%)



Rajah 6
Figure 6

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TABLE 1 : BJT CURRENT-VOLTAGE RELATIONSHIPS IN ACTIVE MODE

$$i_C = I_S\, e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha\, i_E \qquad i_B = (1 - \alpha) i_E = \frac{i_E}{\beta + 1}$$

$$i_C = \beta\, i_B \qquad i_E = (\beta + 1) i_B$$

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1}$$

V_T = thermal voltage $= \dfrac{kT}{q} \cong 25$ mV at room temperature

TABLE 2: RELATIONSHIPS BETWEEN THE SMALL-SIGNAL MODEL PARAMETERS OF THE BJT

Model Parameters in Terms of DC Bias Currents:

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right)$$

$$r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{V_A}{I_C}$$

In terms of g_m:

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In terms of r_e:

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta + 1) r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between α and β:

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1} \qquad \beta + 1 = \frac{1}{1 - \alpha}$$

TABLE 3 : SUMMARY OF IMPORTANT MOSFET EQUATIONS

Current-Voltage Relationships

■ For NMOS Devices:

- *Triode region* ($v_{GS} \geq V_t$, $v_{DS} \leq v_{GS} - V_t$)

$$i_D = k'_n \left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

For small v_{DS}: $r_{DS} \equiv \dfrac{v_{DS}}{i_D} = \left[k'_n\left(\dfrac{W}{L}\right)(v_{GS} - V_t)\right]^{-1}$

- *Saturation region* ($v_{GS} \geq V_t$, $v_{DS} \geq v_{GS} - V_t$)

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

- $k'_n = \mu_n C_{ox}$

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right]$$

$$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}, \qquad q = 1.6 \times 10^{-19} \text{ coulomb}, \ \varepsilon_s = 1.04 \times 10^{-12} \text{ F/cm}$$

$$\lambda = 1/V_A, \qquad V_A \propto L$$

■ For PMOS Devices: V_t, γ, λ and V_A are negative

- For triode region, $v_{GS} \leq V_t$ and $v_{DS} \geq v_{GS} - V_t$
- For saturation region, $v_{GS} \leq V_t$ and $v_{DS} \leq v_{GS} - V_t$

■ For Depletion Devices

- n channel: V_t is negative
- p channel: V_t is positive
- $I_{DSS} = \dfrac{1}{2}k'\left(\dfrac{W}{L}\right)V_t^2$

TABLE 3 (CONTD) : SUMMARY OF IMPORTANT MOSFET EQUATIONS

Small-Signal Model
$g_m = \sqrt{2k'(W/L)}\sqrt{I_D} \qquad r_o = \dfrac{\lvert V_A\rvert}{I_D}$
$g_m = k'(W/L)(V_{GS} - V_t)$
$g_m = \dfrac{2I_D}{V_{GS} - V_t} \qquad V_{GS} - V_t \equiv V_{eff}$
$g_{mb} = \chi g_m, \qquad \chi = \gamma/[2\sqrt{2\phi_f + \lvert V_{SB}\rvert}]$
$C_{gs} = \dfrac{2}{3}WLC_{ox} + WL_{ov}C_{ox} \qquad C_{gd} = WL_{ov}C_{ox}$
$C_{sb} = \dfrac{C_{sb0}}{\sqrt{1 + \dfrac{\lvert V_{SB}\rvert}{V_0}}} \qquad C_{db} = \dfrac{C_{db0}}{\sqrt{1 + \dfrac{\lvert V_{DB}\rvert}{V_0}}}$
$f_T = \dfrac{g_m}{2\pi(C_{gs} + C_{gd})}$