UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 2011/2012

January 2012

EBB 526/3 – Electronic Packaging

Duration : 3 hours

Please ensure that this examination paper contains SIX printed pages before you begin the examination.

This paper consists of SIX questions.

Instruction: Answer **FIVE** questions. If candidate answers more than five questions only the first five questions answered in the answer script would be examined.

The answers to all questions must start on a new page.

All questions must be answered in English.

1. [a] Briefly explain the driving force to further reduce the size of an integrated circuit.

(40 marks)

[b] What are the functions of electronic package? Your answer must be supported by appropriate examples.

(40 marks)

[c] Sketch and label a cross sectional view of a flip chip electronic package.

(20 marks)

2. [a] In order to obtain high modulus and low coefficient of thermal expansion (CTE) high filler content capillary underfill (CUF) is usually used. In your opinion, what is the importance of having high modulus and low CTE in underfill?

(20 marks)

[b] A typical formulation of capillary underfill (CUF) is shown in Table 1.

Table 1: Typical formulation of capillary underfill

Ingredients	**%**
Epoxy resin	40
Curing agent	15
Filler (SiO_2)	40
Catalyst	2
Surfactant	2
Defoamer	0.5
Colour	0.5

(i) Describe the function of the first five ingredients.

(10 marks)

(ii) Can you predict the properties of the underfill if 20% of curing agent is used?

(10 marks)

(iii) If we do not want to use SiO_2 what would you recommend as an alternative filler and why?

(10 marks)

(iv) Is nano size filler suitable to be used in underfill and why? Is there any modification need to be done to the formulation if nano size filler is used?

(20 marks)

(v) What is the effect to the curing process and degree of crosslinking if catalyst is not used?

(10 marks)

[c] Please discuss the effect of filler settlement on the properties of underfill and how to overcome filler settlement issue.

(20 marks)

3. [a] With aid of sketches, describe the causes of thermal mechanical defects which normally occur in the substrate material.

(30 marks)

[b] Briefly discuss the differences between subtractive patterning and semi-additive patterning in the substrate fabrication process.

(30 marks)

[c] Every single substrate material shipped out by the substrate manufacturer is electrically tested for any opens or shorts within the substrate. However, during the open/ short test done after the substrate material is fully assembled (with die, underfill etc), a high resistance readout was detected. Upon further investigation and failure analysis, the following defect was observed in one of the via within the substrate (refer to Figure 1). Explain what are the potential process abnormality at supplier that could lead to the incomplete plating at the via bottom. Explain the implication of this defect to the performance of the substrate.

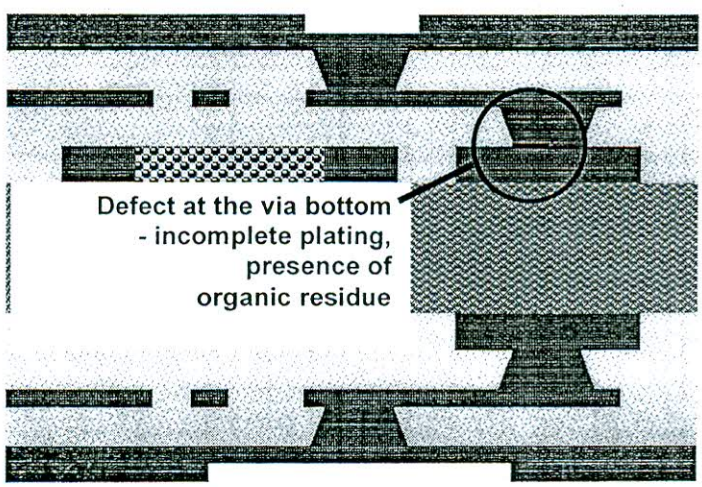

Figure 1

(40 marks)

4. [a] Explain why reliability of a product is so important to a company by giving three reasons.

(15 marks)

[b] What is "use condition"? Use examples to elaborate.

(20 marks)

[c] List five stages of a product life cycle and elaborate them.

(25 marks)

[d] What is accelerated life testing?

(20 marks)

[e] Name 4 major conditions to consider when performing accelerated testing for a semiconductor package.

(20 marks)

5. [a] The concern over toxicity of lead resulted in the change from lead solder to lead free solder as interconnect material in electronic packaging industries. A great number of researches have been reported or published regarding the candidate(s) to replace the traditional lead solder, with SAC and SnAg among the leading potential candidates. But the change also brings a number of issues yet to be resolved. Discuss these issues in details.

(50 marks)

[b] Temperature or heat exposure is one of the major factors affecting the reliability of solder joints. Thus, isothermal aging and thermal cyclic tests are often carried out to evaluate the effect of heat exposure to the solder joint. Discuss how temperature influence reliability of solder joint and what the two tests will provide (in terms of assessing reliability).

(50 marks)

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6. Consider the chip package with heat sink shown in Figure 2. The thermal resistance of the heat sink is obtained from a vendor catalog and is specified as 1.0 K/W. The silicon die is 1 cm x 1 cm and is 1 mm thick. The overall package size is 2 cm x 2 cm. The package is 5 mm thick and the mold material has a thermal conductivity of 0.8 W/mK. The package dissipates 2 W. The thermal interface material is 0.2 mm thick and has a thermal conductivity of 1.5 W/mK. The air gap between the package and the printed wiring board is expected to be 0.1 mm thick. Thermal conduction through the leads is assumed to be negligible. Ambient air temperature is 45°C. Compute the value of the die temperature, if the thermal resistance from the PWB to the air is known to equal 10 K/W.

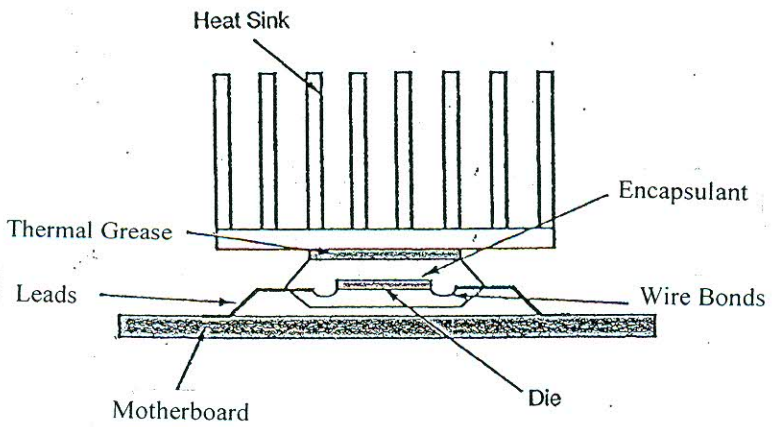

Figure 2

(100 marks)

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