UNIVERSITI SAINS MALAYSIA

Second Semester Examination

Academic Session 2004/2005

March 2005

EEE 523 – Hardware Software Co-Design

Time : 3 Hours

INSTRUCTION TO CANDIDATE:-

Please ensure that this examination paper contains **EIGHT (8)** printed pages and **SIX (6)** question before answering.

Answer **Question 1** and **any FOUR(4)** other questions

Distribution of marks for each question is given accordingly.

All questions must be answered in English.

1. (a) A VHDL Model which uses abstract constructs (such as If-Then-Else) most likely represents which of the following styles of VHDL model?

i. Behavioral Specification
ii. Data Flow Specification
iii. Structural Specification

(2 marks)

(b) Which style of VHDL Model is most appropriate for use during the early stages of a design?

i. Structural model (because components can be easily added and removed)
ii. Data Flow (RTL) model (because logic equations can be easily manipulated for design modifications)
iii. Behavioral model (because it is implementation independent)
iv. Mixture of all three methods (because the appropriate level of abstraction can be chosen which is best suited for our design)

(2 marks)

(c) Which of the following is the most accurate statement about VHDL entities and architectures?

i. A component can have many entity declarations and many architectures.
ii. A component can have many entity declarations but only one architecture.
iii. A component can have only one entity declaration and many alternative architectures.
iv. A component can have only one entity declaration and only one architecture.

(2 marks)

...3/-

(d) Logic gates may have a minimum input pulse width specification (whereby shorter input pulses are not reproduced at the output). If a VHDL model must duplicate this logic behavior, then which of the following delay models should be used?

i. inertial delay model
ii. transport delay model
iii. delta delay model
iv. any one would produce the desired result

(2 marks)

(e) Which of the following VHDL Objects provides a convenient mechanism for local storage by limiting scope to the process where they are declared.

i. signals
ii. variables
iii. constants
iv. files

(2 marks)

(f) VHDL objects of the _____ class are analogous to wires in a design schematic. They have a history of past, present and future values and their assignment is done after a certain delay.

i. signals
ii. variables
iii. constants
iv. files

(2 marks)

(g) Which of the statements below most accurately identifies any/all errors in the VHDL code fragment?

```
ENTITY test is
    PORT (a, b: IN BIT; y, z: OUT BIT; clock: INOUT BIT);
END test;

ARCHITECTURE example OF test IS
  BEGIN
    a <= y AND z AND clock;
    b <= y NOR z AND clock;
    Clock <= NOT clock;
END example;
```

i. Signals y and z are incorrectly used as inputs within the architecture

ii. Signals a and b are incorrectly assigned values within the architecture

iii. Both (a) and (b)

iv. Code is error free.

(4 marks)

(h) With reference to the VHDL behavioral model code segment below, which of the following statements is most accurate?

```
ARCHITECTURE test_behav OF test IS
VARIABLE  x : BIT := '1' ;

BEGIN
    PROCESS ( in_sig, y)
    SIGNAL y : BIT := '0';
    BEGIN
          X := in_sig XOR y;
          Y <= in_sig XOR x ;
       END PROCESS;
END test_behav;
```

i. A variable (x) is incorrectly declared in the process declaration section

ii. A signal (y) is incorrectly defined in the architecture declaration section

iii. Both the Variable and Signal declarations are incorrect.

iv. The code segment is error free

(4 marks)

2. Figure 1 below depicts the generic design flow for both the front-end and back-end approaches for an ASIC design.

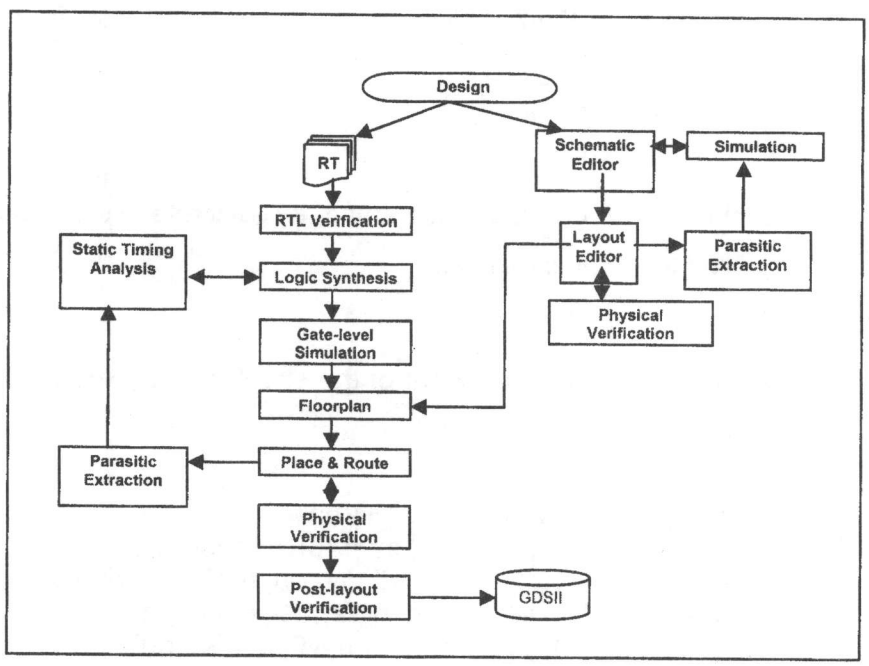

Fig 1: ASIC design flow

Describe at length both the approaches, with respect to the named blocks in the flowchart which would categorically brings the design from design specifications to tape-out.

(20 marks)

...6/-

3. Explain in details FOUR of the following:-

   i. Design abstraction levels
   ii. Inference versus instantiation
   iii. Inertial, transport & delta delay
   iv. Concurrency & sequential nature of VHDL
   v. Signal attributes
   vi. Process and sensitivity list
   vii. Testbench

(20 marks)

4. (a) Describe the VHDL design processing steps of:-

   i. Analyzation
   ii. Elaboration
   iii. Execution
   iv. Synthesis

(12 marks)

(b) Explain what do you understand by Discrete Event Simulation as applied to VHDL simulation.

(8 marks)

5. (a) Sketch a schematic diagram of the structure modeled by the following component instantiation statements:

```
decode_1: entity work.ttl_74x138(basic)
port map (c =>a(2), b=>a(1), a=>a(0), g1=>a(3),
 g2a_n=>sel_n, g2b_n=>'0', y7_n=>en_n(15), y6_n=>en_n(14),
 y5_n=>en_n(13), y4_n=>en_n(12), y3_n=>en_n(11),
 y2_n=>en_n(10), y1_n=>en_n(9), y0_n=>en_n(8);

decode_0: entity work.ttl_74x138(basic)
port map (c=>a(2), b=>a(1), a=>a(0), g1=>'1', g2a_n=>sel_n,
 g2b_n=>a(3), y7_n=>en_n(7), y6_n=>en_n(6),
 y5_n=>en_n(5),y4_n=>en_n(4),y3_n=>en_n(3),
 y2_n=>en_n(2), y1_n=>en_n(1), y0_n=>en_n(0);
```

(10 marks)

...7/-

(b) Given the assignments to the signal s made by the following process:-

```
process is begin

s<='Z', '0' after 10 ns, '1' after 30 ns;
wait for 50 ns;
s<='1' after 5 ns, 'H' after 15 ns;
wait for 50 ns;
s<='Z'
wait
end process;
```

trace the values of signals s'delayed(5ns), s'stable(5ns), s'quiet(5ns) and s'transaction. What are the values of s'last_event, s'last_active and s'last_value at time 60 ns?

(10 marks)

6. A powerful design tool for the implementation of complex digital systems on silicon is the use of VHDL program models for subsystems. The diagram below shows a Static Random Access Memory (RAM) block that is required as part of a complex electronic system. Synthesis techniques are to be employed to implement this part of the design and a VHDL model is required. Write a VHDL program model for the SRAM illustrated in Figure 1. The following section of code should be used at the start of your program to enable standard IEEE functions to be used.

```
LIBRARY ieee;
USE ieee.std_logic-1164.ALL;
USE ieee.std_arith.ALL;
USE ieee.std_logic_unsigned.ALL;
```

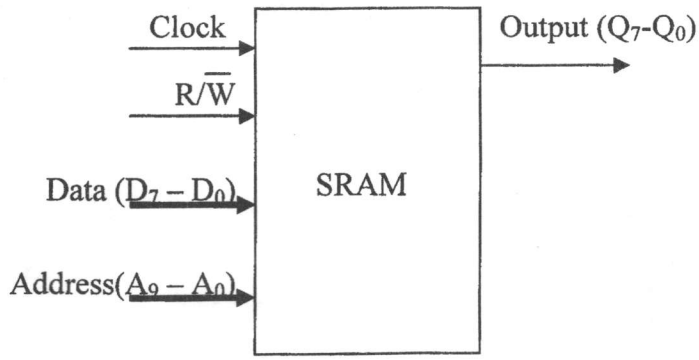

Figure 1

(20 marks)

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