UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 2011/2012

January 2012

EEE 510 – ADVANCED ANALOGUE CIRCUIT DESIGN

Time : 3 hours

INSTRUCTION TO CANDIDATE:

Please ensure that this examination paper contains **SEVEN** printed pages and **SIX** questions before answering.

Answer **FIVE** questions.

Answer to any question must start on a new page.

Distribution of marks for each question is given accordingly.

All questions must be answered in English.

1. (a)

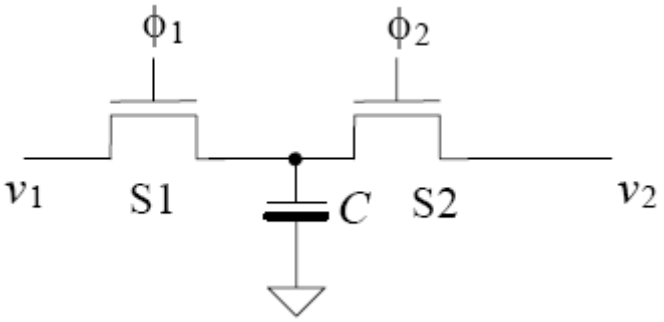

Figure 1: Switched Capacitor Resistor

(i) Explain the function of MOSFET S1 and S2.

(2 marks)

(ii) Derive the equivalent resistance of the circuit in Figure 1.

(6 marks)

(iii) Explain the limitation of the circuit in Figure 1.

(2 marks)

(b) (i) What is the operation of MOSFET whereby the behaviour of VGS is similar as VBE of bandgap device?

(2 marks)

(ii) Together with switched capacitor resistor, design a PTAT current generator. A final equation must be included together with the design.

(8 marks)

…3/-

2. (a) Given the simplified 3-bit DAC mathematical model is

$$Vout = \left(2^2\overline{D[2]} + 2^1\overline{D[1]} + 2^0\overline{D[0]}\right)(I \times R)$$

The model is based on current steering-resistor string approach. Draw the schematic of the DAC. Explain the functions of all the components in the schematic.

(12 marks)

(b) Extend the model up to 8-bit. Explain your model. (8 marks)

3.

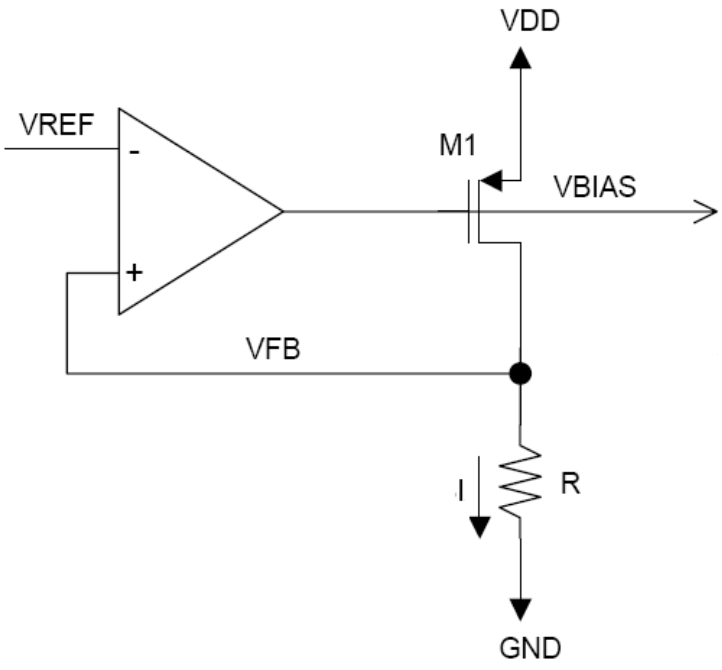

Figure 2 : Biasing circuitries for a typical current steering DAC

(a) Explain the function of the operational amplifier. (2 marks)

(b) What is the value of current I, if R is 3.7 kΩ and VREF = 1.2V? (2 marks)

(c) Assuming VDD = 3 V and M1 is in saturation, W/L = 10/2, Vtp = -1, Kp = 40 μA/V^2 , calculate the required VGS. (6 marks)

(d) Draw the basic 8-bit DAC which must include the biasing circuitries and the DAC resistor string. (10 marks)

4. Question 4 refer to Figure 1.

(a) Draw small signal model of the circuit. (10 marks)

(b) Derive the expression of R_{OUT}. (10 marks)

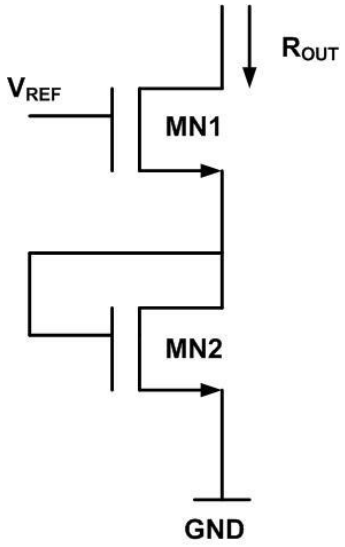

Figure 1

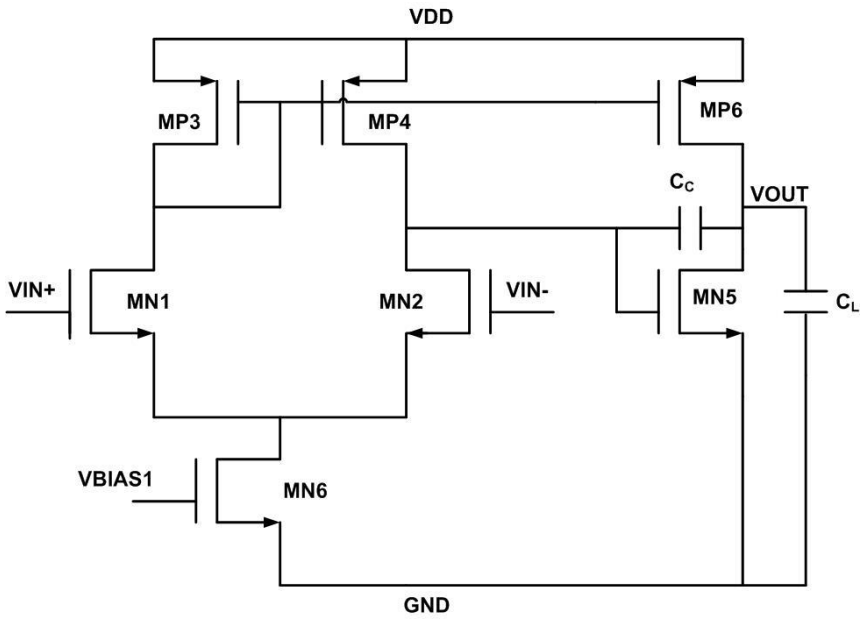

Figure 2

5. Figure 2 shows configuration of two stages CMOS OTA.

(a) Find total DC gain. (5 marks)

(b) The design is required to have 75 degree phase margin what is the ratio of $gm1/gm5$.

(5 marks)

…6/-

(c) Calculate the settling time that gives error percentage ε (0.01%) of unity configuration.

(Neglect intrinsic capacitance , VDD =1V , GBW= 500MHz , assume value of C_L = 1pf)

(10 marks)

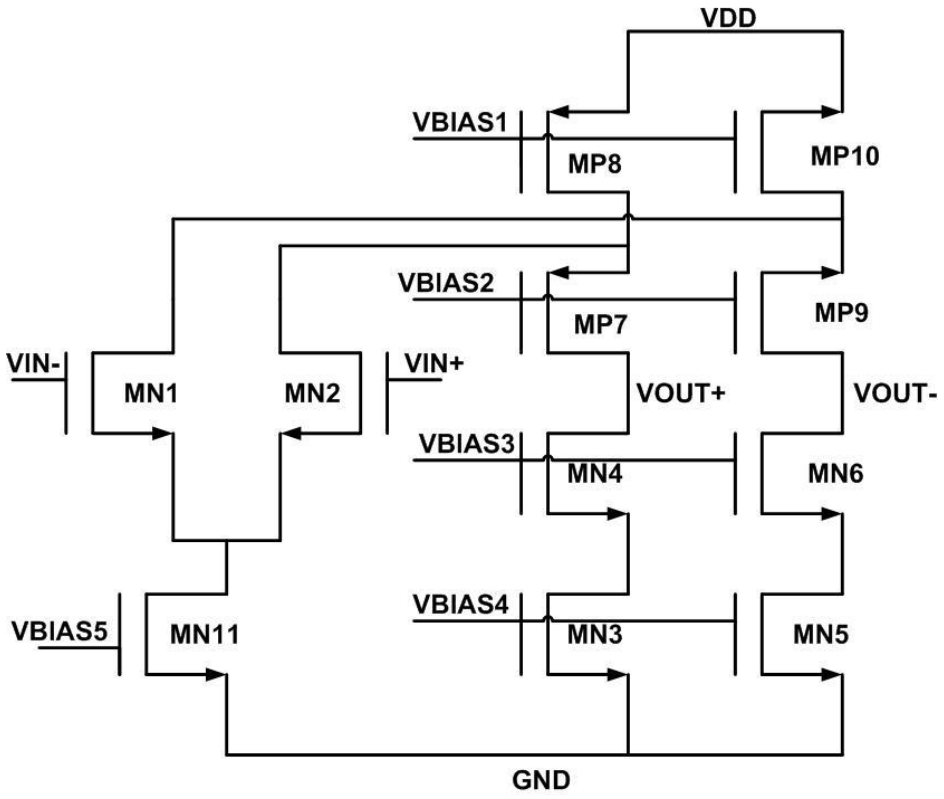

Figure 3

6 . Figure 3 shows the design of CMOS folded cascode configuration.

(a) Design continuous CMFB circuit to get stable output voltage. (10 marks)

(b) Explain how your CMFB circuit operations. (10 marks)

ooo0ooo