UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2011/2012

Januari 2012

EEE 445 – REKABENTUK LITAR ANALOG BERSEPADU

Masa : 3 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **SEPULUH** muka surat bercetak dan **Lampiran SATU** muka surat sebelum anda memulakan peperiksaan ini.

Kertas soalan ini mengandungi **ENAM** soalan

Jawab **LIMA** soalan.

Mulakan jawapan anda untuk setiap soalan pada muka surat yang baru.

Agihan markah bagi soalan diberikan disudut sebelah kanan soalan berkenaan.

Jawab semua soalan di dalam Bahasa Malaysia atau Bahasa Inggeris atau kombinasi kedua-duanya.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah diguna pakai].

"In the event of any discrepancies, the English version shall be used".

1. Rekabentuk penguat sumber-sepunya dengan beban resistif seperti yang ditunjukkan dalam litar skematik Rajah 1 mempunyai spesifikasi berikut:

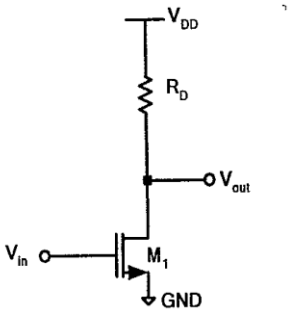
The design of common-source amplifier with resistive load as shown in schematic circuit of Figure 1 below has the following specifications:

- V_{DD} = 1.8 dan M_1 dalam tepuan dengan voltan output minima bagi mengekalkan M_1 dalam tepuan adalah 0.2V.

  V_{DD} = 1.8V and M_1 in saturation with minimum possible output voltage to keep M_1 in saturation is 0.2V

- Jumlah penggunaan kuasa penguat adalah 0.9mW.
  Total power consumption of amplifier is 0.9mW.

- Nilai gandaan mutlak adalah 10 untuk L=0.4 μm
  Absolute value of gain is 10 for L=0.4 μm



Rajah 1 : Penguat Sumber-Sepunya
Figure 1 : Common-Source amplifier

Diberi parameter teknologi bagi transistor NMOS seperti berikut:
Given the following technology parameter for the NMOS transistor:

$\lambda_{(NMOS)} = 0$, $\gamma=0$, $V_{TH(NMOS)} = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$.

Cari nilai-nilai berikut.
Find the following values.

(i) Aras DC bagi input.
DC level of the input (4 markah/marks)

(ii) Lebar (W_1) bagi transistor M_1.
Width (W_1) of transistor M_1 (4 markah/marks)

(iii) R_D (4 markah/marks)

(iv) Aras nominal dc bias bagi nod output.
Nominal dc bias level of the output node. (4 markah/marks)

(v) Ayunan maksimum isyarat output bagi isyarat output simetri.
Maximum output signal swing for a symmetric output signal
(4 markah/marks)

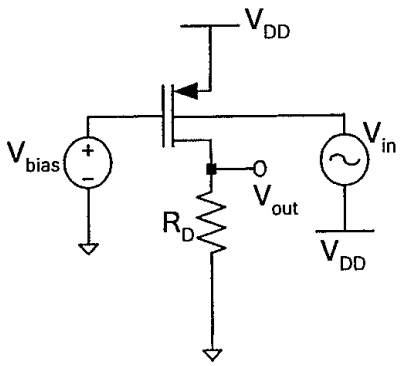
2. (a) Terminal badan suatu transistor boleh digunakan sebagai input suatu penguat. Pertimbangkan litar bias PMOS seperti yang ditunjukkan dalam litar Rajah 2. Bagi Vbias = 1.4V, hitungkan untung isyarat-kecil bagi penguat PMOS, dengan mengambilkira $g_{mb} = \eta g_m$.

It is possible to use the bulk terminal of a transistor as an input of an amplifier. Consider the PMOS bias circuit shown in Figure 2. For Vbias = 1.4V, calculate the small-signal gain of the PMOS amplifier, considering $g_{mb} = \eta g_m$.

Andaikan parameter PMOS:
Assume PMOS parameters:

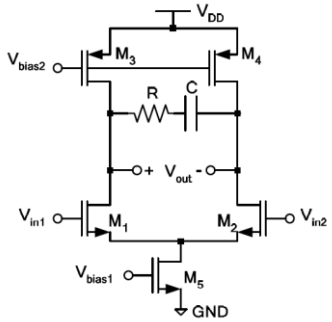
λ=0, η=0.2, $V_{TH(PMOS)}$ = -0.6V, $\mu_p C_{ox}$ =100 μA/V^2, R_D = 1kΩ, $(W/L)_{PMOS}$=20, dan/*and* V_{DD} = 3V.

(8 markah/marks)



Rajah 2
Figure 2

2. (b)



Rajah 3
Figure 3

Bagi litar di atas, andai transistor M_1 dan M_2 serupa, dan M_3 dan M_4 serupa dan γ=0, $\lambda \neq 0$:
In the above circuit, assume transistor M_1 and M_2, and M_3 and M_4 are identical and γ=0, $\lambda \neq 0$:

…5/-

(i) Tentukan ungkapan bagi gandaan voltan pembeza isyarat-kecil $\frac{V_{out}}{V_{in1} - V_{in2}}$ bagi litar tersebut.

Find the expression for the small-signal differential voltage gain $\frac{V_{out}}{V_{in1} - V_{in2}}$ *of the circuit.*

(ii) Apakah gandaan litar pada frekuensi rendah?
What is the gain of the circuit at very low frequencies?

(iii) Apakah gandaan litar pada frekensi tinggi?
What is the gain of the circuit at very high frequencies?

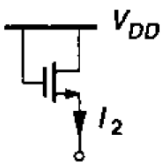
(12 markah/marks)

3. (a) Jelaskan mengapa struktur dalam litar-litar di bawah tidak dapat beroperasi sebagai sumber arus walaupun transistor-transistor adalah dalam tepuan.

Explain why the structures in the Figure below cannot operate as current sources even though the transistors are in saturation.

(4 markah/marks)

Rajah 4(a)
Figure 4(a)

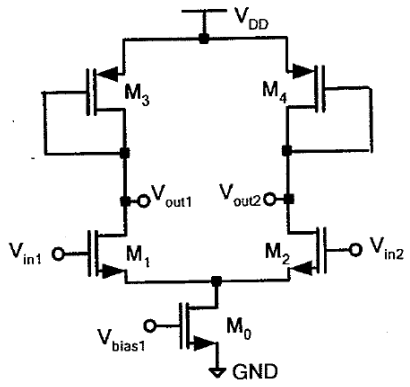


Rajah 4(b)
Figure 4(b)

(b) Rekabentuk penguat pembeza simetri berdasarkan litar dalam Rajah 5, dengan spesifikasi berikut:

Design a symmetric differential amplifier based on the circuit in Figure 5 with the following design specifications:

- V_{DD} = 1.8V
- Jumlah penggunaan kuasa 1.8mW
  Total power consumption of 1.8 mW
- Aras DC output 0.9V.
  Output DC level of 0.9V
- Jumlah gandaan 5.
  Total gain of 5
- L = 0.4 μm untuk semua peranti.
  L = 0.4 μm for all devices



Rajah 5: Penguat pembeza simetri
Figure 5 : Symmetric Differential Amplifier

Andaikan voltan minimum yang diperlukan pada salir M_0 untuk mengekalkannya pada tepuan adalah 0.2V.

Assume that the minimum required voltage at the drain of M_0 to keep it in saturation is 0.2V.

…7/-

Parameter teknologi adalah:
The technology parameters are:

$\lambda_{(NMOS, PMOS)} = 0$, $\gamma=0$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$
$\mu_p C_{ox} = 0.5\ mA/V^2$, and $V_{DD} = 1.8V$.

(i) Tentukan V_{bias1}, dan kesemua lebar transistor (W0, W1, W2, W3 dan W4)
Find Vbias1, and all the transistor widths (W0, W1, W2, W3 and W4)

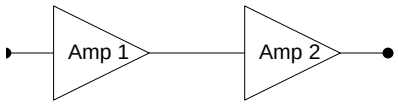
(ii) Tentukan minimum dan maksimum aras input DC.
Find the minimum and maximum allowable input DC levels.

(16 markah/marks)

4. (a) Lukiskan penguat kendalian menyongsang dengan gandaan $-\frac{R_f}{R_S}$ dan huraikan jumlah hingar keluaran.

Draw an inverting operational amplifier with gain of $-\frac{R_f}{R_S}$ *and derive the total output noise.*

(6 markah/marks)



Rajah 6: Dua lata penguat kendalian menyongsang
Figure 6: Two inverting operational amplifier in cascade

(b) Sekiranya R_S = 50 Ω untuk penguat 1 dan 2 (Rajah 6), tentukan jumlah hingar keluaran untuk setiap penguat sekiranya R_f = 100 Ω untuk penguat 1 dan 200 Ω untuk penguat 2.

If source resistance, R_S = 50 Ω for amplifier 1 and amplifier 2 (Figure 6), determine total output noise voltage for each amplifier if feedback resistance, R_f = 100 Ω for amplifier 1 and 200 Ω for amplifier 2.

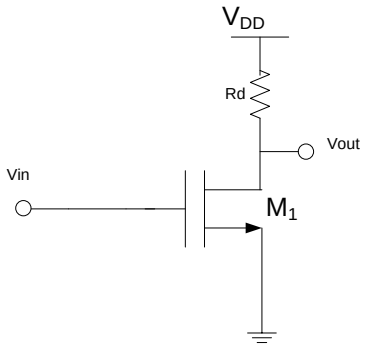
(8 markah/marks)

(c) Kirakan faktor hingar bagi setiap penguat.
Calculate the noise factor for each amplifier.

(6 markah/marks)

5. Fungsi pindah bagi litar dalam Rajah 7 adalah
The transfer function of circuit in Figure 7 is,

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-g_m R_D}{(1+\frac{s}{\omega_{in}})(1+\frac{s}{\omega_{out}})}$$



Rajah 7: Penguat Punca Sepunya
Figure 7: Common source amplifier

(a) Tentukan ungkapan untuk kutub masukan dan kirakan nilai ia sekiranya if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF dan C_{db} = 0.001 pF.

Determine the expression for input pole and calculate the value if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF .

(7 markah/marks)

(b) Tentukan ungkapan untuk kutub keluaran dan kirakan nilai ia sekiranya if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF dan C_{db} = 0.001 pF.

Determine the expression for output pole calculate the value if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF.

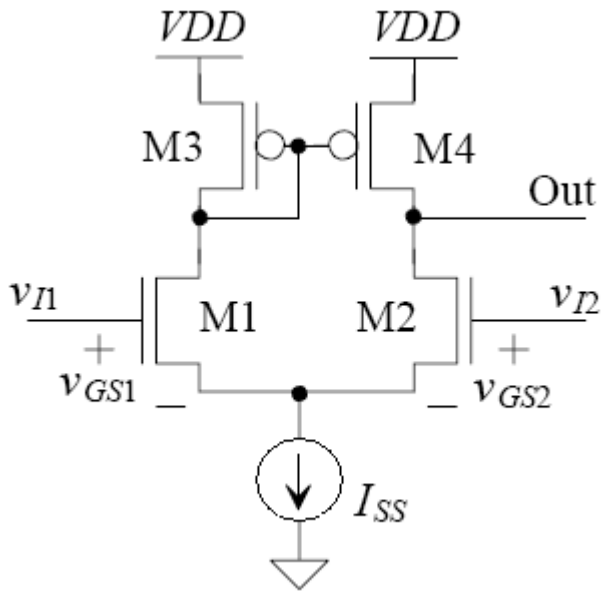
(7 markah/marks)

(c) Apakan nilai gandaan yang diperlukan sekiranya jalur yang ditentukan ialah 15 MHz?. Beban ialah 50 pF. Dengan bebanan tersebut, apakah pandangan anda mengenai kestabilan litar itu

What is the required gain if the wanted bandwidth is 15 MHz if external load is 50 pF? With the capacitive load, what is your prediction of the stability of the circuit

(6 markah/marks)

6.



Rajah 8: Penguat Kebezaan

Figure 8: Differential Amplifier

(a) Sekiranya W/L bagi M1 dan M2 ialah 10/2, $\mu_n.C_{ox}$ = 120 μA/V^2 dan I_{SS} = 50 μA. Jika V_{I2} = 2.4 V, kirakan maksimum dan minimum voltan bagi get M1 supaya M1 dan M2 tidak tutup.

Assume that W/L of M1 and M2 is 10/2, $\mu_n.C_{ox}$ = 120 μA/V^2 and I_{SS} = 50 μA. If V_{I2} = 2.4 V (common mode voltage), calculate the maximum and minimum voltage on the gate of M1 that ensures neither M1 nor M2 shut off. Draw I_{D2} vs V_{I2}.

(8 markah/marks)

(b) (i) Lukiskan litar setara isyarat kecil untuk Rajah 8.
Draw small signal equivalent circuit for Figure 8.

(6 markah/marks)

(ii) Apakah tertib pertama gandaan mod kebezaan?
What is the first order differential mode gain?

(3 markah/marks)

(iii) Kira gandaan mod kebezaan apabila λ_n = 0.01 V^{-1} dan λ_p = 0.0125 V^{-1}
Calculate the differential mode gain if λ_n = 0.01 V^{-1} and λ_p = 0.0125 V^{-1}

(3 markah/marks)

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Lampiran/Appendix: **[EEE 445]**

SenaraiPersamaanUmum/List of general equations

1. Current Equations for NMOS:

$$I_D = I_{DS} = \begin{cases} 0 \quad ; if\ V_{GS} < V_{TH}\ (Cut-off) \\ \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DS} \quad ; if\ V_{GS} > V_{TH}\ , V_{DS} << 2(V_{GS} - V_{TH})\ (Deep\ Triode) \\ \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right] \quad ; if\ V_{GS} > V_{TH}\ , V_{DS} < V_{GS} - V_{TH}\ (Triode) \\ \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \quad ; if\ V_{GS} > V_{TH}\ , V_{DS} > V_{GS} - V_{TH}\ (Saturation) \end{cases}$$

2. Current Equations for PMOS:

$$I_D = I_{SD} = \begin{cases} 0 \quad ; if\ V_{SG} < |V_{TH}|\ (Cut-off) \\ \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{SG} - |V_{TH}|) \cdot V_{SD} \quad ; if\ V_{SG} > |V_{TH}|, V_{SD} << 2(V_{SG} - |V_{TH}|)\ (Deep\ Triode) \\ \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{SG} - |V_{TH}|) \cdot V_{SD} - \frac{1}{2} \cdot V_{SD}^2 \right] \quad ; if\ V_{SG} > |V_{TH}|, V_{SD} < V_{SG} - |V_{TH}|\ (Triode) \\ \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{SG} - |V_{TH}|)^2 \quad ; if\ V_{SG} > |V_{TH}|, V_{SD} > V_{SG} - |V_{TH}|\ (Saturation) \end{cases}$$

3. Transconductance in triode:

$$g_m = \frac{\partial}{\partial V_{GS}} \left(\mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right] \right) \Big|_{V_{DS} = Const.}$$
$$= \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS}$$

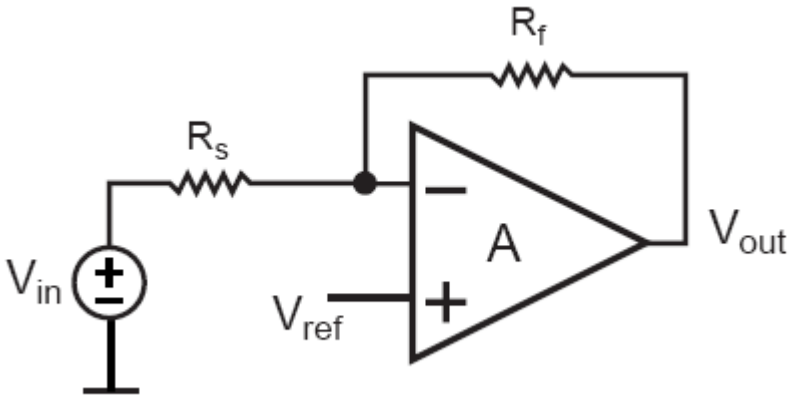
4. Transconductance in saturation:

$$g_m = \frac{\partial}{\partial V_{GS}} \left(\frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \right) \Big|_{V_{DS} = Const.}$$
$$= \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})$$

EEE445 – DR. ARJUNA (SOLUTION)
SEM I, S/A 2011/2012, JAN. 2012

Marking Scheme

4(a).



$$\overline{v_{nout(tot)}^2} \approx \left(\frac{-R_f}{R_s}\right)^2 \overline{e_{nRs}^2} + \overline{e_{nRf}^2}$$

(6 pts)

(b)

Amplifier 1 : Output noise voltage = 2^2 * $4KTR_S$ + $4KTR_F$
= 4*8.28E-19 + 1.65E-18 = 4.968E-18 V^2/Hz (4 pts)

Amplifier 2: Output noise voltage = 4^2 * $4KTR_S$ + $4KTR_F$
= 16*8.28E-19 + 3.312E-18 = 1.65E-17 V^2/Hz (4 pts)

(c)

Amplifier = 1 + Rs/Rf = 1 + 50/100 = 1.5
Amplifier = 1 + Rs/Rf = 1 + 50/200 = 1.25(6 pts)

5.
a). Determine the expression for input pole.

$$f_{p,in} = \frac{1}{2\pi R_S \left[C_{GS} + (1 + g_m R_D) C_{GD}\right]}$$

b). Determine the expression for output pole.

$$f_{p,out} = \frac{1}{2\pi \left[(C_{GD} + C_{DB}) R_D\right]}$$

c). Gain bandwidth product=gm/Cout , = 0.02/50 pF
Gain=Gain bandwidth product/Bandwidth
Gain = 0.02/50 pF /15e6 =26.6

5. a).

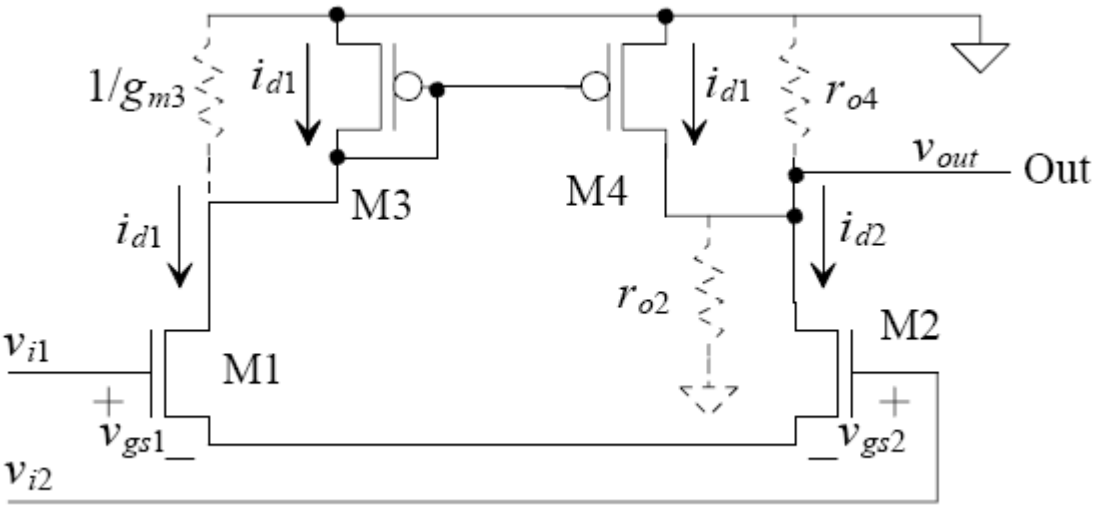
V1Imax= SQRT(2.L.ISS/ W.μ_n.C_{ox}) + VI2

V1Imax= SQRT(2.L.ISS/ W.μ_n.C_{ox}) + 2.4 V
Replace all given parameters.

V1Imax= 0.408 + 2.4 V = 2.808 V
V1Imin= 2.4 – 0.408 = 1.992 V.

b).

i.



Mark will be given based on.

1. Vdd is changed to ground
2. ISS replace with an open.
3. ro2 and ro4 are drawn.

ii. Based on the given Figure,
Ad = gm.(ro2//ro4).

iii. gm = 1.73 e-4 , based on given parameters.
ro2=1/ λ_n Id = 4 e6 Ohm ro4=1/ λ_p Id = 3.2e6

so gain = 1.73e-4 x 1.77e6 = 307