UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2005/2006

November 2005

EEE 320 – MIKROPEMPROSES II

Masa : 2 Jam

ARAHAN KEPADA CALON:-

Sila pastikan kertas peperiksaan ini mengandungi **TUJUH (7)** muka surat beserta **Lampiran (5 muka surat)** bercetak dan **EMPAT (4)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **TIGA (3)** soalan.

Agihan markah diberikan di sudut sebelah kanan soalan berkenaan.

Semua soalan hendaklah dijawab di dalam Bahasa Malaysia.

...2/-

1. (a) Terangkan perbezaan antara mikropemproses dan mikro pengawal?

What are the differences between microprocessor and microcontroller?

(20%)

(b) Tuliskan satu program untuk menyalin 10 bait data dari lokasi RAM bermula daripada alamat 35H kepada alamat yang bermula dengan 60H.

Write a program to copy a block of 10 bytes of data from RAM locations starting at 35H to RAM locations starting at 60H.

(20%)

(c) Tuliskan satu program untuk menyimpan data 44 (decimal) pada alamat 12H seperti yang ditunjukkan dalam Rajah 1.

Write a program to store the value 44 decimal at address 12H as shown in Figure 1.

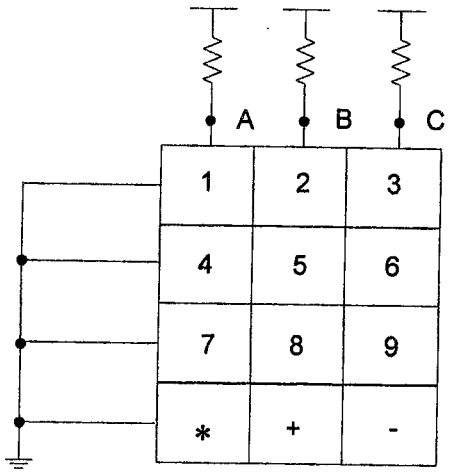
(20%)

...3/-

(c) nombor 9 ditekan
number 9 is pressed

(d) nombor 3 ditekan
number 3 is pressed

(10%)



Rajah 2
Figure 2

(ii) Tuliskan satu program sekiranya pin 5 ditekan, data pada port A akan dihantar ke port B.

Write a program if number 5 is pressed, data from port A will be sent to port B.

(30%)

2. (i) (a) Nyatakan tanda-tanda yang diakibatkan oleh masalah hingar elektrik?

What are the symptoms of electrical noise?

(20%)

...5/-

(b) Terangkan sumber-sumber hingar elektrik dalam litar elektronik.

Explain the sources of electrical noise in electronic circuit.

(30%)

(ii) (c) Nyatakan beberapa keperluan sistem dan spesifikasi sistem untuk merekabentuk satu sistem pengawal lampu isyarat bagi jalan 4 laluan dengan 2 lorong menggunakan unit mikropengawal.

State a few system requirements and system specifications for designing a traffic light control system for a 4-way road with 2 lanes using a microcontroller.

(20%)

(d) Nyatakan garis panduan aturcara untuk algoritma pengawal trafik menggunakan KOD PSEUDO dan CARTA ALIR bagi sistem paparan lampu isyarat yang telah anda pertimbangkan dalam bahagian (a).

Write the program outline for the traffic control algorithm using PSEUDO CODE and FLOWCHART for the traffic light display system that you have considered in part (a).

(30%)

3. (a) Anggapkan kita mempunyai 6 bait data heksadesimal : 4CH, 32H, 45H, 52H, 23H, 2BH. Dapatkan bait semak-jumlah dan pastikan integriti (keadaan lengkap) data. Tunjukkan bagaimana semak-jumlah mengesan kesilapan apabila bait keempat ditukarkan kepada 62H.

Assume that we have 6 bytes of hexadecimal data : 4CH, 32H, 45H, 52H, 23H, 2BH. Find the checksum byte and ensure data integrity. Show how checksum detects error when the fourth byte is changed to 62H.

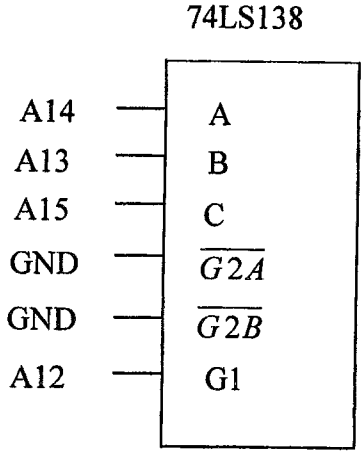
(15%)

...6/-

(b) Untuk rekabentuk yang diberikan, dapatkan julat alamat untuk setiap keluaran Y iaitu Y0 hingga Y7 bagi 74LS138 yang disambungkan kepada ingatan 4K x 8.

For the given design find the address range for each of the Y outputs Y0 to Y7 of the 74LS138 connected to 4K x 8 memory chips.

(20%)



(c) ROM data luaran mempunyai jadual lihat-rujukan untuk punca-punca kiub nombor 0 hingga 9 bermula pada alamat 0. Tulis satu aturcara untuk menyalin kandungan jadual ke dalam RAM dalaman bermula pada alamat 20H. Bincangkan peranan pin PSEN dalam mengakses kod-kod aturcara dalam cip dan luar cip.

The external data ROM has a look-up table for the cube roots of numbers 0 to 9 starting at address 0. Write a program to copy the table contents into the internal RAM starting at address 20H. Discuss the role of PSEN pin in accessing on-chip and off-chip program codes.

(25%)

...7/-

(d) Tunjukkan rekabentuk sistem berasaskan 8051 dengan 16K bait RAM data luaran. Tuliskan satu aturcara untuk membaca 100 bait data dari port A 8255 dan simpankan data ke RAM luaran bermula pada lokasi 3000H.

Show the design of an 8051 based system with 16K bytes of external data RAM. Write a program to read 100 bytes of data from port A of 8255 and save the data in external RAM starting at location 3000H.

(40%)

4. (a) Rekabentuk Komputer Terbenam mempunyai kekangan-kekangan yang ketat bagi kedua-dua kes fungsi dan perlaksanaan. Terangkan kekangan-kekangan yang perlu diambil kira semasa rekabentuk sistem.

Designing Embedded Computers have tight constraints on both functionality and implementation cases. Explain the constraints which need to be considered when designing the system.

(50%)

(b) Untuk memastikan kompetitif dalam pasaran, pereka perlu mengambil kira empat keperluan utama semasa membuat keputusan untuk merekabentuk. Terangkan kesemua keperluan tersebut.

In order to be competitive in the marketplace, the designer must take account four main requirements when making design decision. Explain all the requirements.

(50%)

oooOooo

MCS®-51 INSTRUCTION SET

Table 10. 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings(1)

Instruction	Flag C	OV	AC	Instruction	Flag C	OV	AC
ADD	X	X	X	CLR C	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	O	X		ANL C,/bit	X		
DIV	O	X		ORL C,bit	X		
DA	X			ORL C,bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Note on instruction set and addressing modes:

Rn — Register R7–R0 of the currently selected Register Bank.

direct — 8-bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR [i.e., I/O port, control register, status register, etc. (128–255)].

@Ri — 8-bit internal data RAM location (0–255) addressed indirectly through register R1 or R0.

#data — 8-bit constant included in instruction.

#data 16 — 16-bit constant included in instruction.

addr 16 — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.

addr 11 — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

rel — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

bit — Direct Addressed bit in Internal Data RAM or Special Function Register.

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with Carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with Carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC	A,#data	Add immediate data to Acc with Carry	2	12
SUBB	A,Rn	Subtract Register from Acc with borrow	1	12
SUBB	A,direct	Subtract direct byte from Acc with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB	A,#data	Subtract immediate data from Acc with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment direct RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS (Continued)				
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A & B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12

Mnemonic		Description	Byte	Oscillator Period
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	12
RLC	A	Rotate Accumulator Left through the Carry	1	12
RR	A	Rotate Accumulator Right	1	12
RRC	A	Rotate Accumulator Right through the Carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	Rn,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
DATA TRANSFER (Continued)				
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri, # data	Move immediate data to indirect RAM	2	12
MOV	DPTR, # data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A + DPTR	Move Code byte relative to DPTR to Acc	1	24
MOVC	A,@A + PC	Move Code byte relative to PC to Acc	1	24
MOVX	A,@Ri	Move External RAM (8-bit addr) to Acc	1	24
MOVX	A,@DPTR	Move External RAM (16-bit addr) to Acc	1	24
MOVX	@Ri,A	Move Acc to External RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move Acc to External RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order Digit indirect RAM with Acc	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set Carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement Carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to CARRY	2	24
ANL	C,/bit	AND complement of direct bit to Carry	2	24
ORL	C,bit	OR direct bit to Carry	2	24
ORL	C,/bit	OR complement of direct bit to Carry	2	24
MOV	C,bit	Move direct bit to Carry	2	12
MOV	bit,C	Move Carry to direct bit	2	24
JC	rel	Jump if Carry is set	2	24
JNC	rel	Jump if Carry not set	2	24
JB	bit,rel	Jump if direct Bit is set	3	24
JNB	bit,rel	Jump if direct Bit is Not set	3	24
JBC	bit,rel	Jump if direct Bit is set & clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute Subroutine Call	2	24
LCALL	addr16	Long Subroutine Call	3	24
RET		Return from Subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute Jump	2	24
LJMP	addr16	Long Jump	3	24
SJMP	rel	Short Jump (relative addr)	2	24

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)				
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is Zero	2	24
JNZ	rel	Jump if Accumulator is Not Zero	2	24
CJNE	A,direct,rel	Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE	A, # data,rel	Compare immediate to Acc and Jump if Not Equal	3	24
CJNE	Rn, # data,rel	Compare immediate to register and Jump if Not Equal	3	24
CJNE	@Ri, # data,rel	Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ	Rn,rel	Decrement register and Jump if Not Zero	2	24
DJNZ	direct,rel	Decrement direct byte and Jump if Not Zero	3	24
NOP		No Operation	1	12

1.

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				Timer 0			

TMOD Register

2.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TCON Register

3.

--	--	PT2	PS	PT1	PX1	PT0	PX0

IP Register

4.

EA	--	ET2	ES	ET1	EX1	ET0	EX0

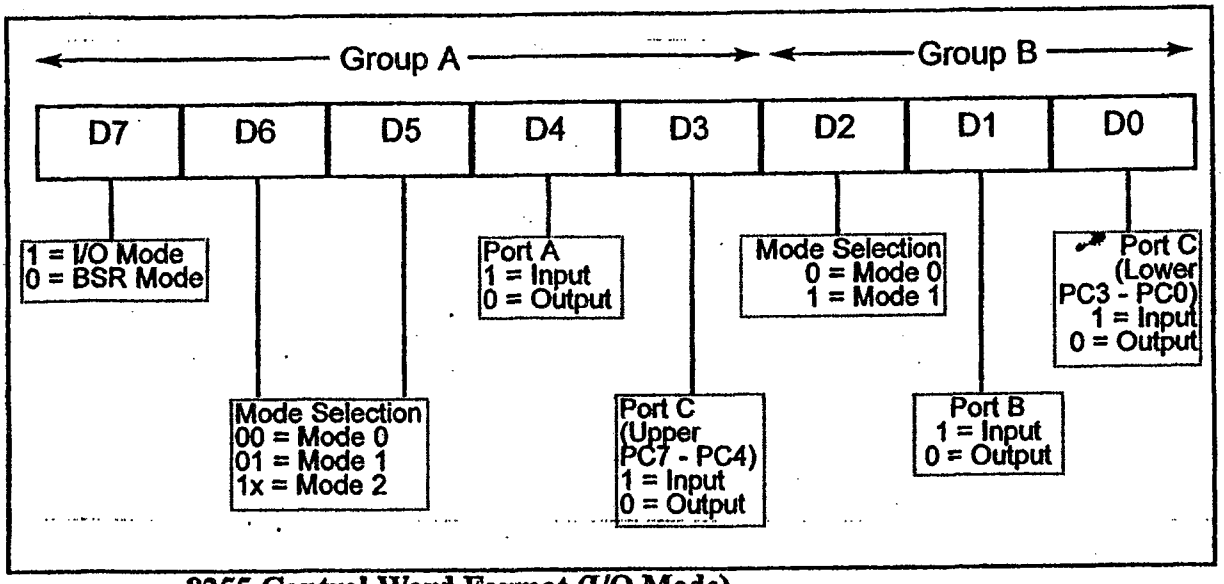
IE Register

5.

CY	AC	FO	RSI	RSO	OV	- -	P

PSW Register

6.



8255 Control Word Format (I/O Mode)