UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 2009/2010

November 2009

EBB 526/3 – Electronic Packaging

Duration : 3 hours

Please ensure that this examination paper contains SIX printed pages before you begin the examination.

This paper consists of SIX questions.

Instruction: Answer **FIVE** questions. If candidate answers more than five questions only the first five questions answered in the answer script would be examined.

The answers to all questions must start on a new page.

All questions must be answered in English.

1. [a] (i) Describe what is Moore's Law.

(ii) High filler content capillary underfills (CUF) have high modulus and low coefficient of thermal expansion (CTE). Discuss why we need to optimized filler content for optimum reliability performance.

(30 marks)

[b] A typical formulation of capillary underfill (CUF) is shown in Table 1.

(i) Describe the function of each of the ingredients.

(ii) What is the effect to the curing process and degree of crosslink if catalyst is not used?

(iii) What is the effect to the underfill if curing agent is not used?

(iv) What is the effect to the underfill if 10% of curing agent is used?

(v) How to remove bubbles in the underfill if defoamer is not used?

Table 1: Typical formulation of capillary underfill

Ingredients	**%**
Epoxy resin	30
Curing agent	5
Filler (SiO_2)	60
Catalyst	2
Surfactant	2
Defoamer	1

(40 marks)

[c] Describe the functions of thermal interface material (TIM) in flip chip package? Give and explain four (4) examples and justification of good TIM properties.

(30 marks)

2. [a] Explain, with the help of appropriate diagram, about a reflow profile and defects commonly associated with the reflow profile of a solder joint.

(40 marks)

[b] Discuss about the following defects. Suggest possible cause and method(s) to eliminate them.

(60 marks)

3. [a] Draw a curve for a typical product reliability failure pattern. Name and label the curve accordingly.

(30 marks)

[b] Consequently, describe each of the 3 sections you mentioned in [a].

(30 marks)

[c] With respect to the Differential Scanning Calorimetry (DSC), gives definitions to the following:

(i) Calorimetry
(ii) Differential
(iii) Scanning
(iv) Exothermic reaction
(v) Endothermic reaction

(40 marks)

4. Consider the chip package with heat sink shown in Figure 1. The thermal resistance of the heat sink is obtained from a vendor catalog and is specified as 1.0 K/W. The silicon die is 1 cm x 1 cm and is 1 mm thick. The overall package size is 2 cm x 2 cm. The package is 5 mm thick and the mold material has a thermal conductivity of 0.8 W/mK. The package dissipates 2 W. The thermal interface material is 0.2 mm thick and has a thermal conductivity of 1.5 W/mK. The air gap between the package and the printed wiring board is expected to be 0.1 mm thick. Thermal conduction through the leads is assumed to be negligible. Ambient air temperature is 45^{o}C. Compute the value of the die temperature, if the thermal resistance from the PWB to the air is known to equal 10 K/W.

Figure 1

(100 marks)

5. [a] Every single substrate material shipped out by the substrate manufacturer is electrically tested for any opens or shorts within the substrate. However, during the open/ short test done after the substrate material is fully assembled (with die, underfill etc), a high resistance readout was detected. Upon further investigation and failure analysis, the following defect was observed in one of the via within the substrate (refer to Figure 2).

(i) Explain why the defect was not detected by supplier. Why the defect only detected after the substrate is fully assembled with die etc. Provide assumptions made in your answers.

(30 marks)

(ii) Explain what are the potential process abnormality at supplier that could lead to the incomplete plating at the via bottom. Use your imaginations.

(20 marks)

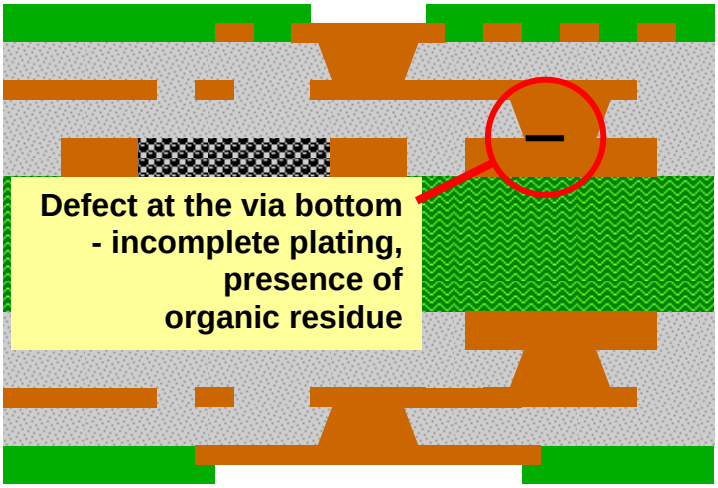

Figure 2

[b] Discuss similarity and difference of electroless and electrolytic copper plating.

(20 marks)

[c] With aid of sketches, briefly explain the differences between subtractive patterning and semi-additive patterning.

(30 marks)

6. [a] Briefly explain the implication of Moore's Law on the development of integrated circuits.

(40 marks)

[b] Sketch and label a cross sectional view of a flip chip electronic package.

(30 marks)

[c] Explain the functions of an electronic package.

(30 marks)

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