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Etching Effect on the Formation of Silicon Nanowire Transistor Patterned by AFM Lithography

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ABSTRACT

Anisotropic etching of silicon has been widely used in fabrication of MEMS devices for many years. In this work, TMAH and KOH with IPA are used to etch silicon nanowire transistor patterns. The silicon nanowire transistor with a silicon nanowire as a channel, source, drain, and lateral gate pads structure was fabricated on silicon-on-insulator substrate. AFM lithography technique was performed to create the nanoscale silicon oxide mask patterns. Patterning parameters such as applied tip voltage and writing speed were well controlled in order to produce as pre-designed transistor structure. One of the patterns was etched in TMAH solution to form oxide-capped silicon nanowire transistor structure. Meanwhile, another sample is etched in KOH with IPA additive solution to improve its etching selectivity. The AFM patterned structure is found to have shadows at surrounding the pads due to the high electric field generated by AFM tip. These ultra thin oxide shadows made the TMAH etched pattern produce bigger pads size. On the other hand, the KOH with IPA additive etched device produce smaller and square shape pads. From electrical characteristics found that both of the TMAH and KOH etched device structures exhibit p-type semiconductor properties. However, the KOH etched device gave small effect to the electrical characteristic curves at varied gate voltage.

1 INTRODUCTION

Etching process plays the important role in lithography process to produce the desired patterning structure. Even the dry etching will produce an optimum result; wet etching will give a better choice in term of cost, etching rate and selectivity (Yang et al., 2005; Camon and Moktadir, 1997; van Veenendaal et al., 2001; Acero et al., 1995; Zubel and Kramkowska, 2001; Biswas and Kal, 2006). This technique will give anisotropic and isotropic result depends on the desired application. Anisotropic etching is widely used in producing the micromechanical structures and device. There are inorganic and organic etchants was use in this process, the most common inorganic etchant are sodium hydroxide (NaOH) and potassium hydroxide (KOH). Recently the most popular etchant as an organic etchant is tetra methyl ammonium hydroxide (TMAH) and water solution ethylendiamine pyrocatecol (EDP). EDP has high toxicity, requires special apparatus and careful handling as it produces reaction gases which are health hazardous and require special safety measurement; based on that factor, researchers try to avoid using this etchant. These anisotropic properties of this etchant are used to creating the coveted etched shape and structures. The etch rate of these etchants are interdependence to defining the geometrical shape of the microstructure by individual crystal planes (van Veenendaal et al., 2001; Zubel and Kramkowska, 2008; Pennelli et al., 2006).

TMAH in water solution is gaining popularity despite as highly cost and complex etch setup, because it's nontoxic and non explosive. It also has satisfactory etching characteristic and selectivity of

silicon dissolution with respect to silicon dioxide (Zubel and Kramkowska, 2001; Acero et al., 1995). In other word it has good selectivity to SiO_2. Hence, KOH has excellent etching properties with respect to anisotropy, etch rate and surface quality, by adding the isopropyl alcohol it will reduces the undercutting of convex corners, which is desirable for etching the silicon (Biswas and Kal, 2006). Without no doubt KOH is the most useful in implementation to device structure. Even the anisotropy is quite high but the decrease of etching rate with boron concentration is smoother. It means the selectivity to respect of silicon dioxide is poor for long time etching. In some cases, TMAH is more useful for this application. The selectivity is higher but the anisotropy is low (van Veenendaal et al., 2001; Zubel and Kramkowska, 2001; Biswas and Kal, 2006). There are few referred journals are discussing these phenomena and by adding some additive is the key to improve the weaknesses. Unfortunately, most of the models are more discussing for microstructures, but less or not least only few discussing in nanostructure.

In this work reported effect of etchant solution on the fabrication of silicon nanowire transistor by atomic force microscopy (AFM) nanolithography. The fabricated device structures made of a silicon nanowire as a channel, a source pad, a drain pad, and a lateral gate pad. The structure formed by a thin layer silicon oxide (~4nm) grown by using AFM tip. The device patterning parameters, which relative humidity, exposure time, applied bias voltage, type of cantilever, tip speed and AFM operation mode are keep constant. The designed transistor was then etched with anisotropic-type etchant of TMAH or KOH with additive of IPA at the same temperature and etching time.

2 MATERIALS AND METHOD

The sample with a surface area of 1 to 1.5 cm^2 was prepared using silicon-on-insulator (SOI) <100> wafer (Soitec, Boron doped, resistivity 5- 10 Ωm, diameter 6-inch, Si layer thickness ~100nm and SiO_2 thickness ~200nm). The wafer was used as-grown without any heat treatment process. These small pieces of SOI substrates were cleaned as standard procedure silicon cleaning process. All the cleaned samples pre-treated with hydrofluoric acid (HF) to provide the same starting condition for all samples. The fabrication of silicon nanowire transistor structure was performed by AFM nanolithography technique using a SII Nanotechnology, SPA300HV machine. The schematic of designed transistor is shown in Figure 1. All the necessaries parameters for this technique are constantly control to perform the same fabrication condition of samples. The process was further continuing with the etching process by using anisotropic etchant: (i) inorganic etchant of 30%wt. KOH with additive of 10%vol. IPA, and (ii) organic etchant of water solution of 25%wt. TMAH. This process was performed at temperature of 65^oC, stirred at 1000 rpm and 25 seconds etching time. The sample was then rinse with DI-water. Further, the TMAH or KOH etched samples are re-etched with HF solution to remove the silicon oxide mask layer in order to produce a completed silicon nanowire transistor. The electrical characterization was performed at room temperature and ambient air using a semiconductor parameter analyzer (Agilent) and Lakeshore probe station.

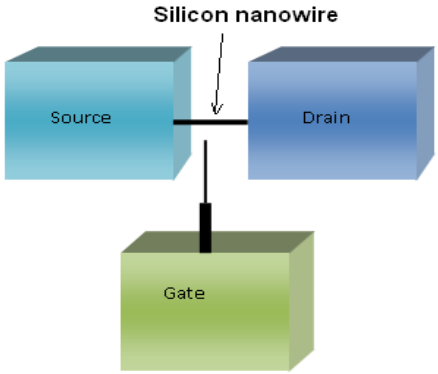
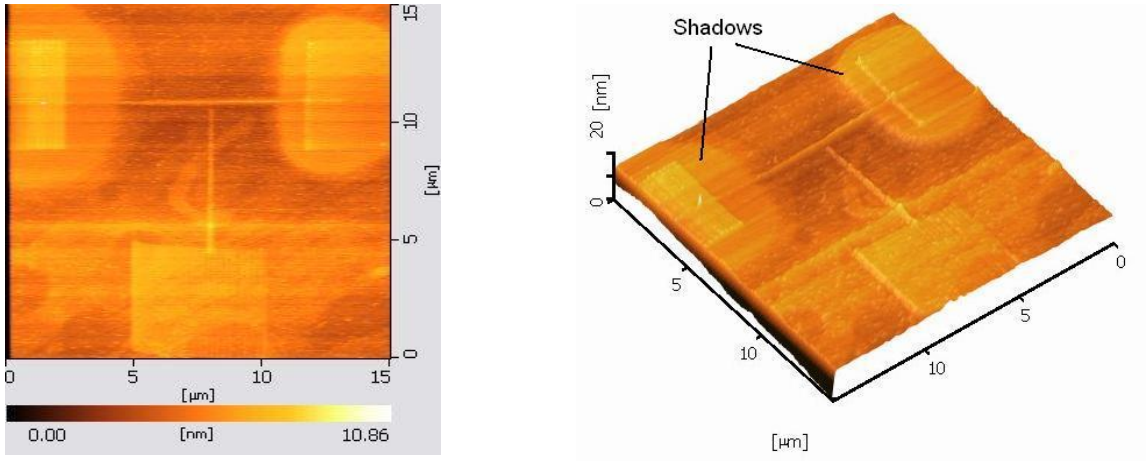


Figure 1: Schematic of silicon nanowire transistor structures patterned by AFM nanolithography.

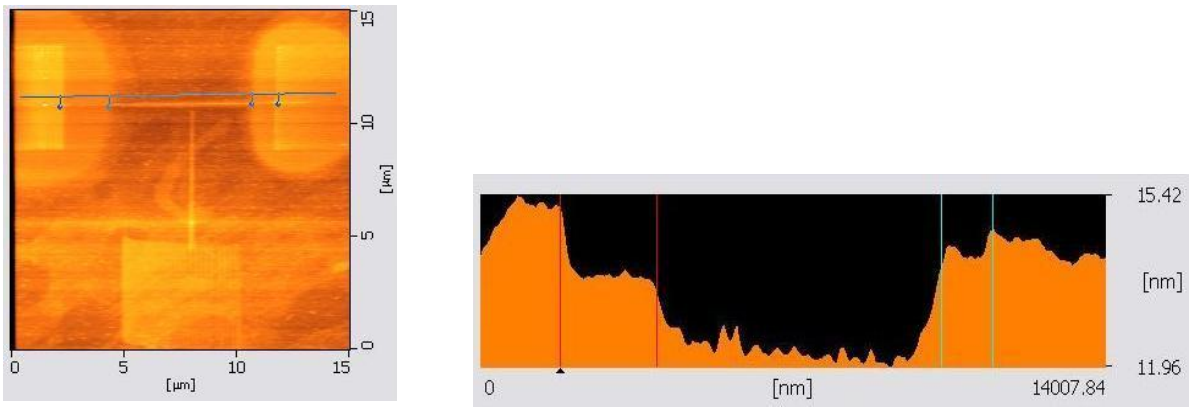
3 RESULTS AND DISCUSSION

Figures 2 and 3 show the fabricated silicon nanowire transistor (SiNWT). It was found that the fabricated device structures have some shadow even in a controlled condition. It was found that the pad not exactly formed square shapes, but have tones (shadow) surrounding the pad. In Figures 3(b) shows the line height profile for pads and shadow surrounding the structures. This problem appeared probably due to the relatively high electric field generated on AFM tip. This field is able to form ultra thin oxide layer shadows surrounding the patterns at high humidity environment inside sample chamber. From AFM topographic measurement found the size of shadow are ~0.7 nm thickness and 1.1 to 1.9 μm in width (Figure 3(b)). These shadow structures may remain on device after TMAH or KOH etching process. It is because TMAH is well known to have high selectivity to silicon dioxide with boron doped and low of anisotropic.



(a) (b)

Figure 2: (a) 2D and (b) 3D topographic images of the SiNWT structure patterned by AFM lithography before etching process



(a) (b)

Figure 3: (a) 2D topographic image with line profile of the SiNWT structure patterned by AFM lithography before etching process, (b) The line profile of patterned device has shadows of about 0.7 nm thickness and 1.1 μm in width.

Figure 4 shows the AFM topography of device after etched with TMAH. It is found that the pads size become bigger with round shape follows the shadow structures. The ultra thin oxide shadows will enough as a mask on TMAH etched device. This is because of the high selectivity and low anisotropic behaviour of TMAH etchant.

There are few reports have been discussed about silicon machining using TMAH etchant (Yang et al., 2005; van Veenendaal et al., 2001; Pennelli et al., 2006). It is known that TMAH has slow etching rate. Therefore, it gives more chances to keep the shadow as it has. Spherical depression of this orientation <100> also contributes to keep the shadow. This is because from the Monte Carlo simulation, it does simulate the orientation having step velocity, which is isotropic (Yang et al., 2005; Camon and Moktadir, 1997). When this step occurred it will effect to slow down the etch rate due to presence of step, and the direction of this step is not important to this factors (Yang et al., 2005; van Veenendaal et al., 2001; Pennelli et al., 2006; Biswas and Kal, 2006). These factors also contribute to slow down the etching process by presence of the steps and addition of boron doped, remain the shadow which occurs from design stage. The opposite way is happens to the KOH etching process. As mention by few referred journal (van Veenendaal et al., 2001; Zubel and Kramkowska, 2001; Biswas and Kal, 2006), KOH have low selectivity and high anisotropic to the silicon dioxide. In addition for boron doped, KOH will decrease the etching rate but for long etching time will over etching the structure.

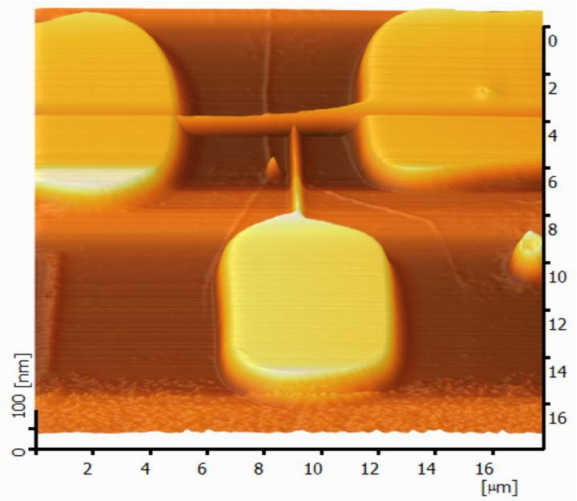


Figure 4: Topographic image of the SiNWT device etched with TMAH

Figure 5 shows the topography image of device after etched with KOH plus IPA additive. In presence of the steps by simulate of Monte Carlo simulation (van Veenendaal et al., 2001; Zubel and Kramkowska, 2001), KOH will etch fastest towards this orientation, and additive of IPA is to getting smooth surface roughness. As a result, it is found that KOH etchant able to remove all the shadow surrounding the structures patterned by AFM nanolithography. A close observation has clearly seen that the pads shape is in square shape and produce smooth surface roughness.

The electrical characterization has been performed at room temperature to the fabricated silicon nanowire transistor. Figure 6 shows the SEM micrograph of a completed silicon nanowire transistor device, labelled with source (S), drain (D) and a lateral gate (G). A completed silicon nanowire transistor obtained after removing silicon oxide mask by HF on a TMAH or KOH + IPA etched device. Figure 7(a) and 7(b) show the I-V characteristics measured in ambient air of the fabricated devices etched with TMAH and KOH + IPA, respectively.

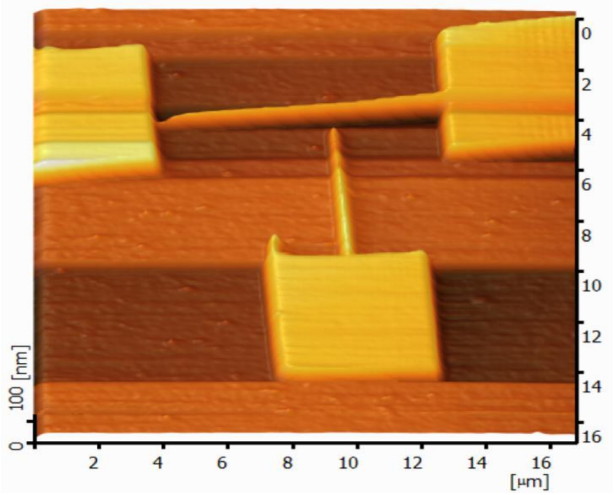


Figure 5: Topographic image of the SiNWT device etched with KOH and IPA additive

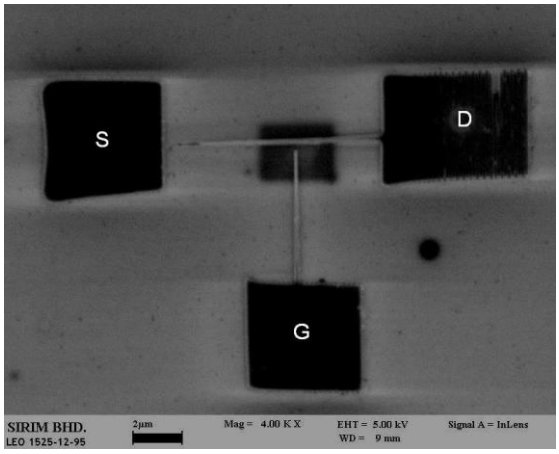


Figure 6: SEM micrograph of a completed SiNWT device after etched with hydroflouric acid (HF)

As can be observed from Figure 7(a), the p-type silicon FET has been produced may be due to passivates at anodic potential, which good agreement with those reported by Acero et al. (1995). The curves shows that the conductance decrease when the lateral gate voltage increase. This curves shows clearly the different gap between the gate voltage applied if compare to the Figure 7(b) for devices etched with KOH + IPA additive. Although the curves trend of both etchants is quite similar, the KOH etched structure found to show a small effect at different applied gate voltage. This phenomenon happens probably due to presents of K^+ ions, which is trapped in the device structure. However both of these devices show p-type semiconductor behaviour characteristics (Salem et al., 2009; Eisele et al., 1995; Martinez et al., 2008; Koo et al., 2005).

4 CONCLUSION

Silicon nanowire transistor has successfully been fabricated by AFM lithography followed by TMAH or KOH and IPA etching process. The AFM patterned device structure found to have some shadows at surrounding the pads due to a relatively high electric field generated by AFM tip. These ultra thin oxide shadows will enough acts as a mask on TMAH etched device. This is because of the high

selectivity and low anisotropic behaviour of TMAH etchant. Meanwhile, a different effect can be shows on KOH with IPA additive etched device. KOH is known as low selectivity to silicon oxide and high anisotropic. Therefore, KOH etching is able to remove shadow from surrounding of pads and whole device. From electrical characteristics found that both of the TMAH and KOH etched device structures show behaviour of p-type semiconductor. KOH with IPA additive etched device characteristics are slightly affected by applied gate voltage. This phenomenon probably may be due to the present of K^+ ions in the fabricated device structure.

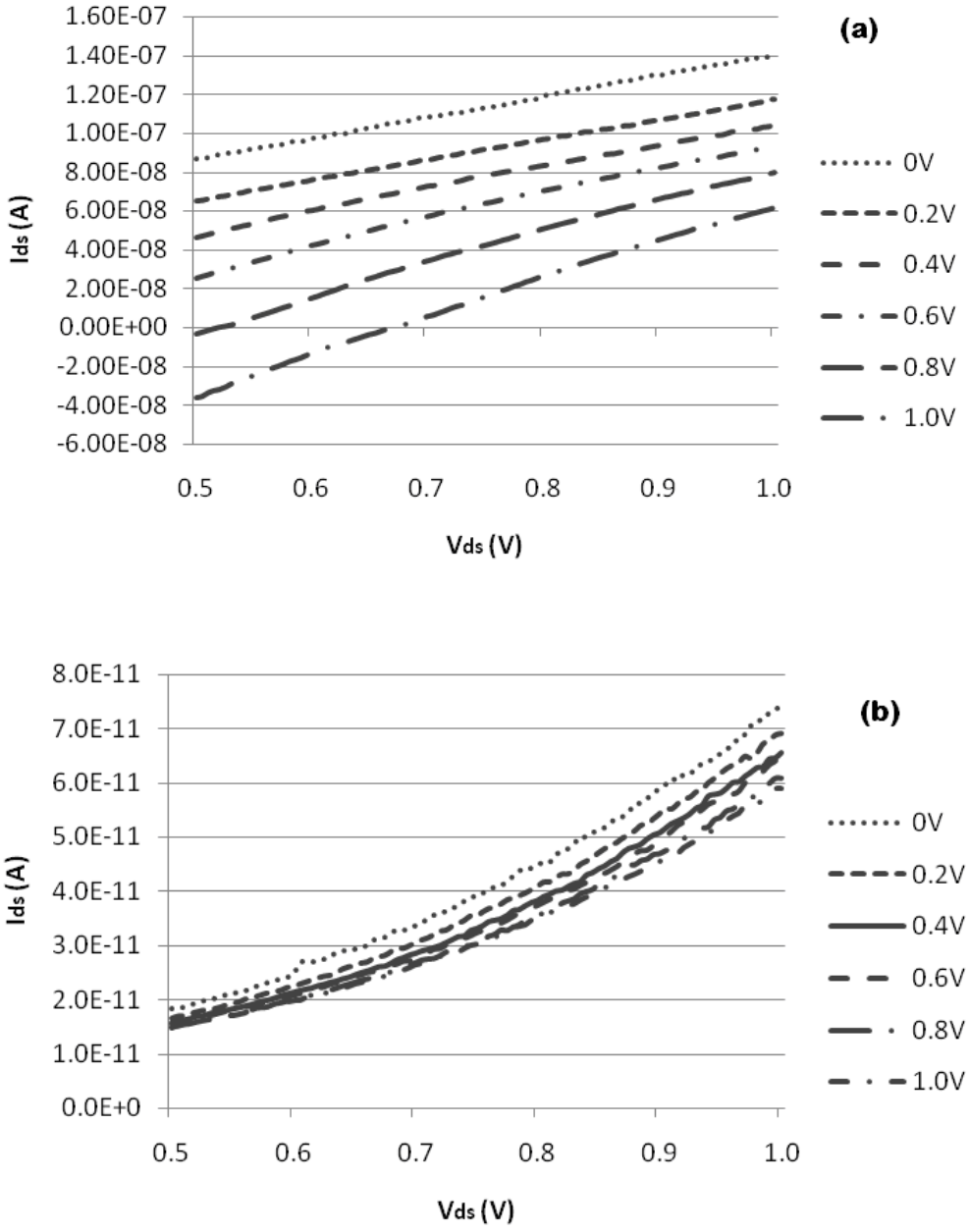


Figure 7: The current-voltage (I-V) characteristics of device (a) etched with TMAH and (b) etched with 30%wt. KOH + 10%vol. IPA. The lateral gate values were varied from 0-1.0 V

5 ACKNOWLEDGEMENTS

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REFERENCES

Acero M.C., Esteve J., Burrer Ch. and Gotz A. (1995). Electrochemical etch-stop characteristics of TMAH:IPA solutions. Sensors and Actuators A, 46-47, 22-26.

Biswas K. and Kal S. (2006). Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon. Microelectronics J., 37, 519-525.

Camon H. and Moktadir Z. (1997). Simulation of silicon etching with KOH. Microelectronics J., 28, 509-517.

Eisele I., Baumgärtner H. and Hansch W. (1995). Silicon nanostructure devices. J. Crystal Growth, 157, 248-254.

Koo S.-M., Li Q., Edelstein M.D., Ritcher C.A. and Vogel E.M. (2005). Enhance channel modulation in dual-doped silicon nanowire transistors., Nanoletters, 5, 2519-2523.

Martinez J., Martinez R.V. and Garcia R. (2008). Silicon nanowire transistors with a channel width of 4 nm fabricated by atomic force microscope nanolithography. Nanoletters, 8, 3636-3639.

Pennelli G., Piotto M. and Barillaro G. (2006). Silicon single-electron transistor fabricated by anisotropic etch and oxidation. Microelectronic Engineering, 83, 1710-1713.

Salem B., Dhalluin F., Abed H., Baron T., Entile P., Pauc N. and Ferret P. (2009). Self-connected horizontal silicon nanowire field effect transistor. Solid State Commun., 149, 799-801.

van Veenendaal E., Sato K., Shikida M. and van Suchtelen J. Micromorphology of sinle crystalline silicon surfaces during anisotropic wet etching chemical in KH and TMAH. Sensors and Actuators A, 93, 219-231.

Yang C.-R., Chen P.-Y., Yang C.-H., Chiou Y.-C. and Lee R.-T. (2005). Effects of various ion-typed surfactants on silicon anisotropic etching properties in KOH and TMAH solutions. Sensors and Actuators A, 119, 271-281.

Zubel I. and Kramkowska M. (2001). The effect of isopropyl alcohol on etching rate and oughness of (100) Si surface etched in KOH and TMAH solutions. Sensors and Actuators A, 93, 138-147.

Zubel I. and Kramkowska M. (2008). Development of etch hillocks on different Si(hkl) planes in silicon anisotropic etching. Surface Science, 602, 1712-1721.