A MONOLITHIC 622MB/S HALF RATE CLOCK AND DATA RECOVERY CIRCUIT UTILIZING A NOVEL LINEAR PHASE DETECTOR

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ABSTRACT

Clock and data recovery (CDR) circuits are crucial components in high speed transceivers. In order to ensure synchronization between data and clock in the most economic way, clock information is embedded into the transmitted data stream. The function of the CDR circuit is to determine not only the frequency at which the incoming signal needs to be sampled, but also the optimal choice of the sampling instant within each symbol interval. This paper discusses the CDR architecture, circuit design and verification of a Half-Rate Clock and Data Recovery circuit utilizing a proposed new Linear Phase Detector for serial interfaces operating at OC-12/STM-4 data rate, which is 622Mb/s. The Phase Detector gain, Kpd is 156μA and the VCO gain, Kvco is 150 MHz/V. This circuit exhibits a BER of 10^{-8} and with a power dissipation of less than 25mW. Design is based upon 0.35μm CMOS fabrication technology with 3.3V operating voltage.

1. INTRODUCTION

Clock and data recovery (CDR) circuits are key components in high speed transceivers, for example network communication systems and chip-to-chip interconnects. They implement the most critical function that is performed at the receiver of a synchronous data communication system. The role of the CDR is to recover the embedded clock information and to resynchronize it with the incoming data, enabling the serial data to be recovered.

This paper introduces a new linear Phase Detector that executes the comparison of the incoming serial data phase with that of a half-rate clock. Additionally, a new simple RS FlipFlop that is incorporated into the Phase Detector is also presented. Each component that made up the CDR circuit will be presented in this paper. Design and simulation is based upon 0.35μm CMOS fabrication.

2. ARCHITECTURE

2.1. Overview

The Clock and Data Recovery architecture consists of 5 main components - Phase Detector (PD), Charge Pump, Loop Filter, Voltage Controlled Oscillator (VCO) and Decision Circuit.

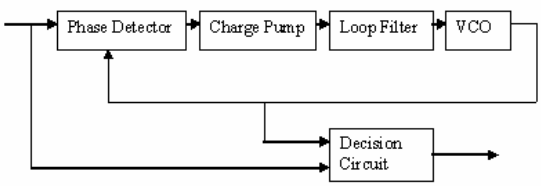

Figure 1: Clock and Data Recovery Block Diagram

2.2. Phase Detector

The Phase Detector compares the phase of the input signal and the output of the VCO. The output of the Phase Detector is a time varying signal whose DC component is proportional to the phase difference between the input signal and the output of the VCO. Hence, in the event of a phase difference between the input signal and the output of the VCO, the Phase Detector will produce a DC voltage that will change the VCO frequency in such a way that the phase difference is eliminated.

The problem with the Hogge Phase Detector [1] is that the up and down output has a strong ripple component, which causes a positive average value at the loop filter output. As a result, there is a phase offset between the data and the clock. This is in fact the motivation to the design of this new PD, shown schematically in Fig. 2. With this PD, the output of the loop filter will be zero when the clock is centered, eliminating the Hogge PD phase offset problem.

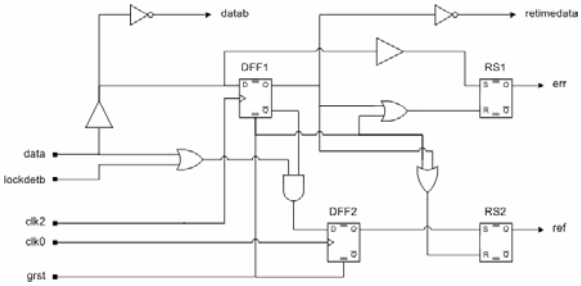

Figure 2: New Half-Rate Linear Phase Detector

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The schematic of the Double-Edge Triggered D-FlipFlop used is as in Fig. 3 and is based on the topology of Blair [2]. The two latches used in this FlipFlop are pass transistor latches with swing restoration buffer in order to avoid performance degradation in the output inverter

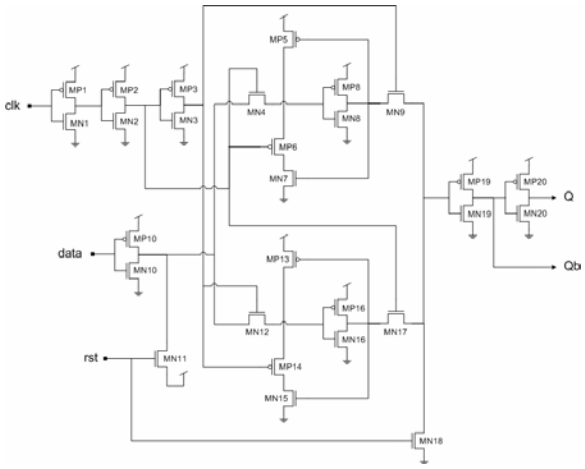

Figure 3: Schematic of Double-Edge Triggered D-FlipFlop

The use of the Double-Edge Triggered D-FlipFlop effectively reduces the clock rate to be only half of the data rate. As a result, in this CDR architecture, only a clock rate of 322MHz is required for the input data rate of 622MB/s.

The RS FlipFlop implemented in this CDR circuit is basically a simple circuit that uses only 7 gates, as shown schematically in Fig. 4.

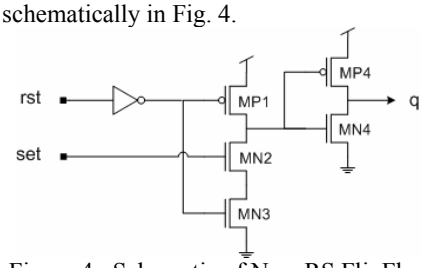

Figure 4 : Schematic of New RS FlipFlop

Table 1 : Truth table of the RS FlipFlop

set	rst	Q
0	0	Hold
0	1	0
1	0	1
1	1	0

This simple design eliminates the condition of unpredictable results at the output when both set and rst input is at logic 1 by clearing the output. This suits the PD application here as it ensures that the *err* and *ref* output to always have a finite pulse width.

2.3. Voltage Controlled Oscillator

The Clock and Data Recovery Circuit requires that the oscillator used is tunable, that is the output frequency of the oscillator as a function of the input control voltage. The result of this is that the clock can be shifted distinctively to always clock in the received bits stream in the middle of the logic pulses.

The Voltage Control Oscillator (VCO) presented here is based upon the topology of Rau et al.[3]. Essentially, the VCO frequency is a linear property of the control voltage.[2] The oscillator control voltage in the s domain is given by,

$$V_c(s) = i_d(s)Z(s) = \frac{I_p Z(s)\theta_e(s)}{2\pi} = K_{pd} Z \theta_e \,. \qquad (1)$$

The top row of PMOS and the bottom row of NMOS in between the inverters act as the current sources. These current sources limit the amount of current available to the inverters. Consequently, the inverters are starved of current. And now, the oscillation frequency of an N-stage ring equals to (2NTD)-1, where TD denotes the large signal delay of each stage [4]. Thus, current starving the inverters is effectively raising the time constant at the output and lowering the oscillation frequency.

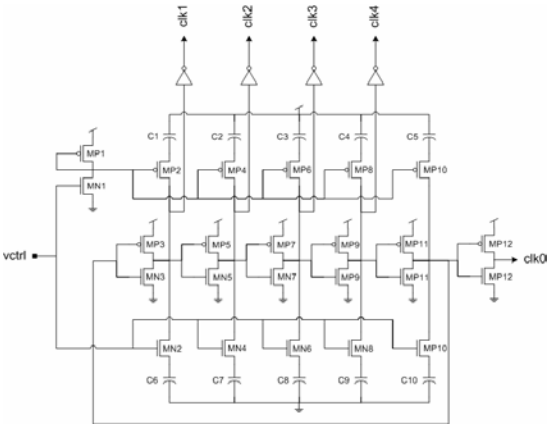

Figure 5 : VCO Schematic

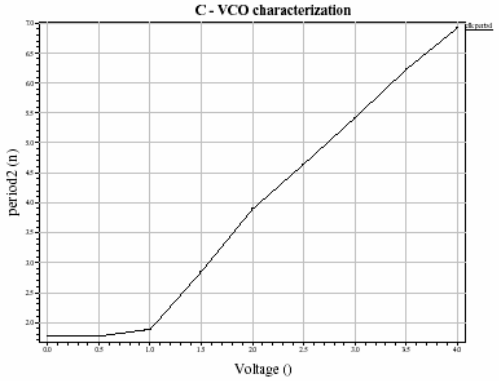

Figure 6 : VCO Characterization

From the waveform, the period of the VCO increases linearly with the control voltage. In other words, the clock frequency reduces linearly as the control voltage increases.

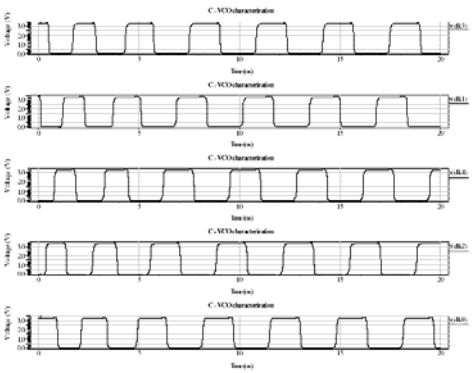

Figure 7: Phase shift of each VCO output clock

Fig. 7 illustrates the phase shift for each output clock from the VCO, which is clk0 to clk4. The VCO employed is a ring oscillator with 5 stages. Thus, the phase shift between each adjacent clock is 72^{o}. This phase shift is a very interesting and useful property of ring oscillators, and can be used to decide whether the received data is being clocked right in the center of the pulse.

2.4. Charge Pump

A charge pump accompanies the phase detector. The phase detector compares the feedback from Voltage Controlled Oscillator (VCO) and the reference signal to generate an error signal which is proportional to the magnitude of the phase difference between them. This error signal is fed to the charge pump. The output of the charge pump feeds the VCO which ultimately controls the clock frequency shift to recover the received data.

The combined transfer function or gain of the Phase Detector and Charge Pump is given by,

$$K_{pd} = \frac{I_p}{2\pi} \frac{A}{rad} \qquad (2)$$

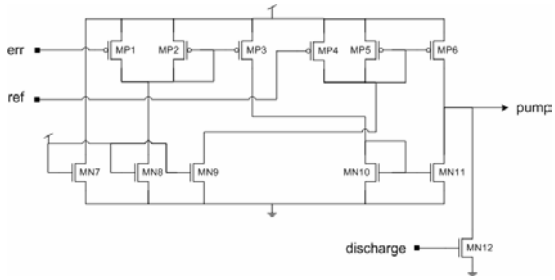

Figure 8 : Charge Pump Schematic

The charge pump is based upon the topology of Wu et al.[5]. The function of the charge pump is to transfer the *Err* and *Ref* signals into the VCO control voltage. When *Ref* is high, there will be a net current flowing to the pump output. And when *Err* is high, there will be a net current flowing out of the charge pump. The charge pump current controls the magnitude of charge stored in the loop filter, thus converting the Phase Detector output to a control voltage recognizable by the VCO.

2.5. Loop Filter

The output of the Phase Detector consists of a dc component and a superimposed ac component. The function of the loop filter is to convert the output of the charge pump to the VCO control voltage and to filter out the high frequency ac component. The loop filter is a complex impedance in parallel with the input capacitance of the VCO [6].

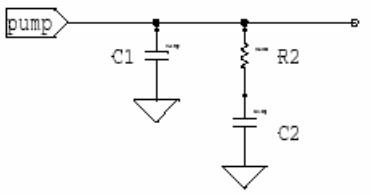

Figure 9: Loop Filter Schematic

Passive low pass filter is employed as it does not require any power supply, hence reducing power consumption and the design is simpler compared to an active filter. The drawback is the large amount of silicon space required for the fabrication of passive components.

3. SIMULATION RESULTS

A continuous stream of 101010 is first used to drive the Data input of the Clock and Data Recovery Circuit to the lock state. It is only after the signal lockdet is asserted, that normal 8b10b encoded data for transmission is allowed to be received to begin the recovery process. 8b10b encoding [7] ensures a run length of no greater than 5 ones or zeroes before getting a transition. Fig. 10 depicts the locking process. Lock time from simulation is approximately 350ns. A margin of 100ns is used to ascertain proper lock before the lockdet signal is asserted.

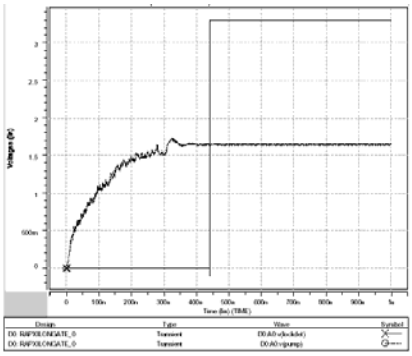

Figure 10 : Waveform displaying the locking process

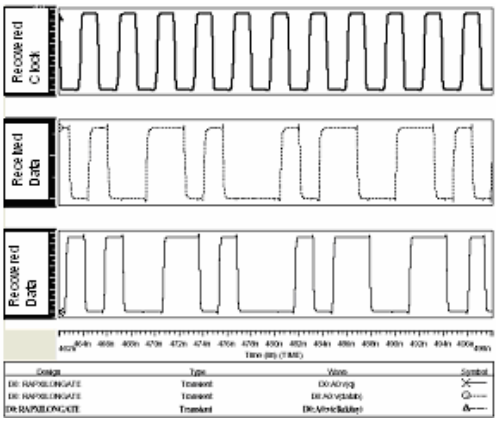

Figure 11 : Waveform of the recovered Data and clock.

The signal clkdelay is Clk2, which is the recovered clock and is from the VCO as described earlier. The signal datab is the inverse of the serial data stream going into the Clock and Data Recovery Circuit. The signal q is the recovered data. Data is recovered at both the positive edge and negative edge of the clock. By using both edges to clock the data, a VCO frequency of 311MHz is needed compared to 622MHz if only a single edge is used.

4. CONCLUSION

A complete Clock and Data Recovery Circuit had been successfully designed, simulated and the layout completed, all utilizing TSMC 0.35µm CMOS fabrication technology with 3.3V operating voltage. This 622MB/s Clock and Data Recovery Circuit exhibits a BER of 10^{-8} and with a power dissipation of less than 25mW.

Additionally, a new Phase Detector architecture is proposed. During the circuit design process, a new RS FlipFlop had also been designed and incorporated into the Clock and Data Recovery Circuit.

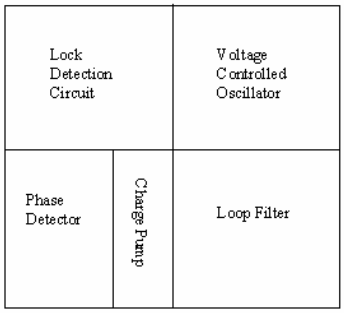

Figure 12 : Floor Plan of the Clock and Data Recovery Circuit

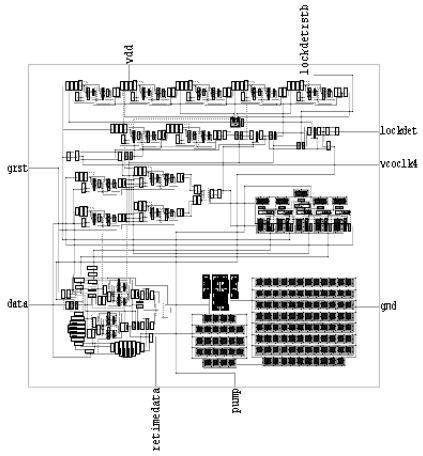

Figure 13 : Layout of the Clock and Data Recovery.

5. REFERENCES

[1] Hogge, C.R., "A Self Correcting Clock Recovery Circuit", *Journal of Lightwave Technology*, Volume LT-3 No 6, 1985.

[2] Blair, G.M., "Low-power Double-edge Triggered FlipFlop", *Electronics Letter*, Vol. 33 No. 10, May 1997.

[3] Rau, M., Oberst, T., Lares, R., Rothermel, A., Schweer, R., Menoux, N., "Clock/Data Recovery PLL Using Half-Frequency Clock", *Journal of Solid State Circuits*, Volume 32, Issue 7, July 1997.

[4] Razavi, Behzad, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, 2001.

[5] Wu, L., Chen, H., Nagavarapu, S., Geiger, R., Lee, E., Black, W., "A Monolithic 1.25GB/s CMOS Clock/Data Recovery Circuit for Fibre Channel Transceiver", *IEEE International Symposium on Circuits and Systems*, Volume 2, June 1999.

[6] Keese, William O., "An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase Locked Loops", *National Semiconductor Application Note* 1001, May 1996.

[7] Widmer, A.X., Franaszek, P.A., "A DC-Balanced, Partitioned-Block, 8b/10b Transmission Code", International Business Machines Corporation, 1983.