# Design of Tunable CMOS Up-Conversion Mixer for RF Integrated Circuit

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**ABSTRACT**

*A high Frequency 1-3GHz tunable pure NMOS Up-conversion mixer topology is presented. The mixer is implemented in a 0.25μm CMOS process technology. Tunable range of frequency had been achieved by utilizing an off-chip tunable inductor. The mixer is implemented by configuring a balanced-modulator topology. High linearity is achieved by utilizing various passive components for biasing and operation purposes. A low voltage topology is achieved by reducing the amount of stacked transistors.*

## 1. INTRODUCTION

Wireless transmitter and receiver can be conceptually separated into baseband and radio-frequency sections. The RF section of the transmitter is responsible for converting the processed baseband signal up to the assigned channel and injecting the signal into the medium [1]. Commonly implemented silicon bipolar technology is expensive and not suited for integration of digital functions. Since the majority of CMOS RF front-end circuits are designed using similar circuit topologies as their bipolar counterpart, it is not surprising that they require higher power dissipation [2].

An Up-conversion mixer is utilized at the transmitter of a transceiver. The purpose of an Up-conversion mixer is to convert the input baseband signal to a high frequency component for reliable transmission. The evolution of mobile communication system promotes the design of low voltage topology in RF circuits [2]. This requirement increases the lifetime per weight of the battery used. The miniaturization of CMOS transistors follows the primary objective of increasing circuit speed and density.

In this paper the design of an Up-conversion mixers in a standard CMOS technology is discussed. Section II reviews the design of a low voltage four quadrant multiplier [3], which is the mixing core of the circuit. In Section III, the design of a high frequency low amplitude error, phase shifter [4] and the design of a cascode amplifier [5] are discussed. The on-chip connection between cascode amplifier and the mixer provides better linearity and saves power consumption. Based on these topologies, a high speed NMOS linear Up-conversion mixer is implemented in Section IV. Section V discusses the simulation results for the high frequency tunable Up-conversion mixer in a 0.25μm standard CMOS technology.

## 2. LOW VOLTAGE MULTIPLIER DESIGN

To reduce the power consumption of mobile communication system, low-voltage topology is best to be used in the design of RF integrated circuits. Today, low voltage topology is implemented by utilizing tuned LC tanks in the circuits [2]. This technique introduces bulky tuned passive component in the circuit. In this paper low voltage topology is introduced by reducing the amount of stacked transistors, hence reducing the dc supply voltage ($V_{dd}>V_T$) for each pair of transistors [3]. This technique also enables the circuit to be scaled down to deep submicron technology. Therefore a low voltage topology, with the turn on voltage consumption $V_T \cong 0.72V$, had been realized in 0.25μm CMOS process technology.

A parallel structure of CMOS four-quadrant multiplier [3] is used as the core of the mixer topology. The circuit realization is shown in Fig. 1, where the output is sensed by proper matching each of the differential transistor stages [1]. The corresponding output voltage $v_{out}$ is given by:

$$v_{out} = 4v_1v_2B\left[\left(2AV_1 + A'\right)\left(4AV_1 + A'\right)\right] = K'v_1v_2 \quad (1)$$

where $B=-R_sK$, $A=-R_LK$ and $A'=2R_LKV_T$, where $K$ is the transconductance parameter of the transistor used, hence the multiplication function had been realized. From (1), $v_1=v_L$ which is the input carrier signal, obtained from external voltage controlled oscillator ($VCO$) , $v_2=v_{BB}$ which is the input baseband signal.

## 3. PHASE SHIFTER AND CASCODE AMPLIFIER DESIGN

### 3.1. Phase shifter

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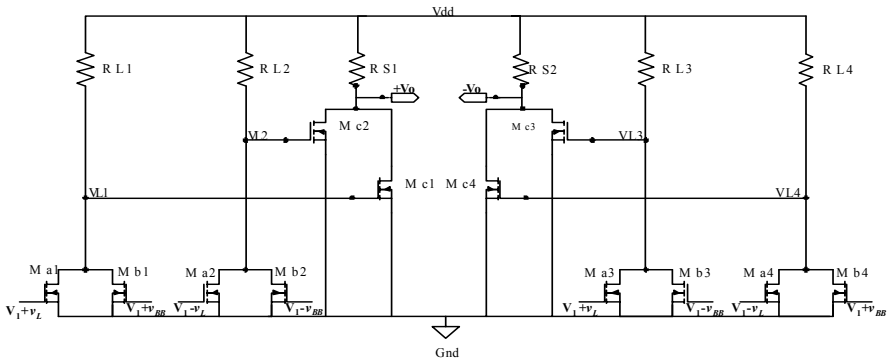



Fig. 1. Low Voltage Four Quadrant Analog Multiplier [3].

The proposed high gain ***90***° phase shifter [4] is shown in Fig. 2. The circuit consists of an off-chip tunable inductor (Lp3 and Lp4), to tune the amplitude of the phase shifted output waveform so that the subsequent stages are not saturated. The input is sensed through a degenerated resistor (Rs3 and Rs4) to increase the linearity of the circuit [6]. The circuit has a tolerable 0.1% phase error and dc blocking capacitors [4] are not required as the dc potentials of the output are $V_{pp}$, where $V_{pp}$ sets the constant dc level of the output voltage swing of the circuitry. $V_{pp}$ also provides input dc bias to the subsequent output stages, $V_{pp}<V_{dd}$.

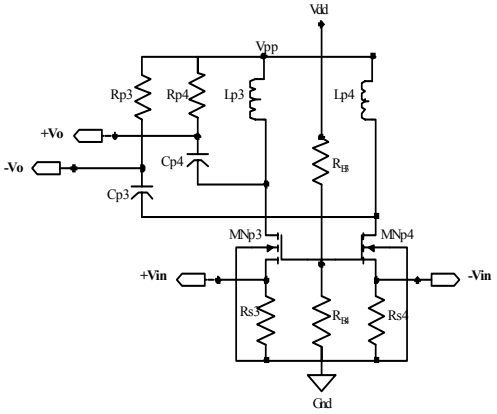



Fig. 2. High Frequency Phase Shifting Network.

### 3.2. Cascode amplifier design

Fig. 3 shows a simplified schematic of a cascode amplifier [5]. The common gate transistor M2, provides high isolation between input and output terminals and avoids Miller amplification of the gate-drain capacitance of M1. The integration of a high frequency cascode amplifier increases the sensitivity of the output waveform. In Fig. 3 transistor M2 boosts the output impedance of M1 by a factor of $(g_{m2}+g_{mb2})r_{o2}$. The voltage gain at the output is increased due to an increase of the output resistance is given by (2).

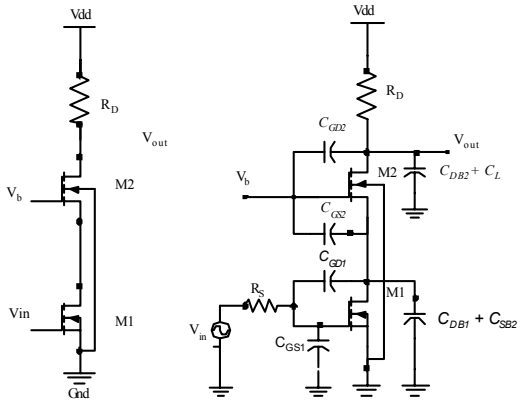



Fig. 3. (a) Cascode Amplifier, (b) High Frequency Model of a Cascode Amplifier.

### 4. LINEAR NMOS UP-CONVERSION MIXER

Fig. 4 shows the schematic diagram of the designed Up-conversion mixer circuit excluding the phase shifting network. The output from the Up-conversion mixer is sensed differentially to suppress even order distortion [1]. The multiplied input voltages are coupled through a capacitor to the input of the cascode amplifier to avoid dc coupling.

Each differential stage transistor represents the combiner, is matched geometrically to avoid distortion due to transistor mismatch. Passive biasing resistors are utilized to increase the linearity [4] of the circuit. The gain of the Up-converter network is given by (3), where $A_1$ and $A_2$ are the amplitude of the carrier and baseband signal respectively and $C=C_{F1}=C_{F2}=C_{F3}=C_{F4}$, which is the coupling capacitance of Fig. 4.

$$A(s)=\frac{A_1A_2K'(g_{m2}+g_{mb2})r_{o2}g_{m1}r_{o1}}{sC\left\{1+sR_S\left[C_{GS1}+\left(1+\frac{g_{m1}}{g_{m2}+g_{mb2}}\right)C_{GD1}\right]\left[1+sR_D(C_{DB2}+C_L+C_{GD2}\right]\right\}} \quad (3)$$

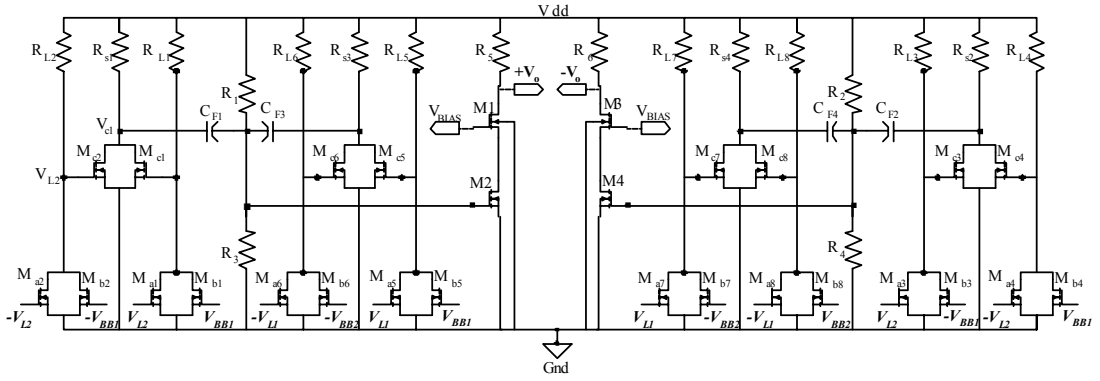
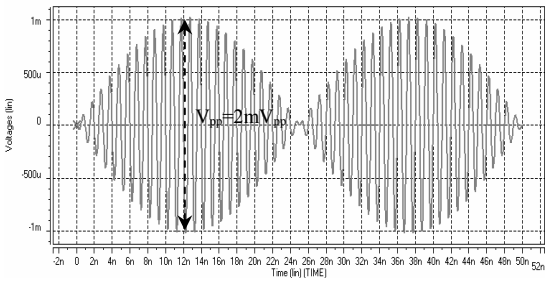


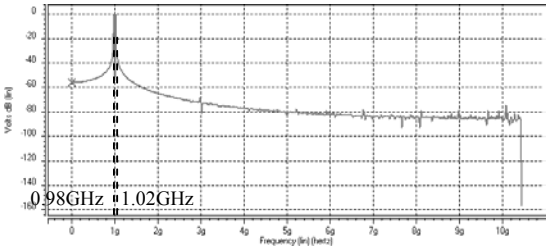

Fig. 4. The Up-conversion Mixer topology, excluding the High Gain Phase Shifter Topology.

## 5. ANALYSIS OF SIMULATION RESULTS

The analysis of the designed Up-conversion mixer was performed with 1-3 GHz of carrier (Local Oscillator) frequency and 20-100MHz of baseband frequency.




(a)




(b)

Fig. 5. (a) Double sideband suppressed carrier waveform at 20MHz baseband signal and 1GHz of carrier signal, (b) Corresponding Fourier Transform.

Fig. 5(a) shows the corresponding output of the low voltage four quadrant analog multiplier at 20MHz of baseband frequency and 1 GHz of local oscillator frequency. Fig. 5(b) shows that the Fourier transform coefficient peaks at lower sideband and upper sideband frequency, which are at 0.98GHz and 1.02GHz, respectively. This topology is simulated with supply voltage as low as 1.2Vdc and dissipates 28.85mW of power. The output voltage swing is $2mV_{pp}$. It could be observed from Fig. 5(b) that the output spurious signal has tolerable peaks, hence resulting in a linear mode of operation.

From Fig. 6, it could be concluded that the proposed high gain phase shifting network has good amplitude accuracy, hence relaxing the requirement of cascading limiting amplifiers at subsequent stages. The phase error of this topology is almost negligible, which is approximately 0.1% [4].

Fig. 7 displays the gain response and the input-output noise analyses of the designed cascode amplifier. It could be observed that the –3dB gain of the cascode amplifier is 8.9dB with corresponding bandwidth of 4.8GHz. The amount of power dissipation is 2.648mW, at 2Vdc of supply voltage. Fig. 8 displays the output

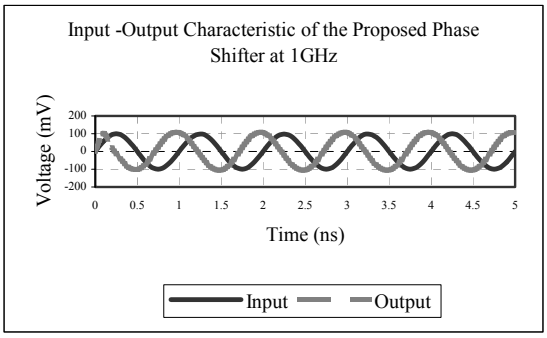



Fig. 6. Input-Output response of the designed Phase Shifting network.

characteristic of the designed Up-conversion mixer at 40MHz baseband frequency and 1GHz of carrier frequency. This topology was realized at 2Vdc of supply voltage and dissipates 150mW of power. The output noise is $7.25\times10^{-16}$ V/$\sqrt{Hz}$ .

To describe the tunable characteristic of the designed mixer, Fig. 9 shows the Fourier transform coefficient peaks of the mixer at different baseband and carrier frequency. Fig. 10 describes the response of 4 different cases, i.e. at 100MHz of baseband frequency and 1GHz of carrier frequency, 500MHz of baseband frequency and 1GHz of carrier frequency, 100MHz of baseband frequency and 2GHz of carrier frequency, and 100MHz of baseband frequency and 3GHz of carrier frequency.

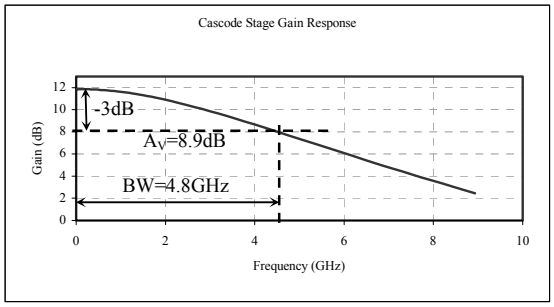



Fig. 7. Gain response of the cascode amplifier.

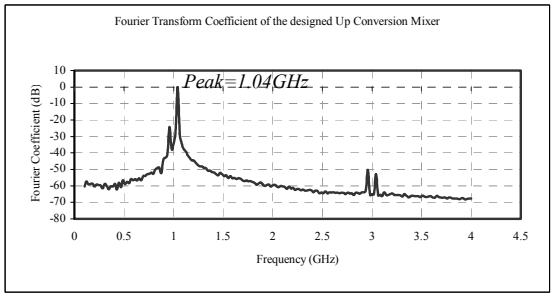



Fig. 8. Fourier transform coefficient of the output.

Conversion loss is a measure of efficiency of the mixer. Fig. 10 shows the plot of conversion loss versus the changes of baseband and carrier signal level of the mixer. It is clear from Fig. 10 that the operation of the mixer is highly linear.

Table I lists the measured performance of the designed up-conversion mixer topology.

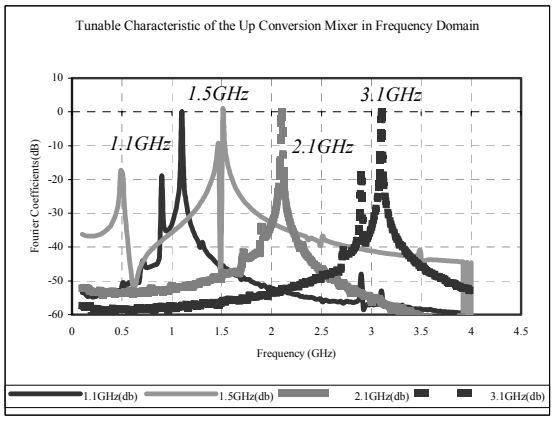



Fig. 9. Fourier Transform coefficient responses with: (a) Baseband 100MHz, Carrier 1GHz, (b) Baseband 500MHz, Carrier 1GHz, (c) Baseband 100MHz, Carrier 2GHz, (d) Baseband 100MHz, Carrier 3GHz.

## 6. CONCLUSION

An Up-conversion mixer with tunable range of frequency is designed using phasing method. A phase shifter with negligible phase error and a high frequency cascode amplifier had been designed.

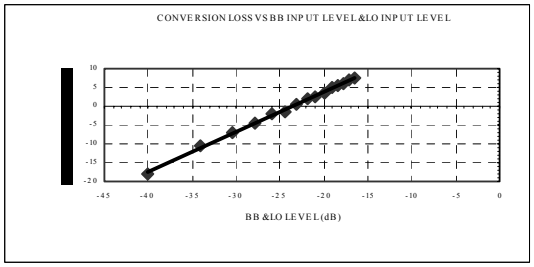



Fig. 10. Conversion Loss versus the changes of Input Baseband and Carrier signal Level.

TABLE I
MEASURED PERFORMANCE

| Performance Parameter | Mixer Output |
|---|---|
| Voltage supply | 2.0Vdc |
| Power Dissipation | 150mW |
| Baseband frequency | 40MHz |
| Carrier frequency | 1GHz |
| Carrier Power | -50dBm |
| Lower Sideband suppression | -24.2dB |
| Carrier feedthrough | -33.2dB |
| Input $IIP_3$ | 0dBm |
| 1dB compression level | 4.6dB |

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