UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 2008/2009

November 2008

EBB 526/3 - Electronic Packaging

Duration : 3 hours

Please ensure that this examination paper contains SIX printed pages before you begin the examination.

This paper contains SIX questions.

Instructions: Answer **FIVE** questions. If a candidate answers more than five questions only the first five questions in the answer sheet will be graded.

Answer to any question must start on a new page.

All questions must be answered in English.

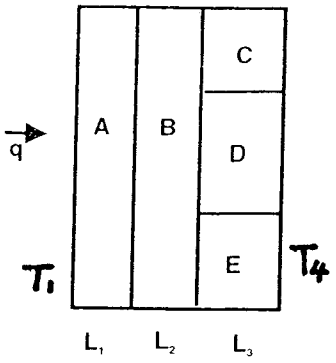

Figure 1

1. [a] Referring to the Figure 1, let L_1, L_2, L_3 be 0.153 m, 0.244 m and 0.305 m. It is assumed the total heat transfer rate q, is 29.3 W. Other assumptions are listed in the table below. Determine the temperature difference between T_1 and T_4.

Thermal conductivity, W/m-K	86.52	138.42	173.03	173.03	173.03
Cross-sectional area, m^2	0.093	0.093	0.028	0.037	0.028

(50 marks)

[b] State the various types of thermal interface materials (TIM). Write briefly on one of them.

(50 marks)

2. [a] Briefly explain the driving force of device scaling down.

(40 marks)

[b] Sketch and label a cross sectional view of a flip chip electronic package.

(20 marks)

[c] Explain the functions of an electronic package.

(40 marks)

3. [a] A typical formulation of an underfill is shown in Table 1. Describe the function of each of the ingredients. What are the effects to the underfill if catalyst and curing agent are removed from the formulation? How to remove bubbles in the underfill if defoamer is not used?

Table 1 - Typical formulation of an underfill

Materials	%
Resin (Epoxy)	30
Filler (SiO_2)	60
Catalyst	2
Curing agent (amine)	5
Toughening agent	1
Defoamer	2

(40 marks)

[b] What is coefficient of thermal expansion (CTE), glass transition temperature (T_g) and gel time? Why are they important in selecting an underfill material?

(40 marks)

[c] What are the functions of thermal interface material (TIM)? Give five (5) examples of good TIM properties.

(20 marks)

4. [a] Define 'Quality' and 'Reliability', explain how they are different and provide an example of each.

(40 marks)

[b] Explain all possible areas of how to guarantee enough reliability of a product while maintaining the cost competitiveness of that product.

(20 marks)

[c] Define the 'Extrinsic' and 'Intrinsic' defect of a silicon packaging technology. Provide an example of each.

(40 marks)

5. [a] Discuss about the following:

(i) Brittle fracture phenomenon at solder joint.

(ii) The four ingredients in flux and how does flux react to perform its function.

(iii) Typical reflow profile and factors to be concerned of during reflow.

(iv) Surface tension in soldering.

(60 marks)

[b] The electronic packaging industries are now moving towards lead-free and halogen free materials. Discuss how these affect the choice of solder alloys, flux and the surface finish in interconnect technology.

(40 marks)

6. [a] Every single substrate material shipped out by the substrate manufacturer is electrically tested for any opens or shorts within the substrate. However, during the open/short test done after the substrate material is fully assembled (with die, underfill etc), a high resistance readout was detected. Upon further investigation and failure analysis, the following defect was observed in one of the via within the substrate (refer to Figure 2)

(i) Explain why the defect was not detected by supplier. Why the defect only detected after the substrate is fully assembled with die etc. Provide assumptions made in your answers.

(30 marks)

(ii) What type of screening test could the substrate manufacturer carried out to detect such defect, in addition to the regular open/short test?

(20 marks)

(iii) Explain what are the potential process abnormality at supplier that could lead to the incomplete plating at the via bottom. Use your imaginations.

(20 marks)

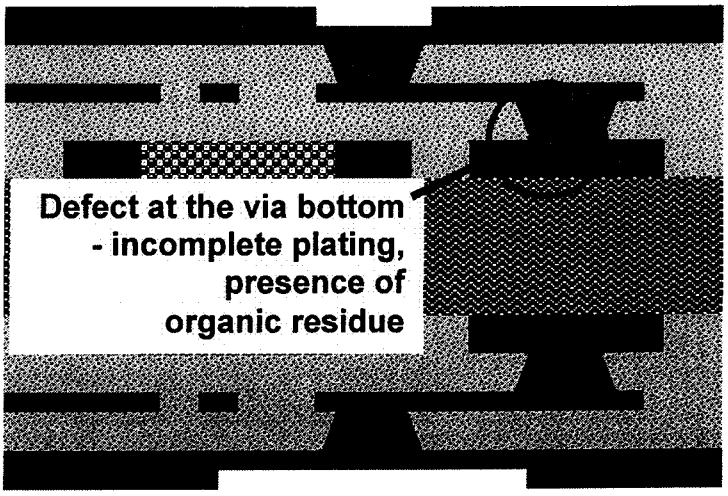

Figure 2

[b] Explain the function of Phosphorus content in the ENIG surface finish plating.

(30 marks)

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