UNIVERSITI SAINS MALAYSIA

Peperiksaan Kursus Semasa Cuti Panjang
Sidang Akademik 2007/2008

Jun 2008

EEE 241 – ELEKTRONIK ANALOG I

Masa: 3 jam

Sila pastikan bahawa kertas peperiksaan ini mengandungi TUJUH muka surat dan DUA muka surat LAMPIRAN yang bercetak sebelum anda memulakan peperiksaan ini.

Kertas soalan ini mengandungi ENAM soalan.

Jawab LIMA soalan.

Mulakan jawapan anda untuk setiap soalan pada muka surat yang baru.

Agihan markah bagi setiap soalan diberikan di sudut sebelah kanan soalan berkenaan.

Jawab semua soalan dalam bahasa Malaysia atau bahasa Inggeris atau kombinasi kedua-duanya.

1. (a) Satu transistor pnp mempunyai lebar tapak efektif $10\,\mu m$ dan $I_C = 0.5$ mA. Jika kapasitan susutan pemancar-tapak adalah 2 pF dalam kawasan pincang ke depan dan adalah tetap, kira frekuensi peralihan peranti tersebut. Diberikan $\tau_F = \frac{W_B^2}{2D_p}$. Abaikan kapasitan pengumpul-tapak. Koefisien resapan bagi pembawa minoriti dalam tapak ialah $13\ cm^2/s$ dan voltan setara suhu atau voltan terma ialah 26 mV.

A pnp transistor has an effective base width of $10\,\mu m$ *and* $I_C = 0.5$ mA. *If the emitter-base depletion capacitance is 2 pF in the forward-bias region and is constant, calculate the device transition frequency. Given* $\tau_F = \frac{W_B^2}{2D_p}$. *Neglect the collector-base capacitance. Diffusion coefficient of minority carrier in the base is* $13\ cm^2/s$ *and temperature equivalent voltage or thermal voltage is 26 mV.*

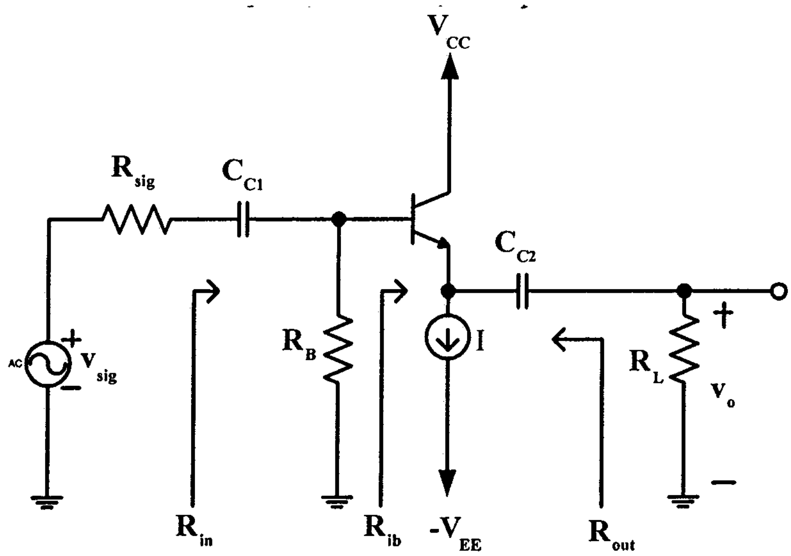
(b) Lukis litar setara isyarat kecil satu BJT dengan mengabaikan rintangan pengumpul-tapak, r_μ, dan rintangan siri pemancar, r_{ex}. Tunjukkan bahawa gandaan arus ac ialah $B(j\omega) = \frac{g_m}{j\omega(C_\pi + C_\mu)}$ dan frekuensi gandaan uniti adalah $f_T = \frac{1}{2\pi} \frac{g_m}{C_\pi + C_\mu}$.

Draw the small signal equivalent circuit of a BJT by ignoring the collector-base resistance, r_μ, *and emitter lead series resistance,* r_{ex}. *Show that the ac current gain is* $B(j\omega) = \frac{g_m}{j\omega(C_\pi + C_\mu)}$ *and the unity gain frequency is* $f_T = \frac{1}{2\pi} \frac{g_m}{C_\pi + C_\mu}$.

(20 marks)

2. Pengikut pemancar dalam Rajah 1 digunakan untuk menyambungkan satu sumber ac yang mempunyai $R_{sig} = 10k\Omega$ kepada satu beban $R_L = 1k\Omega$. Transistor dipincang pada I = 5mA, menggunakan perintang $R_B = 40k\Omega$, dan mempunyai $\beta_F = \beta_o = 100$, $V_A = 100V$ dan V_{th} = 26 mV. Tentukan $R_{ib}, R_{in}, A_v = \frac{v_o}{v_{sig}}$ dan R_{out}. Anggap bahawa kapasitor gandingan C_{C1} dan C_{C2} adalah litar pintas pada frekuensi operasi. Anggap r_o adalah finit dan harus dipertimbangkan semasa membuat pengiraan. Lukis dan gunakan litar setara isyarat kecil hibrid-π semasa menentukan nilai-nilai ini.

The emitter follower in Figure 1 is to connect an ac source with $R_{sig} = 10k\Omega$ to a load $R_L = 1k\Omega$. The transistor is biased at I = 5mA, utilizes a resistance $R_B = 40k\Omega$, and has $\beta_F = \beta_o = 100$, $V_A = 100V$ and V_{th} = 26 mV. Find $R_{ib}, R_{in}, A_v = \frac{v_o}{v_{sig}}$ and R_{out}. Assume that the coupling capacitors C_{C1} and C_{C2} are shorted at the frequency of operation. Assume r_o is finite and should be taken into consideration in the calculation. Draw and use the hybrid-π small-signal equivalent circuit in determining these values.



Rajah 1
Figure 1

(20 marks)

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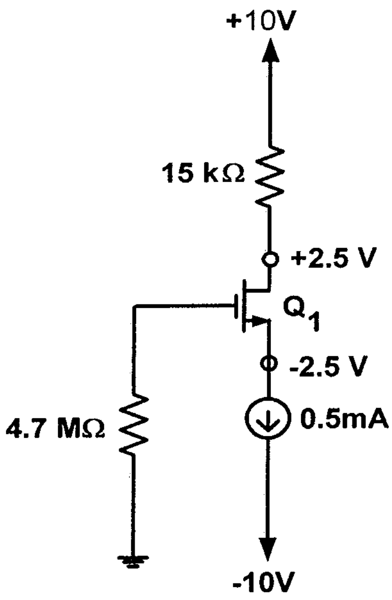
3. Pertimbangkan litar dalam Rajah 2. Kirakan V_{OV} , V_{GS} , V_G , V_S , dan V_D jika litar adalah dalam keadaan berikut: $V_A = 75\ V$, $V_{th} = 1.5\ V$ dan $k'(W/L) = 1\ mA/V^2$. Kirakan juga g_m dan r_o .

Consider the circuit in Figure 2. Calculate V_{OV} , V_{GS} , V_G , V_S , and V_D *if the circuit is under the following conditions:* $V_A = 75\ V$, $V_{th} = 1.5\ V$ *and* $k'(W/L) = 1\ mA/V^2$. *Calculate also* g_m *and* r_o .

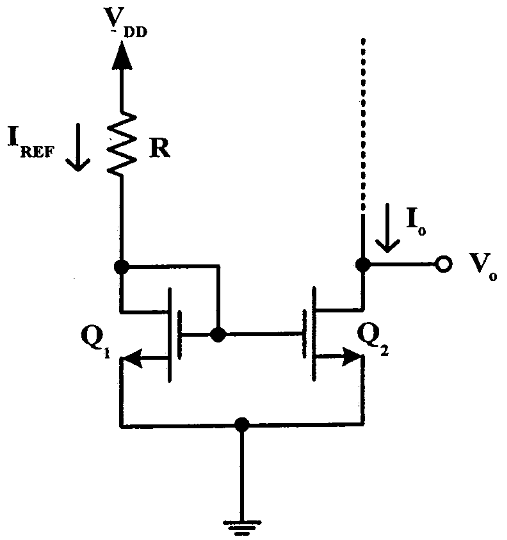


Rajah 2
Figure 2

(20 marks)

4. Diberikan $V_{DD} = 3V$ dan $I_{REF} = 100\mu A$, anda dikehendaki merekabentuk satu litar seperti dalam Rajah 3 bagi mendapatkan arus keluaran $100\mu A$. Kirakan R jika Q_1 dan Q_2 adalah sepadan dan mempunyai panjang saluran $1\mu m$, lebar saluran $10\mu m$, $V_{th} = 0.7V$ dan $k' = 200\mu A / V^2$ di mana $k' = \frac{\mu_n C_{ox}}{2}$. Apakah nilai terendah yang boleh bagi V_o? Menganggap bahawa bagi teknologi proses ini voltan Early ialah $V_A = 20V$, kirakan rintangan keluaran sumber arus ini. Tentukan juga perubahan pada arus keluaran jika berlaku perubahan sebanyak +1V pada V_o.

Given $V_{DD} = 3V$ and using $I_{REF} = 100\mu A$, it is required to design the circuit of Figure 3 to obtain an output current whose nominal value is $100\mu A$. Find R if Q_1 and Q_2 are matched and have channel lengths of $1\mu m$, channel widths of $10\mu m$, $V_{th} = 0.7V$ and $k' = 200\mu A / V^2$ where $k' = \frac{\mu_n C_{ox}}{2}$. What is the lowest possible value of V_o? Assuming that for this process technology the Early voltage $V_A = 20V$, find the output resistance of the current source. Also, find the change in output current resulting from a +1V change in V_o.



Rajah 3
Figure 3

(20 marks)

5. Pertimbangkan litar dalam Rajah 4 bagi kes $V_{CC} = V_{EE} = 10\ V, I = 1\ mA, R_B = 100\ k\Omega, R_C = 8\ k\Omega, \beta_{dc} = 100$ dan $V_{BE} = 0.7\ V$.

Consider the circuit of Figure 4 for the case $V_{CC} = V_{EE} = 10\ V, I = 1\ mA, R_B = 100\ k\Omega, R_C = 8\ k\Omega, \beta_{dc} = 100$ *and* $V_{BE} = 0.7\ V$.

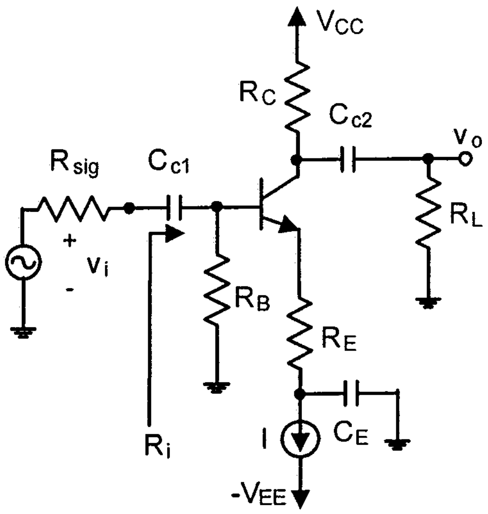
(a) Lakukan analisa isyarat besar dan tentukan semua arus dc (iaitu I_C, I_B dan I_E) dan voltan di setiap terminal transistor (iaitu V_C, V_B dan V_E).

Do large signal analysis and find all dc currents (i.e. I_C, I_B and I_E*) and voltage at each transistor terminal (i.e.* V_C, V_B and V_E).

(b) Lakukan analisa isyarat kecil dan tentukan nilai R_E yang menyebabkan R_{in} bersamaan 4 kali rintangan R_{sig}. $R_{sig} = 5\ k\Omega, R_L = 5\ k\Omega, \beta_o = 100$ dan $V_{th} = 26\ mV$.

Do small signal analysis and find the value of R_E *that results in* R_i *equals to 4 times the source resistance* R_{sig}. $R_{sig} = 5\ k\Omega, R_L = 5\ k\Omega, \beta_o = 100$ *and* $V_{th} = 26\ mV$.

(20 marks)

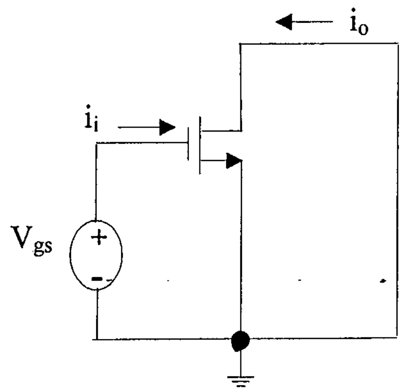


Rajah 4
Figure 4

6. Diberikan satu transistor MOS seperti yang ditunjukkan dalam Rajah 5. Lukis model isyarat kecil bagi transistor tersebut. Anggap $V_{sb} = V_{ds} = 0$, g_{mb}, r_o, C_{sb} dan C_{db} boleh diabaikan. Buktikan bahawa

Given a MOS transistor as shown in Figure 5. Draw the small signal model of the transistor. Assume $V_{sb} = V_{ds} = 0$, g_{mb}, r_o, C_{sb} and C_{db} are ignored. Prove that

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}}$$



Rajah 5
Figure 5

Bandingkan ungkapan di atas dengan ungkapan frekuensi gandaan uniti bagi BJT.

Compare the above expression with the unity gain frequency expression for the BJT.

(20 marks)

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APPENDIX

A.1.1 SUMMARY OF ACTIVE-DEVICE PARAMETERS

(a) *npn* Bipolar Transistor Parameters

Quantity	Formula
Large-Signal Forward-Active Operation	
Collector current	$I_c = I_S \exp \dfrac{V_{be}}{V_T}$
Small-Signal Forward-Active Operation	
Transconductance	$g_m = \dfrac{qI_C}{kT} = \dfrac{I_C}{V_T}$
Transconductance-to-current ratio	$\dfrac{g_m}{I_C} = \dfrac{1}{V_T}$
Input resistance	$r_\pi = \dfrac{\beta_0}{g_m}$
Output resistance	$r_o = \dfrac{V_A}{I_C} = \dfrac{1}{\eta g_m}$
Collector-base resistance	$r_\mu = \beta_0 r_o$ to $5\beta_0 r_o$
Base-charging capacitance	$C_{b'} = \tau_F g_m$
Base-emitter capacitance	$C_\pi = C_b + C_{je}$
Emitter-base junction depletion capacitance	$C_{je} \simeq 2C_{je0}$
Collector-base junction capacitance	$C_\mu = \dfrac{C_{\mu 0}}{\left(1 - \dfrac{V_{BC}}{\psi_{0c}}\right)^{n_c}}$

Quantity	Formula
Small-Signal Forward-Active Operation	
Collector-substrate junction capacitance	$C_{cs} = \dfrac{C_{cs0}}{\left(1 - \dfrac{V_{SC}}{\psi_{0s}}\right)^{n_s}}$
Transition frequency	$f_T = \dfrac{1}{2\pi} \dfrac{g_m}{C_\pi + C_\mu}$
Effective transit time	$\tau_T = \dfrac{1}{2\pi f_T} = \tau_F + \dfrac{C_{je}}{g_m} + \dfrac{C_\mu}{g_m}$
Maximum gain	$g_m r_o = \dfrac{V_A}{V_T} = \dfrac{1}{\eta}$

(b) *NMOS* Transistor Parameters

Quantity	Formula
Large-Signal Operation	
Drain current (active region)	$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{gs} - V_t)^2$
Drain current (triode region)	$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}[2(V_{gs} - V_t)V_{ds} - V_{ds}^2]$
Threshold voltage	$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}\right]$
Threshold voltage parameter	$\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon N_A}$
Oxide capacitance	$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 3.45\ \text{fF}/\mu\text{m}^2$ for $t_{ox} = 100$ Å
Small-Signal Operation (Active Region)	
Top-gate transconductance	$g_m = \mu C_{ox}\frac{W}{L}(V_{GS} - V_t) = \sqrt{2I_D\mu C_{ox}\frac{W}{L}}$
Transconductance-to-current ratio	$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_t}$
Body-effect transconductance	$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}g_m = \chi g_m$
Channel-length modulation parameter	$\lambda = \frac{1}{V_A} = \frac{1}{L_{eff}}\frac{dX_d}{dV_{DS}}$
Output resistance	$r_o = \frac{1}{\lambda I_D} = \frac{L_{eff}}{I_D}\left(\frac{dX_d}{dV_{DS}}\right)^{-1}$
Effective channel length	$L_{eff} = L_{drwn} - 2L_d - X_d$
Maximum gain	$g_m r_o = \frac{1}{\lambda}\frac{2}{V_{GS} - V_t} = \frac{2V_A}{V_{GS} - V_t}$
Source-body depletion capacitance	$C_{sb} = \frac{C_{sb0}}{\left(1 + \frac{V_{SB}}{\psi_0}\right)^{0.5}}$

Quantity	Formula
Small-Signal Operation (Active Region)	
Drain-body depletion capacitance	$C_{db} = \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\psi_0}\right)^{0.5}}$
Gate-source capacitance	$C_{gs} = \frac{2}{3}WLC_{ox}$
Transition frequency	$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})}$