TERJEMAHAN

UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2000/2001 Academic Session

April/May 2001

ZCT 106/3 - Electronic

Time : 3 hours

Please check that the examination paper consists of **TWELVE** printed pages before you commence this examination.

Answer all FOUR questions. Candidates may choose to answer all questions in the Malay Language. If candidates choose to answer in the English Language, it is compulsory to answer at least one question in the Malay Language.

1. (a) In Fig. 1.1 find the voltage V and the current I as indicated. The diodes drop 0.7V when conducting.

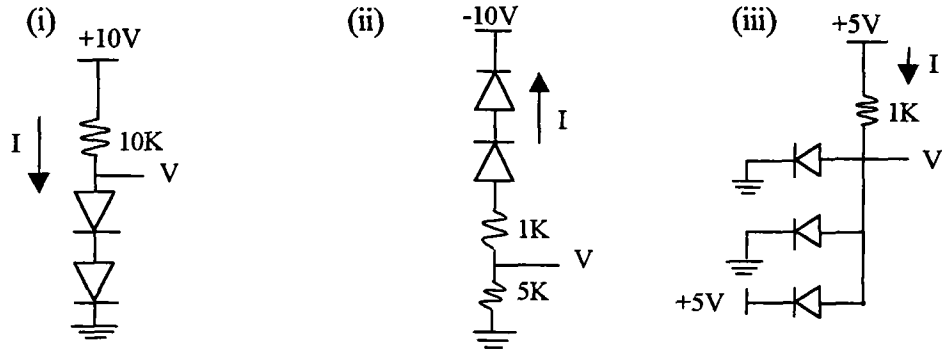

Fig. 1.1

(30/100)

... 8/-

(b) Find exactly the DC values of I_B, I_C, I_E and V_C for Fig. 1.2.

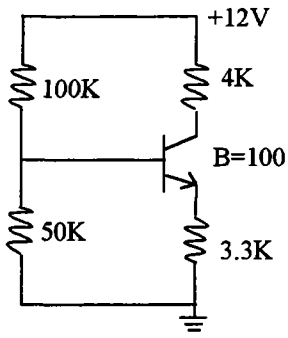

Fig. 1.2

(40/100)

(c) Find V_o/V_i for the transistor model circuit shown in Fig. 1.3.

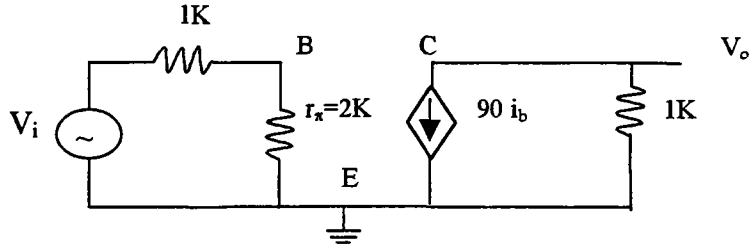

Fig. 1.3

(30/100)

2. For the circuits shown in Fig. 2.1 determine I_B, I_C and V_{CE}.

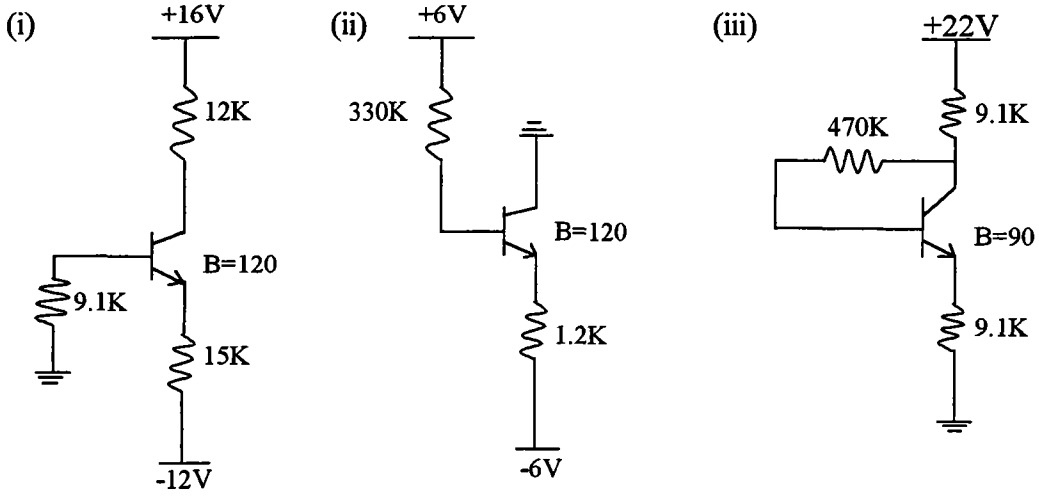

Fig. 2.1

(60/100)

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(b) For the transistor circuit model shown in Fig. 2.2:

(i) Derive an expression for the amplifier voltage gain V_o/V_i as a function of frequency. From this find expressions for the DC gain and the 3-dB frequency

(ii) Calculate the DC gain and the -3-dB for R_s = 20KΩ, r_π = 100K, C_i = 6pF, g_m = 144 mA/V and R_L = 1K.

(iii) Calculate the frequency at which the gain become 0dB.

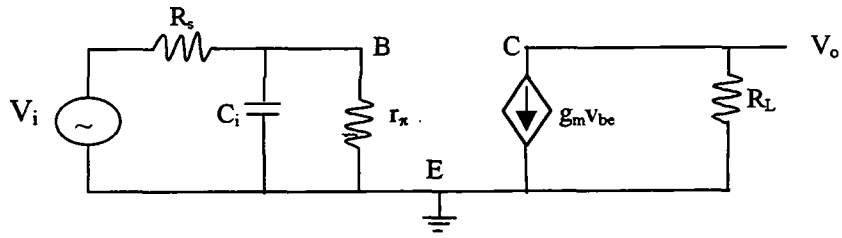

Fig. 2.2

(40/100)

3. (a) (i) Calculate the output voltage for an input of V_i = 1V, for the circuit in Fig. 3.1.

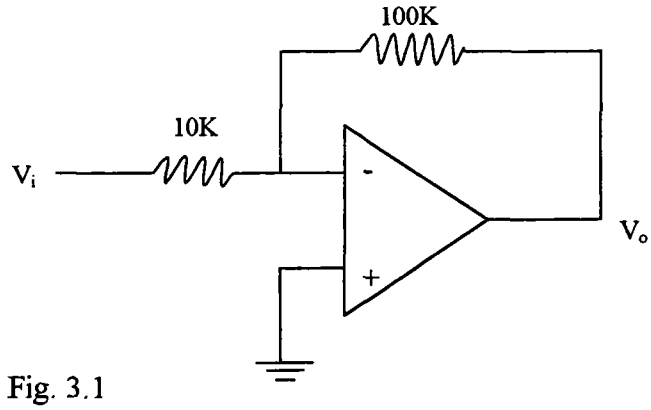

Fig. 3.1

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(ii) Calculate the output voltage for an input of V_i = 10mV for the circuit in Fig. 3.2

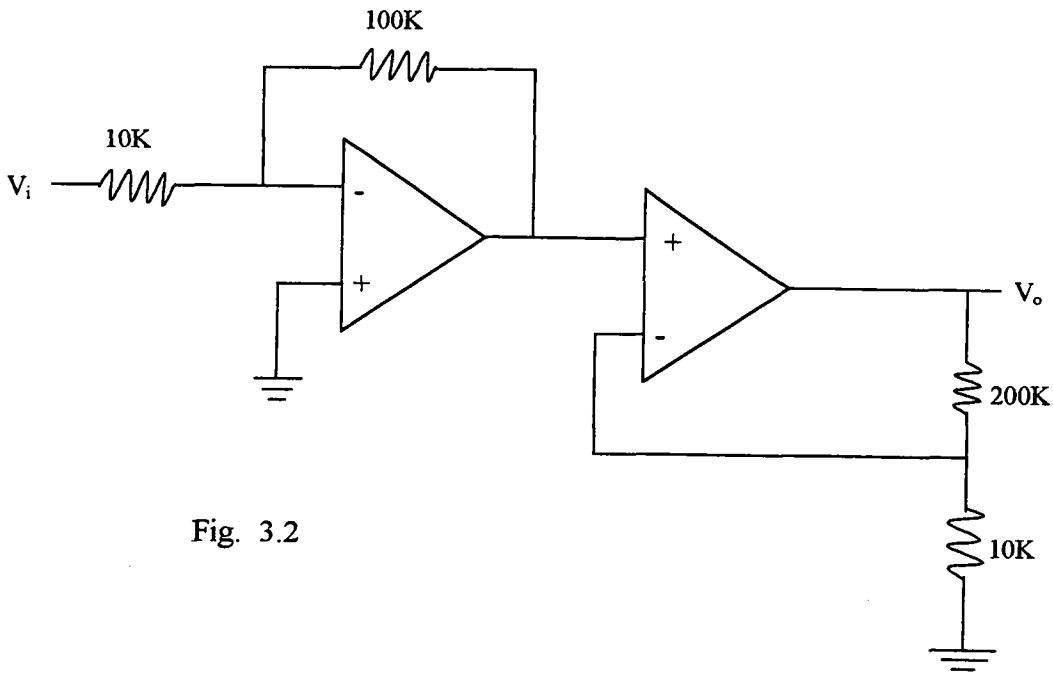

Fig. 3.2

(iii) Calculate the output voltage for the cirucit in Fig. 3.3

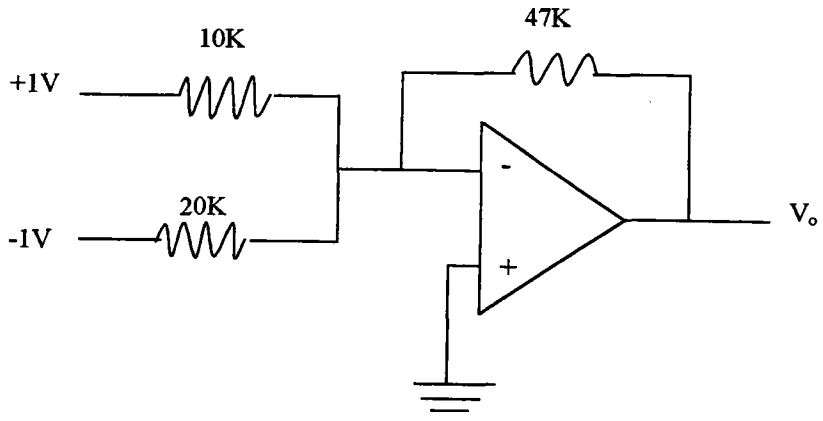

Fig. 3.3

(60/100)

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(b) (i) In Fig. 3.4 specify suitable components to achieve a cut off frequency of 1 kHz, with a DC gain of 20dB and input resistance of at least 10K.

(ii) At what frequency does the gain drop to unity.

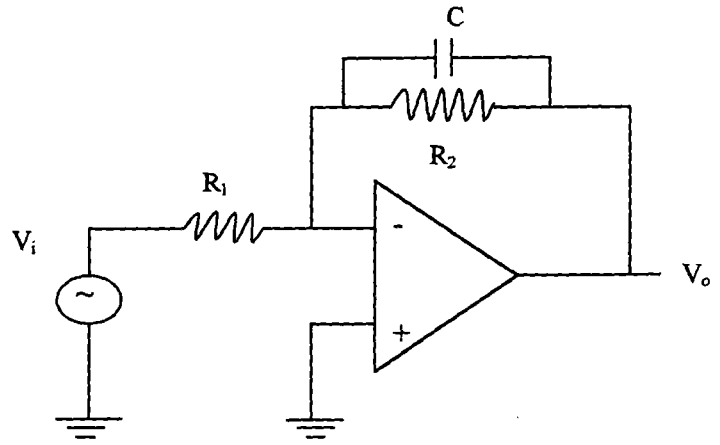

Fig. 3.4

(40/100)

4. (a) Determine the regulated voltage and circuit currents for the shunt regulator, as in Fig. 4.1.

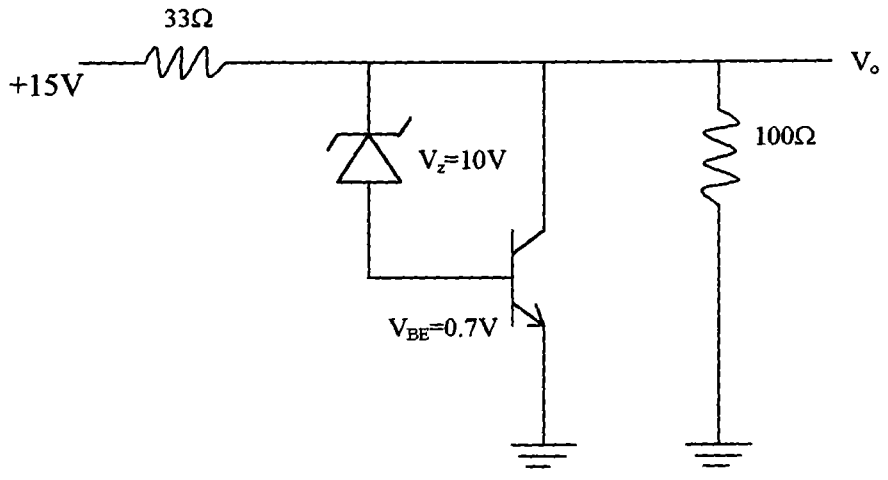

Fig. 4.1

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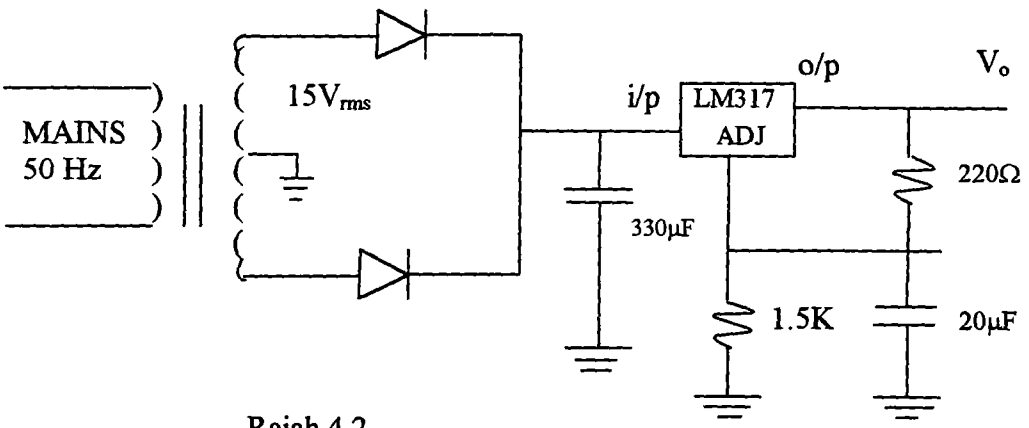
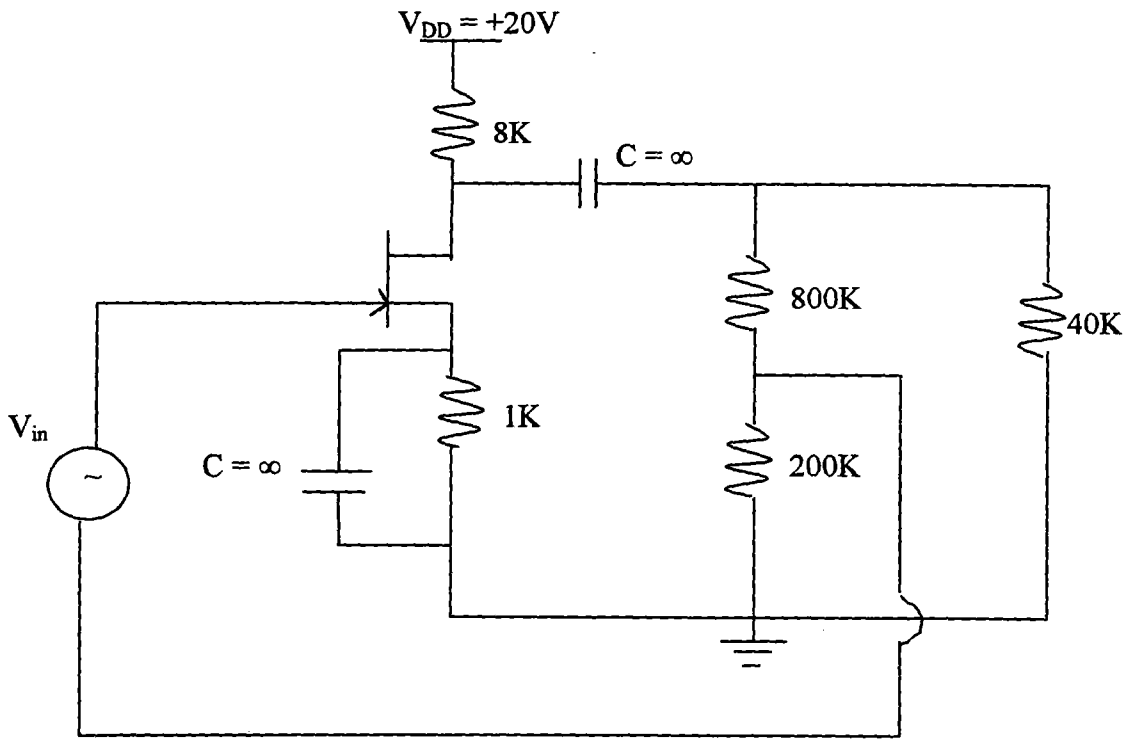
(b) Determine the regulated output voltage from the circuit of Fig. 4.2 if $V_{REF} = 1.25V$.



Rajah 4.2

(30/100)

(c) Calculate the gain with and without feedback for an N-channel JFET as shown in Fig. 4.3 if $g_m = 5000$ µs.



(40/100)

Rajah 4.3

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