Mo-P-65

Effect of Nitric-Oxide Post-Oxidation Annealing on High-Temperature Oxidized 4H SiC

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Metal-Oxide-Semiconductor FETs using 4H-SiC have been investigated intensively because 4H-SiC semiconductor has excellent physical properties for power-device applications.[1,2,3] However, ideal on-resistance of the MOSFETs has not been realized due to very low channel mobility. One of the origins of the low channel mobility is because of high interface-trap density (D_{it}) closer to conduction-band edge. The prevailing factor contributing to the high D_{it} is the existence of intrinsic carbon that originated from two sources: (1) residual carbon from surface of substrate prior to oxidation and (2) carbon generated at the interface during oxidation.[4,5] In this paper, we have investigated MOS characteristics of thermally nitrided SiO_2 on 4H SiC at high oxidation temperature ($\geq$1300 ^{o}C). A comparison has also being made between the nitrided and dry oxides.

N-type 4H-SiC wafers with 5-μm thick epilayer doped with $(0.9\sim1.5)\times10^{16}$ cm^{-3} of nitrogen and chemically cleaned with a modified RCA method with a final dip in dilute HF solution ($HF:H_2O=1:9$) were used in this work. The wafers were inserted into a tube furnace and then oxidized in a dry oxygen environment at 1300 and 1400 ^{o}C. The oxidation time was controlled to obtain a 65~70-nm thick oxide. After the oxidation, one set of sample was underwent post-oxidation annealing (POA) in nitric acid (NO) ambient (1175 ^{o}C), while other sample did not go through the annealing process. After cooling down, top of the samples were deposited with a layer of aluminium using a thermal evaporator. The areas of the MOS capacitors were then defined by photolithography. Finally, after removing the back oxide, a large area aluminum back contact was deposited on the N^{+} substrate. A computer-controlled Keithely 590 CV analyzer/595 Quasistatic C-V meter was employed at room temperature to measure capacitance-voltage (C-V). The D_{it} was estimated by simultaneous high-low C-V method. Dry oxide grown at 1300^{o}C is having a lower D_{it} than the oxide grown at 1400℃ (Fig. 1). A reverse situation has been recorded in NO POA sample, whereby a higher growth temperature demonstrates a lower D_{it} value but it is still higher than its none-annealed

counterpart. The results of the normalized capacitance-voltage (C-V) curves in Fig. 2 indicate that the interface properties were deteriorated during high temperature oxidation (1400℃) and this property is further deteriorated after NO POA. In the full manuscript, these observations will be explained in detail.

References

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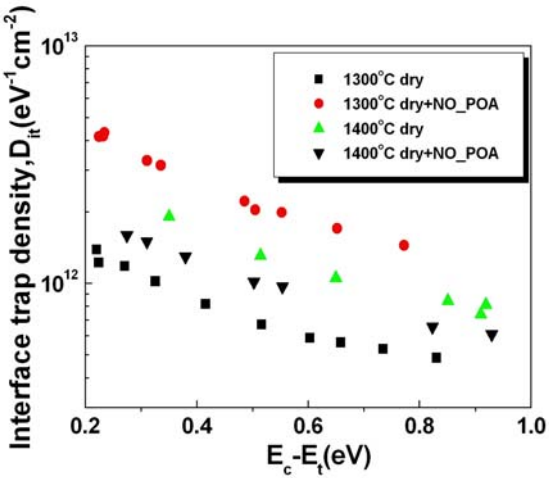
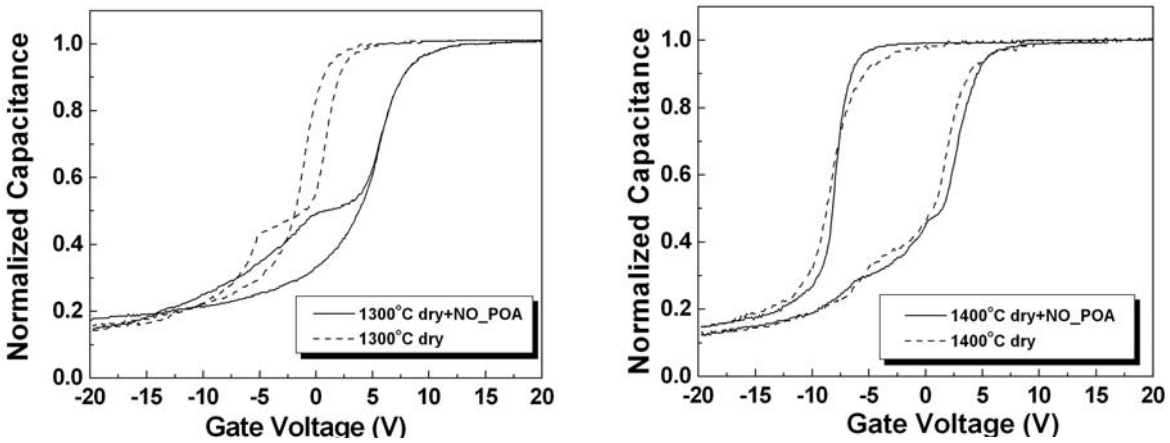


Fig. 1. Energy profiles of D_{it} for samples oxidized in dry oxygen at 1300, 1400℃ and NO POA



(a) (b)

Fig. 2. Normalized capacitance-voltage (C-V) characteristics of MOS capacitors oxidized (a) at 1300℃, (b) 1400℃ and NO POA