UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama

Sidang 1987/88

EEE 206 Litar Elektronik I

Tarikh: 31 Oktober 1987 Masa: 9.00 pagi - 12.00 tengahari

(3 Jam)

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi 8 muka surat berserta 6 Lampiran yang bercetak sebelum anda memulakan peperiksaan ini.

Jawab TIGA (3) soalan daripada Bahagian 'A'
dan DUA (2) soalan daripada Bahagian 'B'.

Jawab kesemua soalan di dalam Bahasa Malaysia.

...2/-

Bahagian A

1. (i) Apakah kebaikan tarik ke atas aktif dan tarik ke bawah aktif di dalam suatu get NAND TTL?

(50%)

(ii) Dengan menggunakan data di Jadual 1, tentukan yang berikut:-

a) Berapakah bilangan get Schottky TTL yang dapat didorong oleh satu get TTL kuasa-rendah ?

b) Berapakah bilangan get TTL kuasa-rendah yang dapat didorong oleh satu get Schottky TTL?

(50%)

Parameter	TTL Kuasa Rendah	Schottky TTL
V_{OL} max	0.4 V	0.4 V
V_{OH} min	2.4 V	2.4 V
V_{IL} max	0.8 V	0.8 V
V_{IH} min	2.0 V	2.0 V
I_{IL} max	0.18 mA	2 mA
I_{IH} max	10µA	50µA
I_{OL} max	3.6 mA	20 mA
I_{OH} max	200 µA	1 mA

Jadual 1

...3/-

2. (i) Apakah keperluan get-get TTL pengumpul terbuka?

(30%)

(ii) Merujuk kepada kertas data, kirakan bilangan 74107 yang dapat didorong pada masukan jam oleh satu output tunggal daripada 7437.

(50%)

(iii) Apakah kebaikan yang penting bagi ECL apabila dibandingkan dengan TTL?

(20%)

3. (i) Bandingkan keluarga logik TTL dan CMOS.

(30%)

(ii) Manakah keadaan-keadaan operasi yang berikut yang mungkin akan menghasilkan purata terendah P_D untuk suatu sistem logik CMOS? Terangkan.

a) V_{DD} = 12v , frekuensi pensuisan f_{max} = 2 MHz

b) V_{DD} = 12v , f_{max} = 100 kHz

c) V_{DD} = 5v , f_{max} = 100 kHz

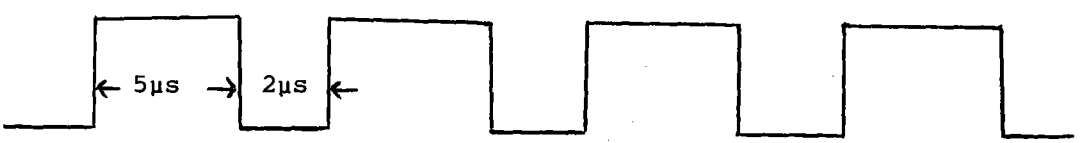
(20%)

...4/-

(iii) Adalah diperlukan untuk mendorong sepuluh (10) get-get NAND 74 H 20 oleh satu keluaran CMOS. Get CMOS dipincang oleh suatu bekalan kuasa 12v dan mempunyai $I_{OH\ max} = -360\mu A$ dan $I_{OL\ max} = 360\mu A$. Dengan menggunakan kertas data 74 H 20 , rekabentuk suatu litar perantaramukaan.

(50%)

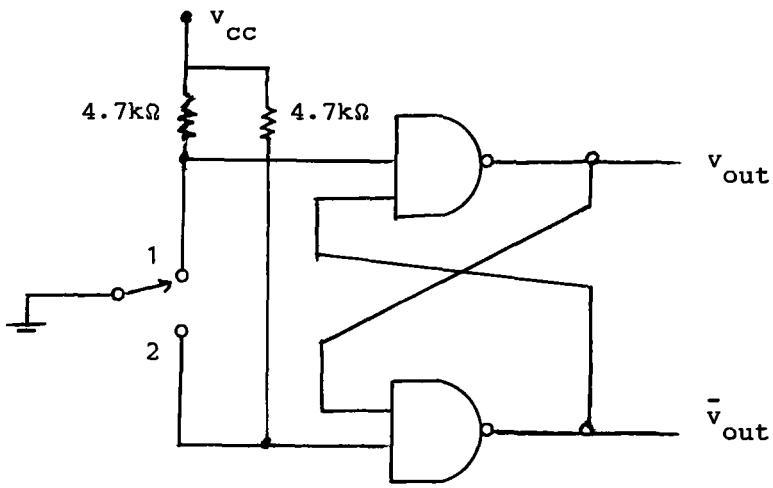
4. (i) Rekabentuk suatu litar dengan satu 74121 dan satu NE555 untuk menghasilkan bentuk gelombang seperti berikut:-



(40%)

...5/-

(ii) Kenalpastikan litar di dalam Rajah (1) dan terangkan operasinya.



(30%)

Rajah (1)

(iii) Bagaimanakah kitar tugas merupakan suatu pembatasan ke atas frekuensi picu?

(30%)

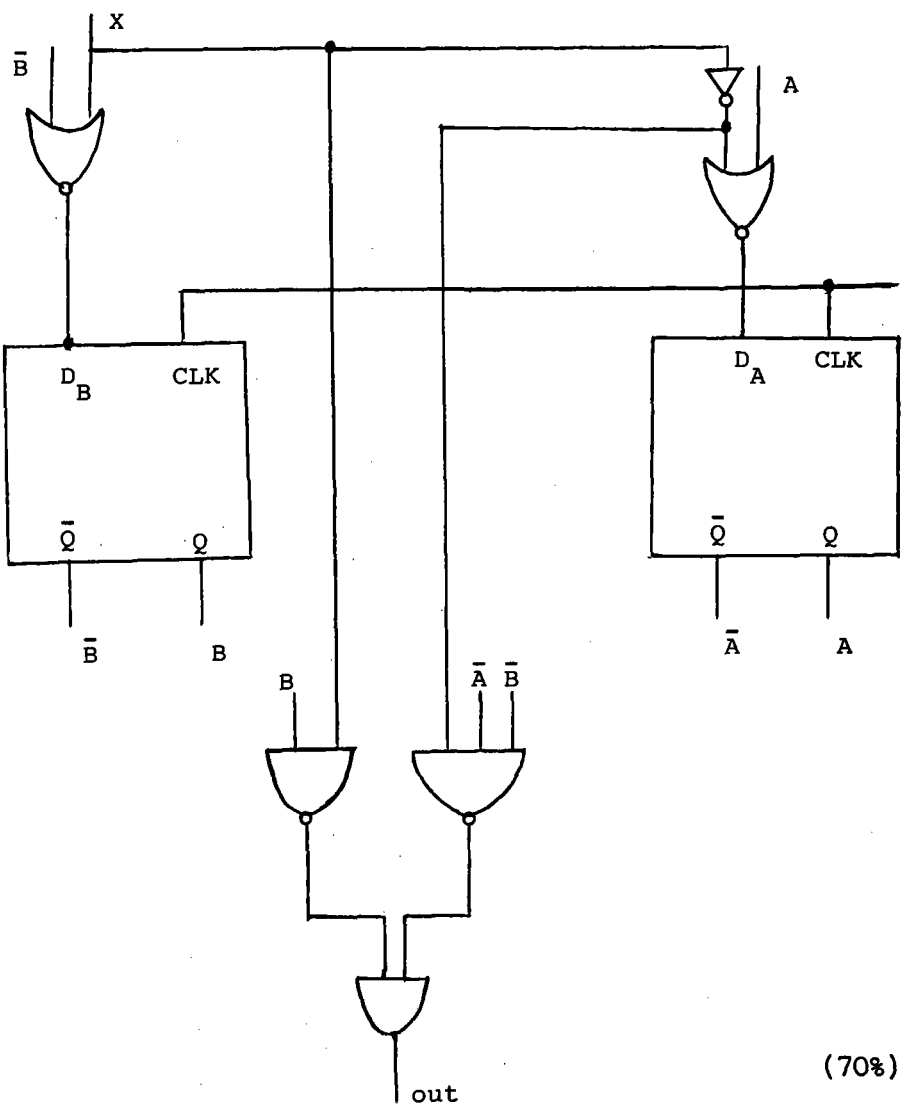
...6/-

Bahagian B

1. (i) Apakah perbezaan di antara litar-litar bergabungan dan litar-litar jujukan.

(30%)

(ii) Analisiskan mesin keadaan di dalam Rajah (2) dengan sepenuhnya.



(70%)

Rajah (2)

2. (i) Apakah suatu sistem segerak utama?

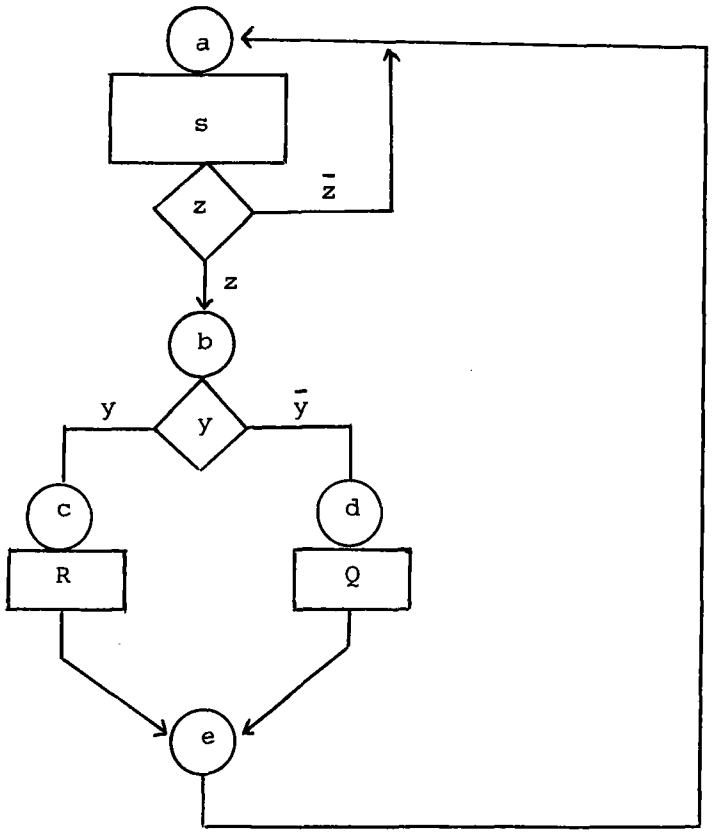
(20%)

(ii) Suatu sistem mensampel suatu talian masukan pada tepi menaik sistem jam. Sistem ini bertugas untuk mengambil empat sampel sebelum kembali kepada keadaan awalnya. Sistem seharusnya mengset suatu keluaran jika jujukan-jujukan 1111 atau 1101 dikesankan. Rekabentukan suatu sistem lengkap dengan menggunakan flip-flop JK. Pastikan sistem anda kembali ke keadaan awal pada tepi-menaik yang keempat denyut jam. Catatan selanjutnya bahawa data di atas talian input bertukar hanya pada tepi-menurun sistem jam.

(80%)

3. (i) Untuk gambarajah keadaan di dalam Rajah (3), tugaskan keadaan-keadaan sedemikian rupa sehingga litar untuk penyahkod keadaan selanjutnya diminimumkan dan juga untuk menyingkirkan keluaran glic. Komenkan terhadap jawapan anda.

...8/-



Rajah (3)

(50%)

(ii) Rekabentukkan suatu pembilang dengan suatu masukan NAIK/TURUN untuk menjanakan jujukan-jujukan berulang 000, 001, 010, 100, 011, 110, 000 ... . Pembilang seharusnya mula-diri.

(50%)

-ooo0ooo-

LAMPIRAN I

54/74107
54LS/74LS107

DUAL JK FLIP-FLOP
(With Separate Clears and Clocks)

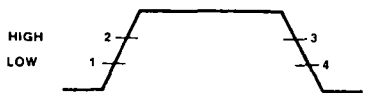
DESCRIPTION — The '107 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



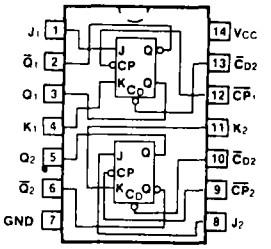
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

The 'LS107 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

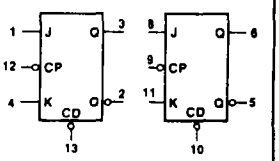
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +125°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74107PC, 74LS107PC		9A
Ceramic DIP (D)	A	74107DC, 74LS107DC	54107DM, 54LS107DM	6A
Flatpak (F)	A	74107FC, 74LS107FC	54107FM, 54LS107FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

LAMPIRAN II

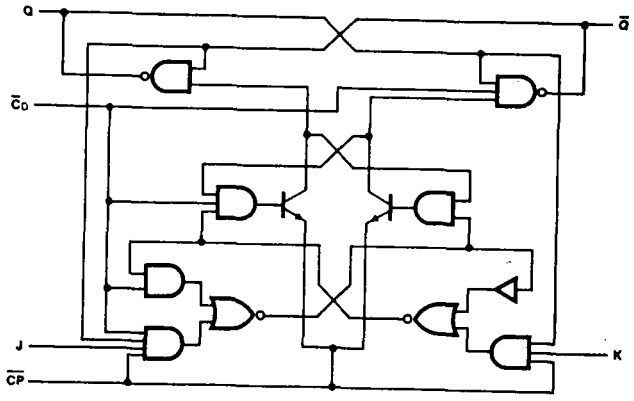
Sambungan 54/74107

54LS/74LS107

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	20/10	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		40		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

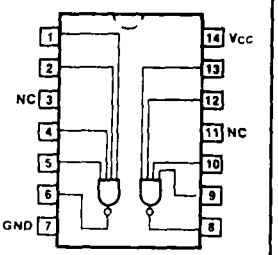
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-10

LAMPIRAN III

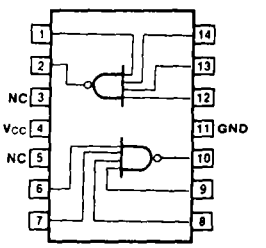
54/7420
54H/74H20
54S/74S20
54LS/74LS20

DUAL 4-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7420PC, 74H20PC 74S20PC, 74LS20PC		9A
Ceramic DIP (D)	A	7420DC, 74H20DC 74S20DC, 74LS20DC	5420DM, 54H20DM 54S20DM, 54LS20DM	6A
Flatpak (F)	A	74S20FC, 74LS20FC	54S20FM, 54LS20FM	3I
	B	7420FC, 74H20FC	5420FM, 54H20FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply	4.0		8.4		8.0		0.8		mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current	11		20		18		2.2			V_{IN} = Open	
t_{PLH}	Propagation Delay	22		10	2.0	4.5	15			ns	Figs. 3-1, 3-4	
t_{PHL}		15		10	2.0	5.0	15					

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

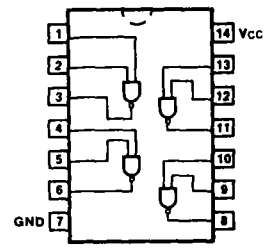
LAMPIRAN IV

54/7437
54LS/74LS37
QUAD 2-INPUT NAND BUFFER

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°c to +125°C	
Plastic DIP (P)	A	7437PC, 74LS37PC		9A
Ceramic DIP (D)	A	7437DC, 74LS37DC	5437DM, 54LS37DM	6A
Flatpak (F)	A	7437FC, 74LS37FC	5437FM, 54LS37FM	3I

CONNECTION DIAGRAM
PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	30/30	30/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		2.5		V	V_{CC} = Max, I_{OH} = -1.2 mA	
		XC	2.4		2.7			V_{IN} = V_{IL}	
V_{OL}	Output LOW Voltage	XM, XC		0.4			V	I_{OL} = 48 mA	V_{CC} = Min, V_{IN} = 2.0 V
		XM				0.4		I_{OL} = 12 mA	
		XC				0.5		I_{OL} = 24 mA	
I_{OS}	Output Short Circuit Current	XM	-20	-70	-30	-130	mA	V_{CC} = Min, V_{OUT} = 0 V	
		XC	-18	-70	-30	-130			
I_{CCH}	Power Supply Current			15.5		2.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				54		12		V_{IN} = Open	
t_{PLH}	Propagation Delay			22		20	ns	Figs. 3-1, 3-4	
t_{PHL}				15		20			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

LAMPIRAN V

54/74121

MONOSTABLE MULTIVIBRATOR

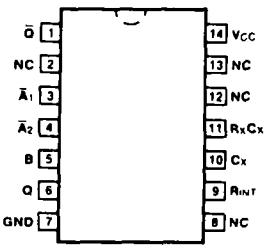
DESCRIPTION — The '121 features positive and negative dc level triggering inputs and complementary outputs. Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers.

When triggering occurs, internal feedback latches the circuit, prevents re-triggering while the output pulse is in progress and increases immunity to negative-going noise. Noise immunity is typically 1.2 V at the inputs and 1.5 V on V_{CC}.

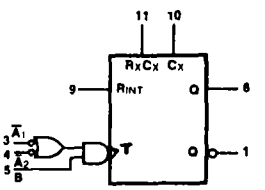
Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application. A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent. Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor. Duty cycles beyond this range tend to reduce the output pulse width. Otherwise, output pulse width follows the relationship:

$$t_w = 0.69\ R_X C_X$$

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2.0/2.0
Q, $\overline{Q}$	Outputs	20/10

NE 555 Monostable