UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2008/2009

November 2008

EEE 105 – TEORI LITAR I

Masa : 3 Jam

ARAHAN KEPADA CALON:-

Sila pastikan kertas peperiksaan ini mengandungi **DUABELAS** muka surat bercetak dan **ENAM** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah diberikan di sudut sebelah kanan soalan berkenaan.

Semua soalan hendaklah dijawab di dalam Bahasa Malaysia atau Bahasa Inggeris.

1. (a) Voltan dan arus pada terminal satu elemen litar adalah:

The voltage and current at the terminals of one circuit element are:

$$v = \begin{cases} 0\,V & ;t < 0 \\ e^{-500t} - e^{-1500t}\ V & ;t \geq 0 \end{cases}$$

$$i = \begin{cases} 0\ mA & ;t < 0 \\ 30 - 40e^{-500t} + 10e^{-1500t}\ mA & ;t \geq 0 \end{cases}$$

(i) Dapatkan kuasa pada t = 1 ms.

Find the power at t = 1 ms.

(ii) Berapa banyak tenaga yang dibekalkan kepada elemen litar tersebut di antara 0 dan 1 ms?

How much energy is delivered to the circuit element between 0 and 1 ms?

(iii) Dapatkan jumlah tenaga yang dibekalkan kepada elemen tersebut.

Find the total energy delivered to the element.

(40%)

(b) Berdasarkan Rajah 1:

Based on Figure 1:

(i) Dapatkan bilangan nod dan cabang.

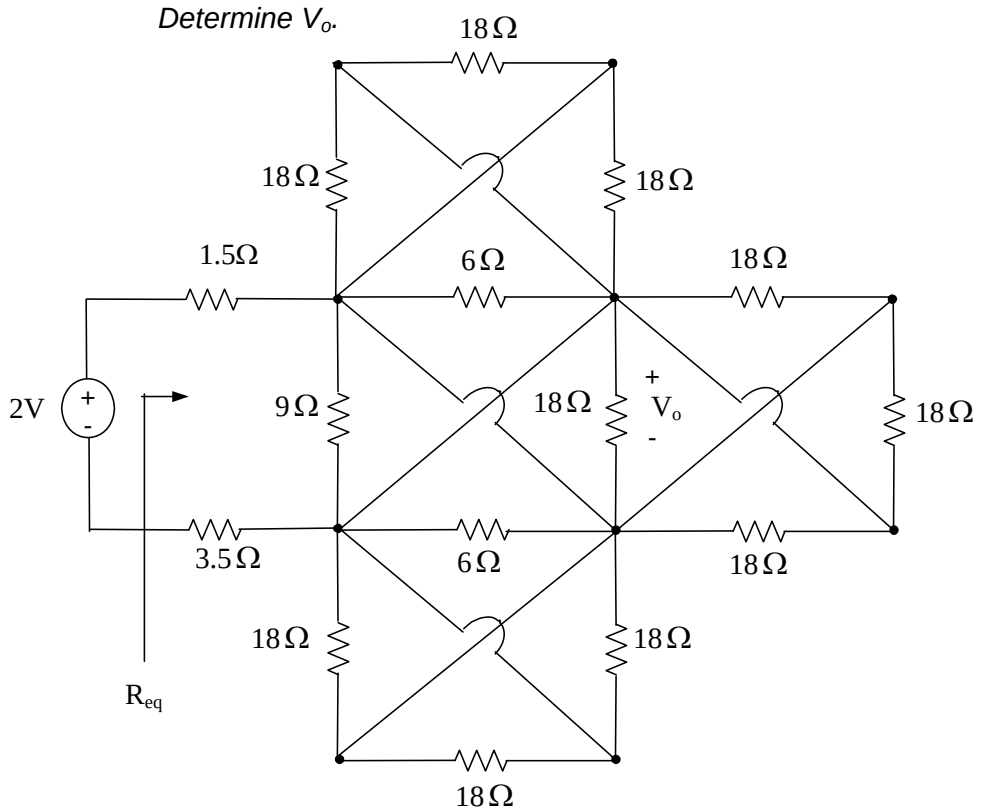
Determine number of nodes and branches.

(ii) Tanpa menggunakan transformasi wye-delta, dapatkan R_{eq}. (Saranan: Lukis semula litar tersebut).

Without using wye-delta transformation, find R_{eq}. (Hint: Redraw the circuit).

(iii) Dapatkan V_o.

Determine V_o.



Rajah 1
Figure 1

(60%)

2. (a) Berdasarkan Rajah 2(a).

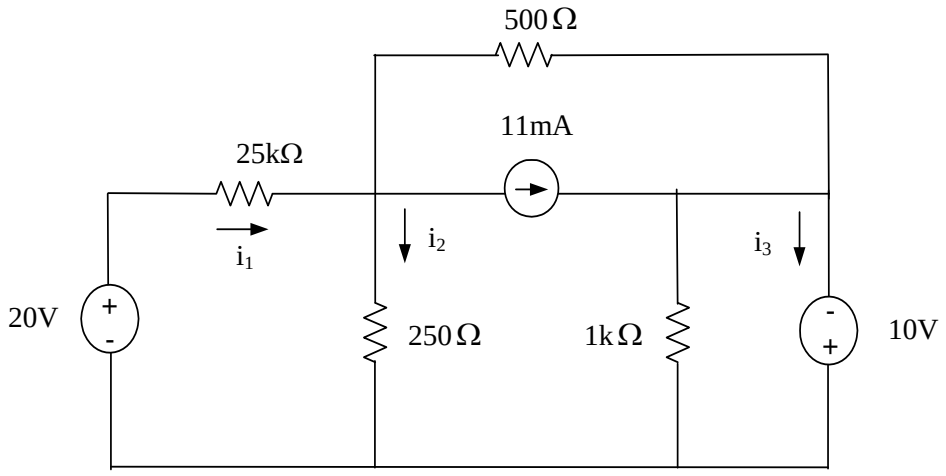
Based on Figure 2(a).

(i) Dengan menggunakan analisis nod, dapatkan semua voltan nod dan dapatkan arus cabang i_1, i_2 dan i_3.

By using nodal analysis, find all node-voltages and find the branch currents i_1, i_2 and i_3.

(ii) Dapatkan kuasa yang dilesap dan dijana.

Find the total power dissipated and developed.



Rajah 2(a)
Figure 2(a)

(55%)

(b) Berdasarkan Rajah 2(b), di bawah keadaan dc, dapatkan

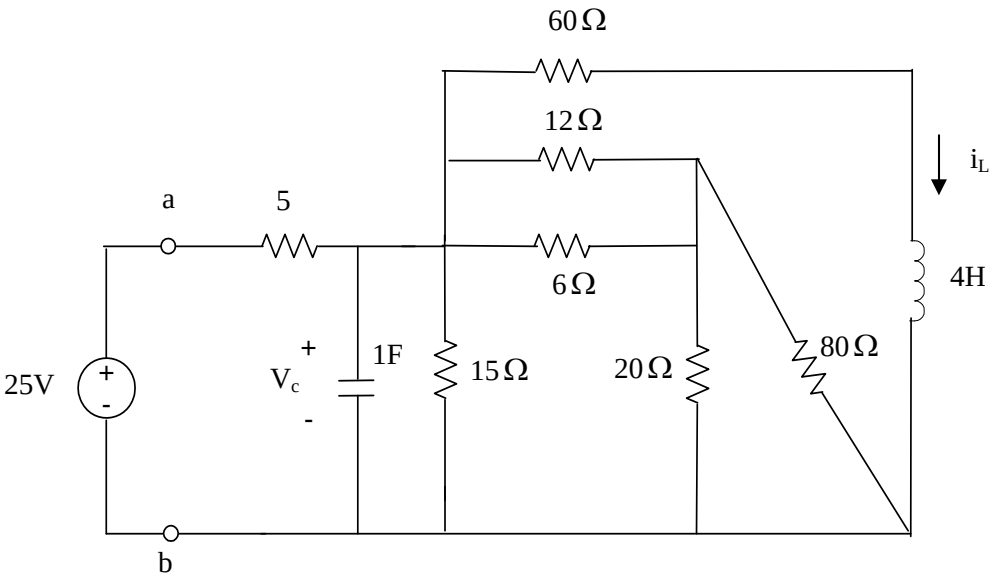
Based on Figure 2(b), under dc condition, find

(i) R_{eq} pada terminal a-b

R_{eq} at terminal a-b

(ii) i_L

(iii) V_c

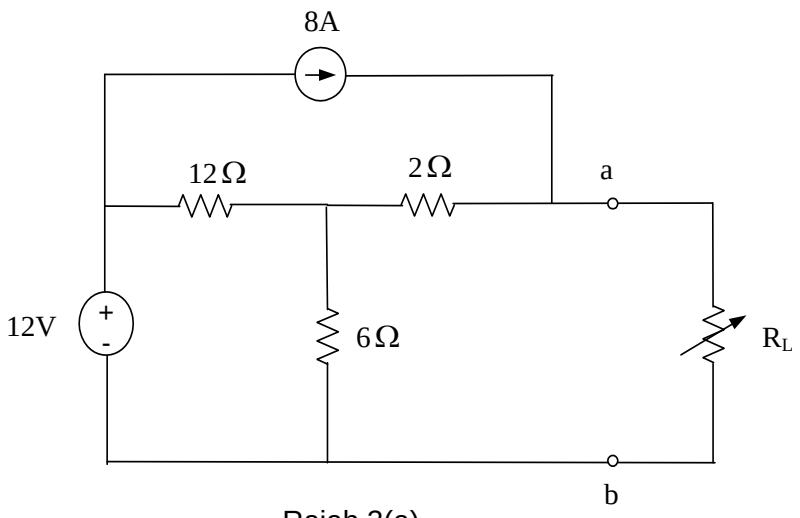


Rajah 2(b)
Figure 2(b)

(45%)

3. (a) Dapatkan litar setara Thevenin pada terminal a-b untuk litar dalam Rajah 3(a). Kemudian, dapatkan kuasa maksimum yang dihantar kepada R_L.

Find the Thevenin equivalent circuit at terminal a-b for circuit in Figure 3(a). Then, determine the maximum power transferred to R_L.

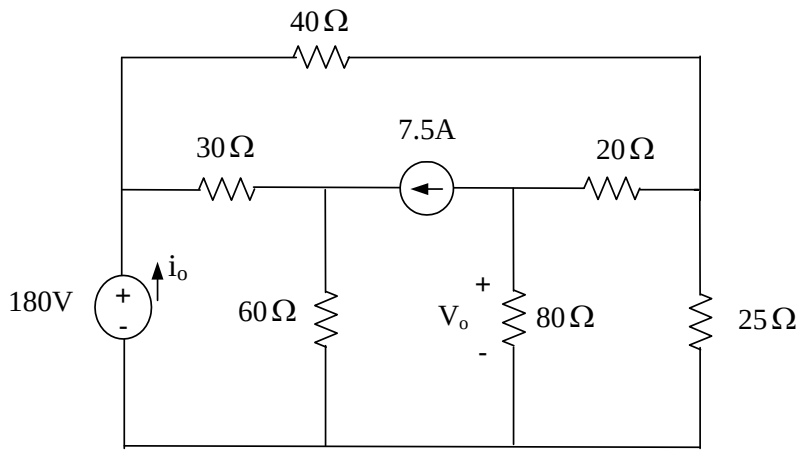


Rajah 3(a)
Figure 3(a)

(35%)

(b) Dengan menggunakan teorem superposisi dan analisis nod, dapatkan i_o dan v_o dalam litar yang ditunjukkan dalam Rajah 3(b).

By using superposition theorem and nodal analysis, find i_o and v_o in the circuit shown in Figure 3(b).



Rajah 3(b)
Figure 3(b)

(65%)

4. (a) Kedua-dua suis di dalam litar Rajah 4(a) ditutup lama. Pada masa $t = 0$, suis 1 dibuka. Kemudian selepas 35 ms, suis 2 pula dibuka.

The two switches in the circuit shown in Figure 4(a) have been closed for a long time. At $t = 0$, switch 1 is opened. Then 35 ms later, switch 2 is opened.

(i) Cari $i_L(t)$ untuk $0 \leq t \leq 35$ ms.
Find $i_L(t)$ for $0 \leq t \leq 35$ ms.

(10%)

(ii) Cari $i_L(t)$ untuk $t \geq 35$ ms.
Find $i_L(t)$ for $t \geq 35$ ms.

(10%)

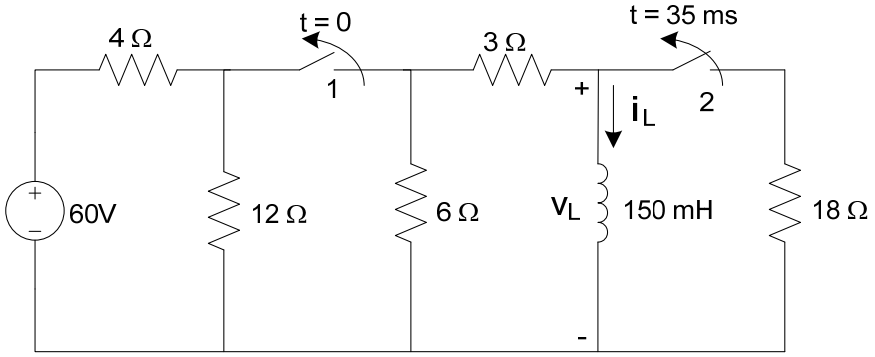
(iii) Apakah peratusan daripada tenaga inisial tersimpan di dalam pengaruh 150 mH yang telah dibebaskan pada perintang $18\,\Omega$?

What percentage of the initial energy stored in the 150 mH inductor is dissipated in the $18\,\Omega$ resistor?

(20%)

(iv) Ulangkan (iii) bagi perintang-perintang $3\,\Omega$ dan $6\,\Omega$.
Repeat (iii) for the $3\,\Omega$ and $6\,\Omega$ resistors.

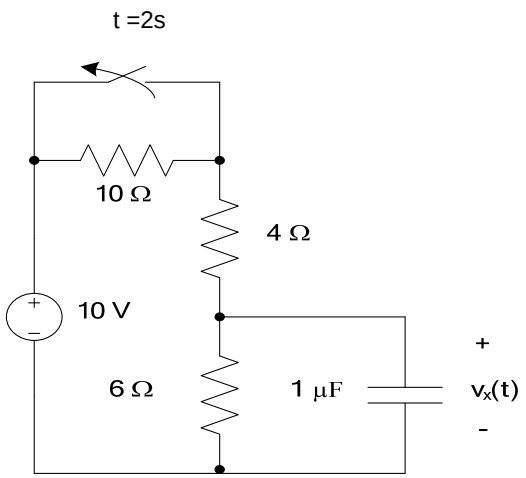
(20%)



Rajah 4(a)
Figure 4(a)

(b) Rujuk Rajah 4(b) untuk menjawab soalan-soalan berikut:

Refer to Figure 4(b) to answer the following questions:



Rajah 4(b)
Figure 4(b)

(i) Tentukan $v_x(t)$ sekiranya suis S1 dibuka pada t =2s.

Determine $v_x(t)$ if switch S1 opens at t =2s.

(20%)

(ii) Apakah masa pemalar bagi litar ini?

What is the time constant for this circuit?

(10%)

(iii) Apakah sambutan berkenaan yang ditentukan pada (i)?

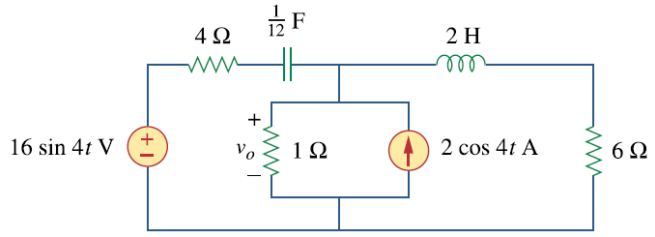
What is the corresponding response determined in (i)?

(10%)

5. (a) Dapatkan v_0 dari litar di Rajah 5(a).

Determine v_0 in the circuit of Figure 5(a).

(30%)

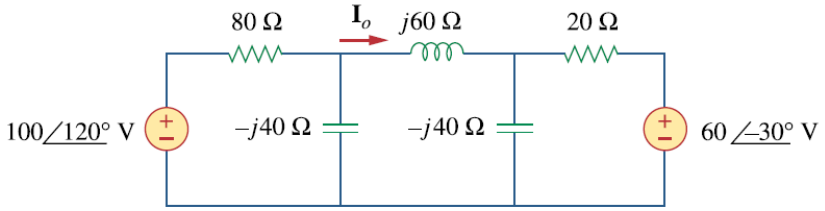


Rajah 5(a)
Figure 5(a)

(b) Tentukan arus $\mathbf{I}_0$ dalam litar di Rajah 5(b) dengan menggunakan kaedah analisis jejaring.

Determine current $\mathbf{I}_0$ in the circuit of Figure 5(b) using mesh analysis.

(30%)

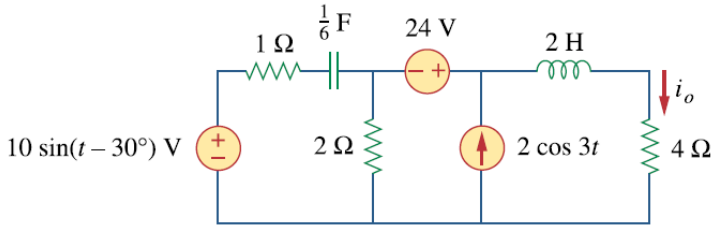


Rajah 5(b)
Figure 5(b)

(c) Gunakan kaedah prinsip tindihan untuk mengira i_0 di dalam litar Rajah 5(c).

Use superposition principle to determine i_0 in the circuit of Figure 5(c).

(40%)

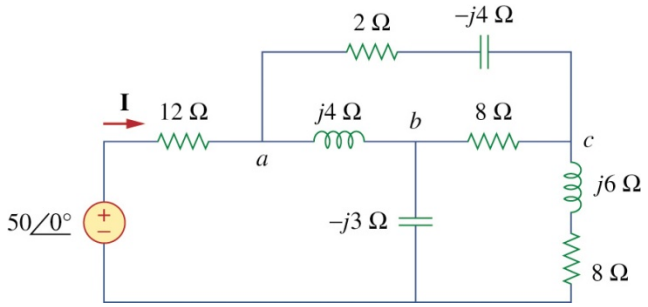


Rajah 5(c)
Figure 5(c)

6. (a) Kirakan arus $\mathbf{I}$ dalam litar di Rajah 6(a).

Find current $\mathbf{I}$ in the circuit of Figure 6(a).

(50%)



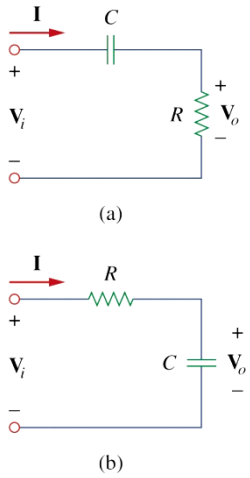
Rajah 6(a)
Figure 6(a)

(b) Jawab soalan-soalan berikut.
Answer following questions.

(i) Terangkan mengapa frekuensi bagi litar-litar di dalam Rajah 6 (a) dan (b) dikatakan tidak berubah walaupun perintang dan kapasitor telah diubah posisi masing-masing.

Explain why the frequencies in Figure 6 (a) and (b) below are said to be the same even though the resistor and capacitor are switched in their position.

(20%)



Rajah 6 (a) dan (b)
Figure 6(a) and (b)

(ii) Berdasarkan perubahan tempat tersebut, apakah perbezaan yang dapat diperhatikan. Terangkan.

Based on the position changed, what are the differences can be observed. Explain.

(20%)

(iii) Apakah nama litar ini?
What is the name of the circuit?

(10%)

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