UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama

Sidang Akademik 1999/2000

September 1999

IQK 211 - SISTEM DIGIT

Masa: [3 jam]

Sila pastikan bahawa kertas soalan ini mengandungi **SEMBILAN (9)** mukasurat yang bercetak termasuk lampiran sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan. Semua soalan mesti dijawab di dalam **Bahasa Malaysia**.

1. (a) Apakah number BCD yang dihantar kepada suatu voltmeter digit 3-angka yang mengukur 135 Volts?

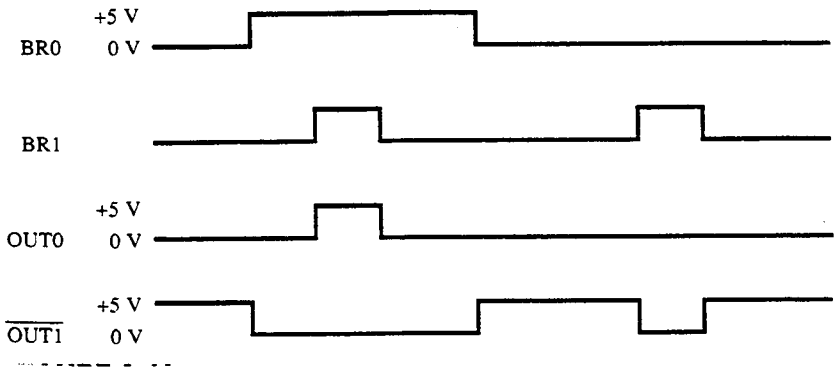
(20 markah)

(b) Rujuk kepada bentuk-bentuk gelombang di Rajah 1. Dengan input BR0 dan BR1, lukis get logik yang mengeluarkan:

(40 markah)

(i) output OUT0

(ii) output $\overline{OUT1}$



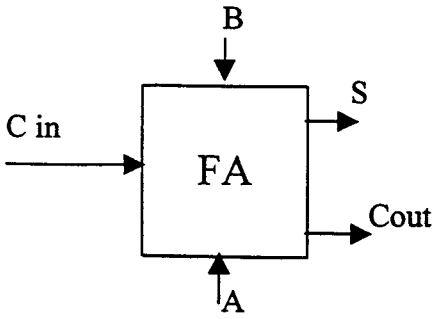
Rajah 1

(c) Ringkaskan persamaan berikut dan bina litar logiknya dengan get-get NAND.

$$X = \overline{A \cdot \overline{B}} + A.\overline{(A + \overline{C})}$$

(40 markah)

2. (a) Rekabentuk litar pejumlah penuh (Full Adder) 1-bit dalam Rajah 2.
NOTA: Ambil perhatian bahawa litar ini mempunyai 2-output.

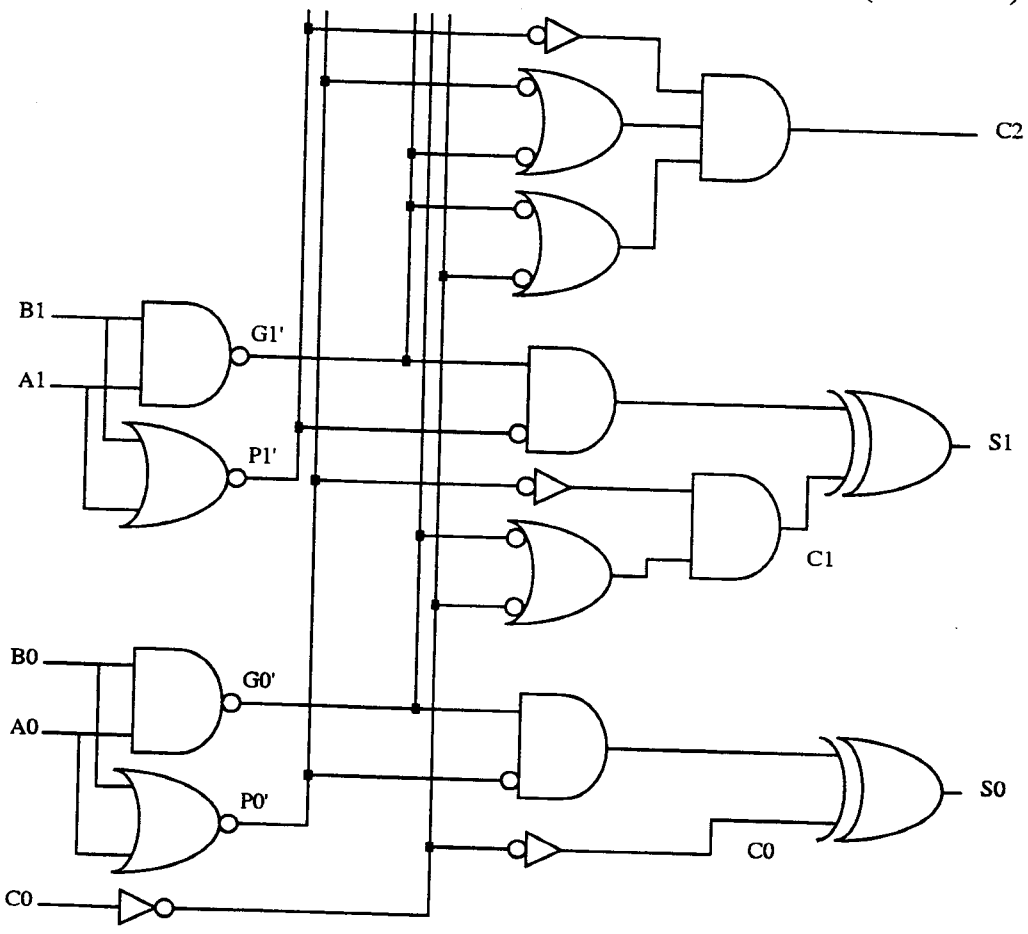


Rajah 2

(40 markah)

(b) Buktikan sama ada litar dalam Rajah 3 merupakan suatu pejumlah 2-bit.

(60 markah)



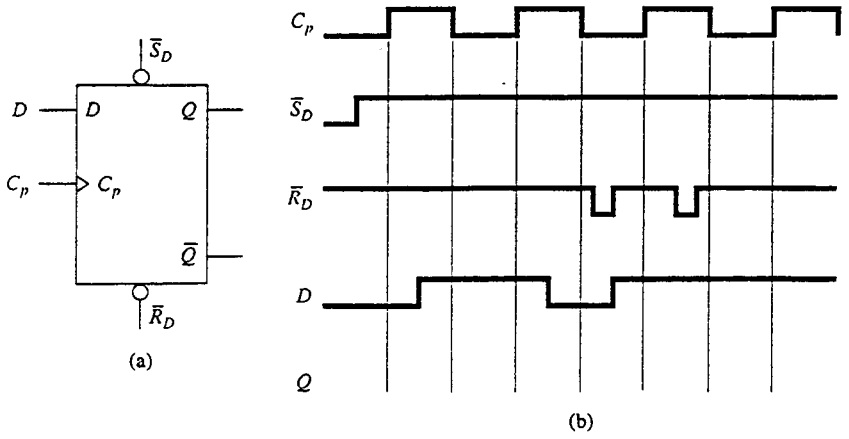
Rajah 3

3. (a) Terangkan input-input segerak dan taksegerak bagi sesuatu flip-flop. Bagi flip-flop D di Rajah 4a, apakah input-input segerak dan input-input taksegerak?

(20 markah)

(b) Lakarkan bentuk gelombang output Q, diberi input-input C_p, D, S_D, R_D di Rajah 4.

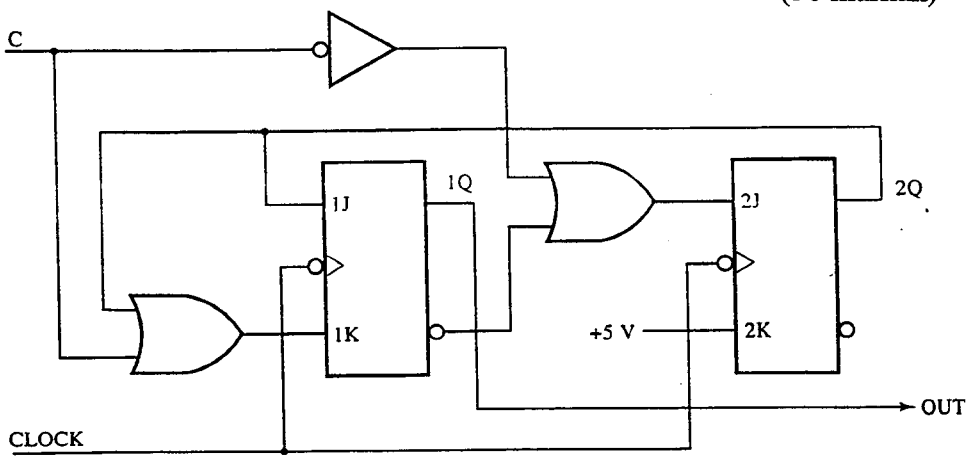
(30 markah)



Rajah 4

(c) Analisakan operasi litar di Rajah 5 bagi kedua-dua nilai input kawalan C. Buat demikian melalui rajah keadaan dan jadual keadaan. Jika frekuensi jam adalah 1.2 MHz, apakah frekuensi pada output 1Q apabila C=0 dan C=1?

(50 markah)



Rajah 5

4. Rujuk kepada litar di Rajah 6.

(a) Kenapakah songsang pemicu Schmitt (Schmitt Inverter) digunakan dalam litar astabil ini dan bukan suatu songsang biasa seperti 7404?

(25 markah)

(b) Terangkan operasi litar ini dan lakarkan bentuk-bentuk gelombang pada V_c dan $V_{out.}$ Spesifikasi 74HC14 dengan pembekal kuasa 6V adalah:

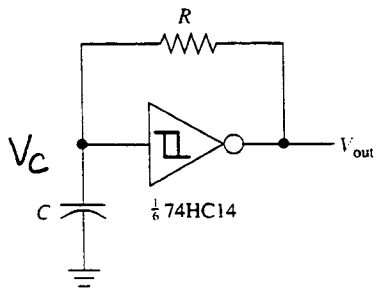
$V_{OH} = 6.0$ V, $V_{OL} = 0.0$ V, $V_{T+} = 3.3$ V and $V_{T-} = 2.0$ V.

(35 markah)

(c) Dalam litar ini, jika voltan histeresis (V_{T+} - V_{T-}) dikurang disebabkan oleh perubahan suhu, apakah yang berlaku pada:

(i) frekuensi output (ii) voltan output

(40 markah)



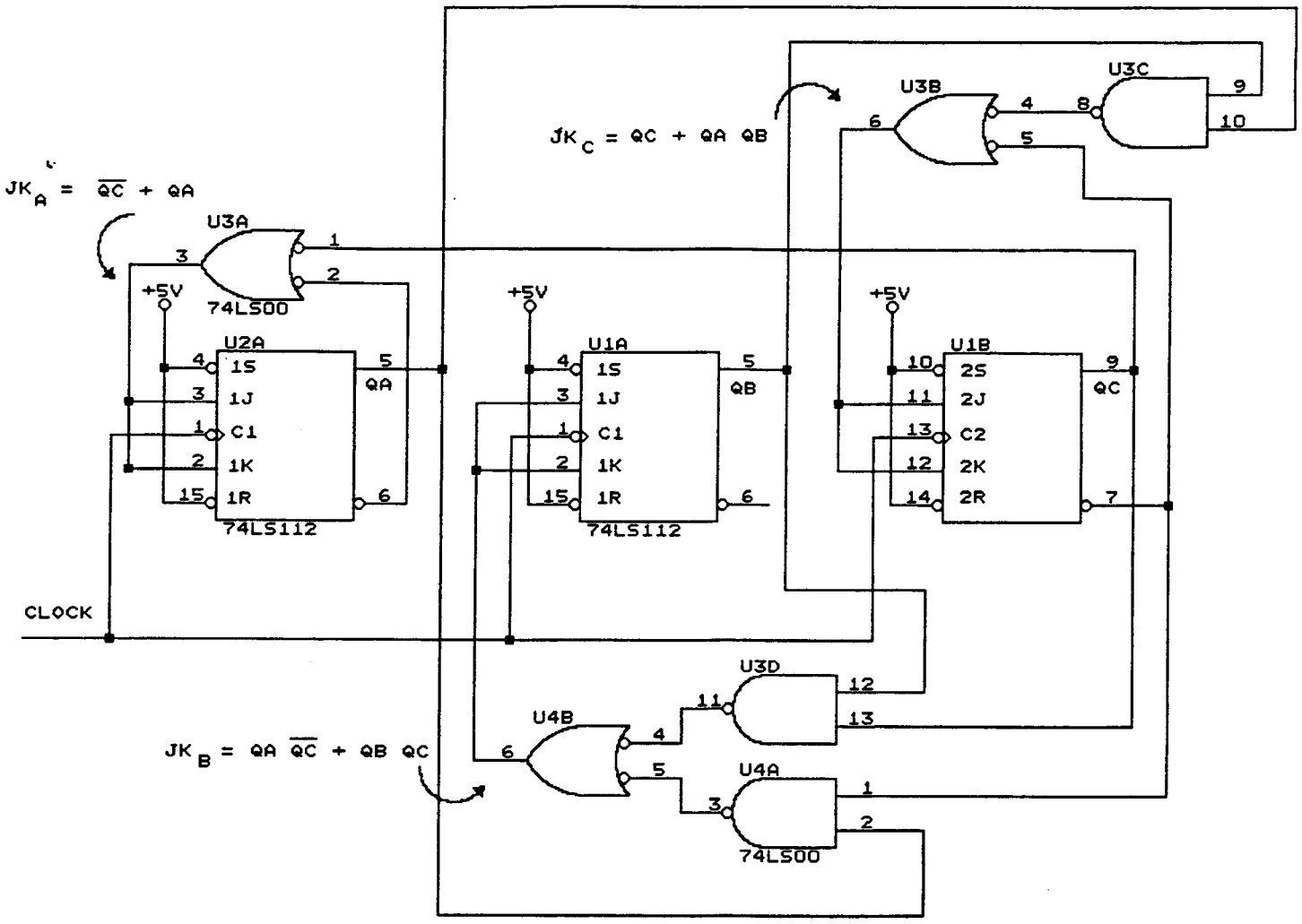
Rajah 6

5. (a) Rekabentuk pembilang menurun MOD-6 dengan menggunaksn 74193. (rujuk kepada Lampiran A)

(40 markah)

(c) Analisakan litar dalam Rajah 7, tulis jadual keadaan dan lukis rajah keadaan bagi litar itu.

(60 markah)



Rajah 7

6. (a) Apakah perintang tarik keatas? Kenapakah ia digunakan?

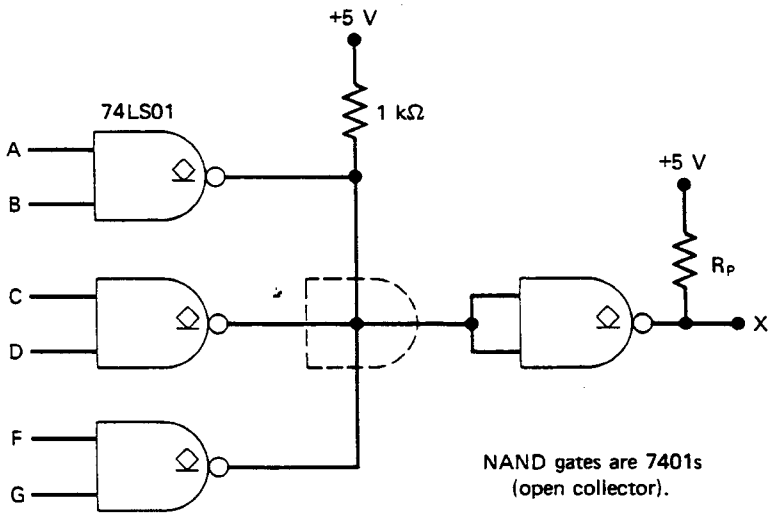
(20 markah)

(b) Kenalpasti persamaan logik bagi output X dalam Rajah 8.

(30 markah)

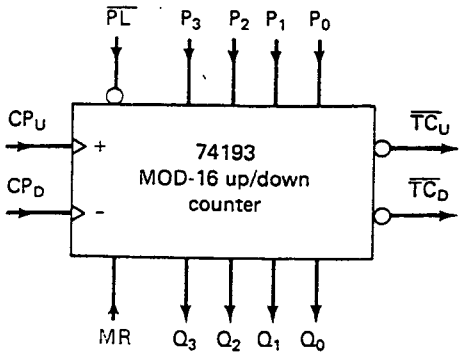
(c) Tentukan nilai R_p dalam Rajah 8 jika output X mendorong input bersih (Clear input) bagi 4 flip-flop jenis 74LS112.
(Nota: Rujuk kepada kertas data dalam Lampiran B)

(50 markah)



Rajah 8

LAMPIRAN A



(a)

Mode Select

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Asynch. reset
L	L	X	X	Asynch. preset
L	H	H	H	No change
L	H	↑	H	Count up
L	H	H	↑	Count down

H = HIGH; L = LOW
X = Don't care; ↑ = PGT

(c)

Pin Names	Description
CP_U	Count-up clock input (active rising edge)
CP_D	Count-down clock input (active rising edge)
MR	Asynchronous master reset input (active HIGH)
$\overline{PL}$	Asynchronous parallel load input (active LOW)
P_0-P_3	Parallel data inputs
Q_0-Q_3	Flip-flop outputs
$\overline{TC_D}$	Terminal count-down (borrow) output (active LOW)
$\overline{TC_U}$	Terminal count-up (carry) output (active LOW)

(b)

74193 MOD-16 UP/DOWN COUNTER

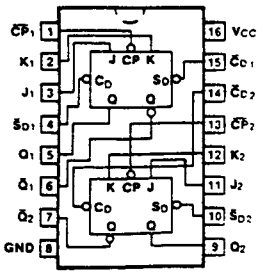
LAMPIRAN B

54S/74S112
54LS/74LS112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '112 features individual J, K, Clock and asynchronous Set and Clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

CONNECTION DIAGRAM
PINOUT A



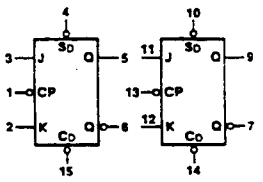
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S112PC, 74LS112PC		9B
Ceramic DIP (D)	A	74S112DC, 74LS112DC	54S112DM, 54LS112DM	6B
Flatpak (F)	A	74S112FC, 74LS112FC	54S112FM, 54LS112FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.5/2.5	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.5/4.375	1.5/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

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