UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2001/2002

September 2001

IQK 211 – SISTEM DIGIT

Masa : 3 jam

Sila pastikan bahawa kertas peperiksaan ini mengandungi ENAM BELAS muka surat yang bercetak sebelum anda memulakan peperiksaan ini.

Jawab LIMA soalan. Semua soalan mesti dijawab dalam Bahasa Malaysia.

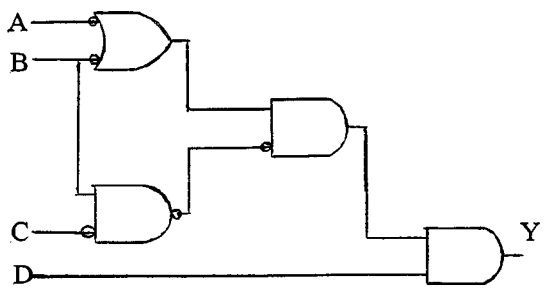
Nota:

- Gunakan Appendix A untuk memberi jawapan yang memerlukan bentuk gelombang-bentuk gelombang.
- Data bagi semua litar terkamil di beri dalam Appendix B.

...2/-

1. (a) Merujuk kepada litar di Rajah 1, tanpa menulis jadual kebenaran atau persamaan Boolean, tentukan syarat – syarat input yang mengaktifkan output. Daripada syarat-syarat ini bina jadual kebenaran.

(5 markah)



Rajah 1

(b) Dengan menggunakan teorem Boolean dan Syarat De'Morgan kurangkan persamaan berikut.

(5 markah)

$$Z = \overline{A}C(\overline{\overline{A}BD}) + \overline{A}B\overline{CD} + A\overline{B}C$$

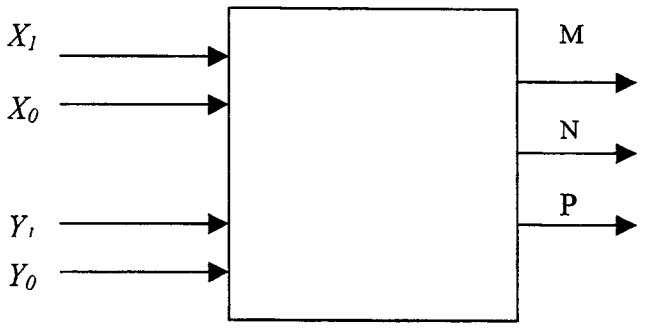
(c) Rajah 2 mewakili satu pengesan magnitud-relatif yang mengambil dua nombor binary 2-bit $x\ (x_1\ x_0)$ dan $y\ (y_1\ y_0)$ dan tentukan sama ada dua nombor ini adalah sama dan, jika tidak, yang manakah di antaranya lebih besar. Terdapat tiga keluaran yang ditakrifkan berikut:

- M = 1 hanya jika kedua-dua nombor masukan adalah sama
- N = 1 hanya jika x adalah lebih besar daripada y
- P = 1 hanya jika y adalah lebih besar daripada x

Rekabentuk pengesan magnitud-relatif ini.

(10 markah)

...3/-



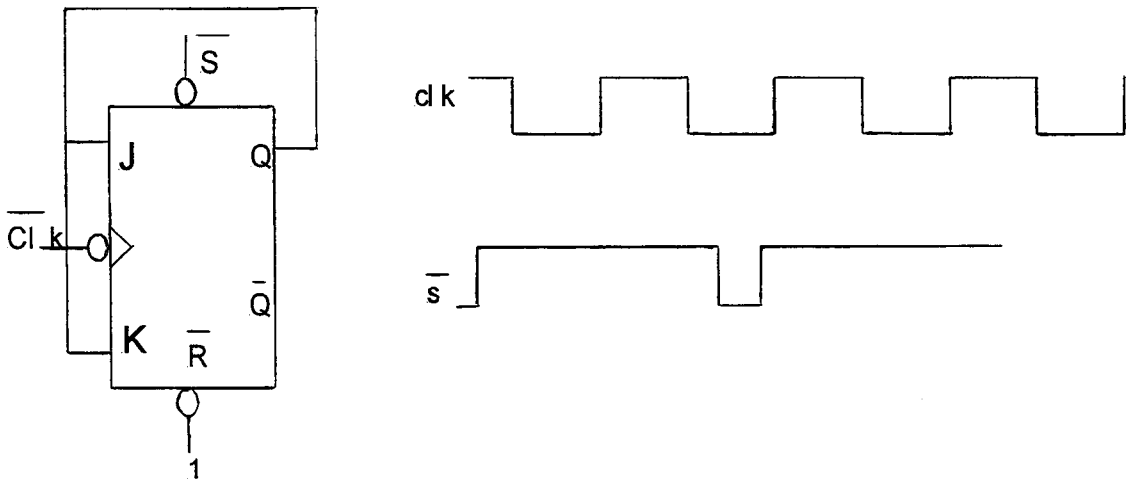
Rajah 2

2. (a) Jelaskan input-input segerak dan tak segerak flip-flop.

(6 markah)

(b) Bagi litar di Rajah 3, lakarkan bentuk gelombang pada output Q

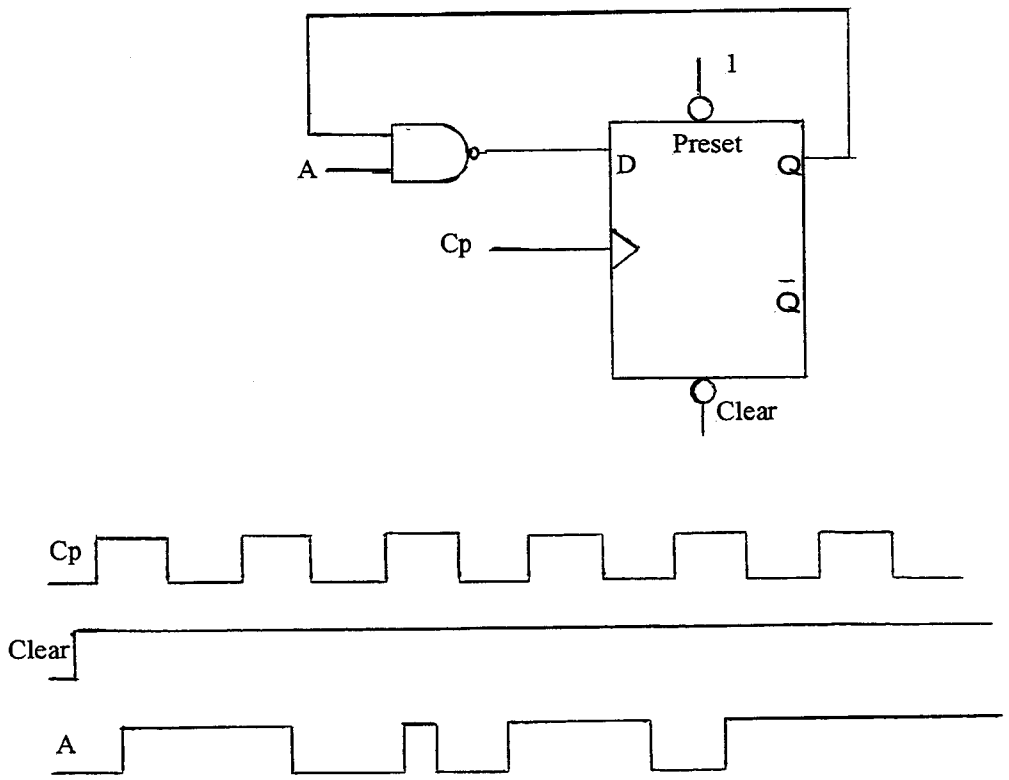
(7 markah)



Rajah 3

(c) Dalam litar di Rajah 4, input-input adalah seperti yang diberikan. Lakarkan bentuk-bentuk gelombang pada D dan Q.

(7 markah)



Rajah 4

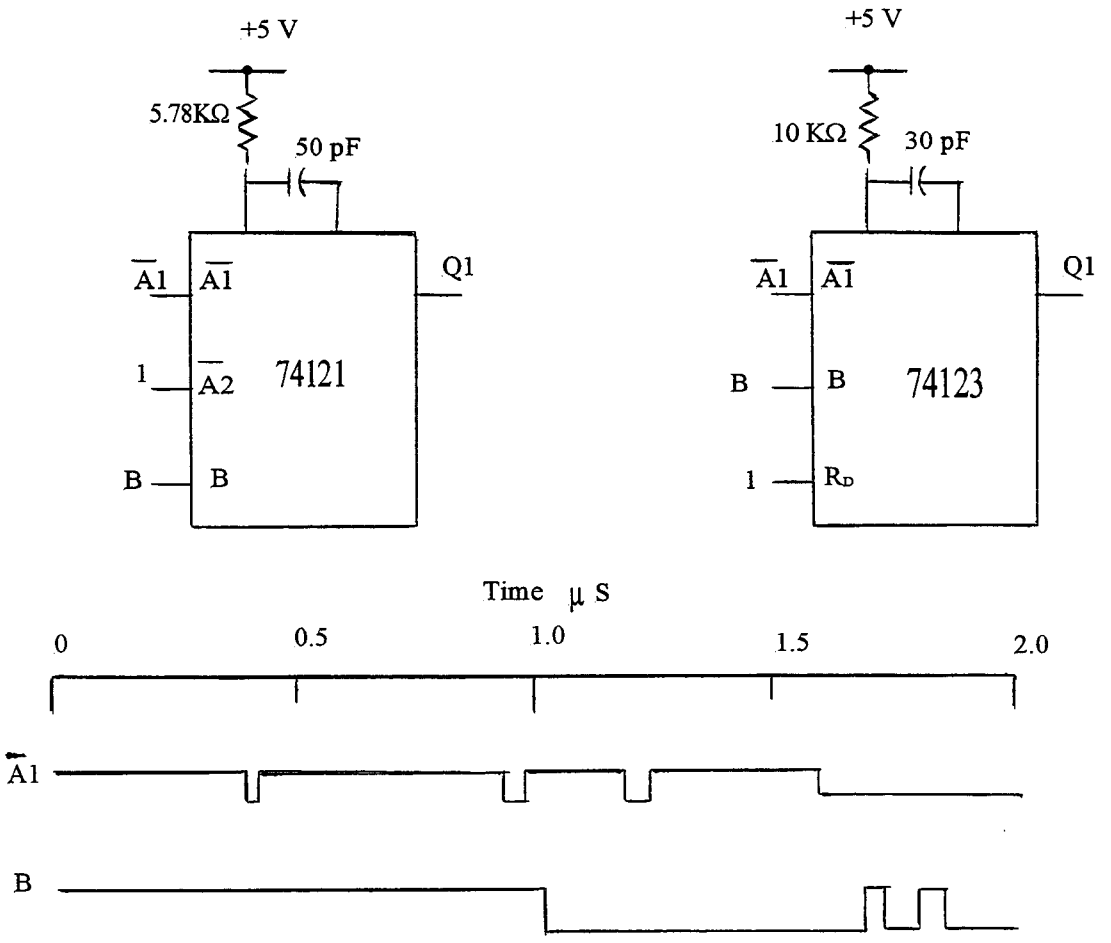
3. (a) Dengan menggunakan bentuk-bentuk gelombang yang sesuai, jelaskan perbezaan di antara monostabil boleh di picu semula dan monostabil tidak boleh di picu semula.

(6 markah)

...5/-

(b) Lakarkan output Q_1 dan Q_2 bagi litar-litar monostabil di Rajah 5.

(8 markah)

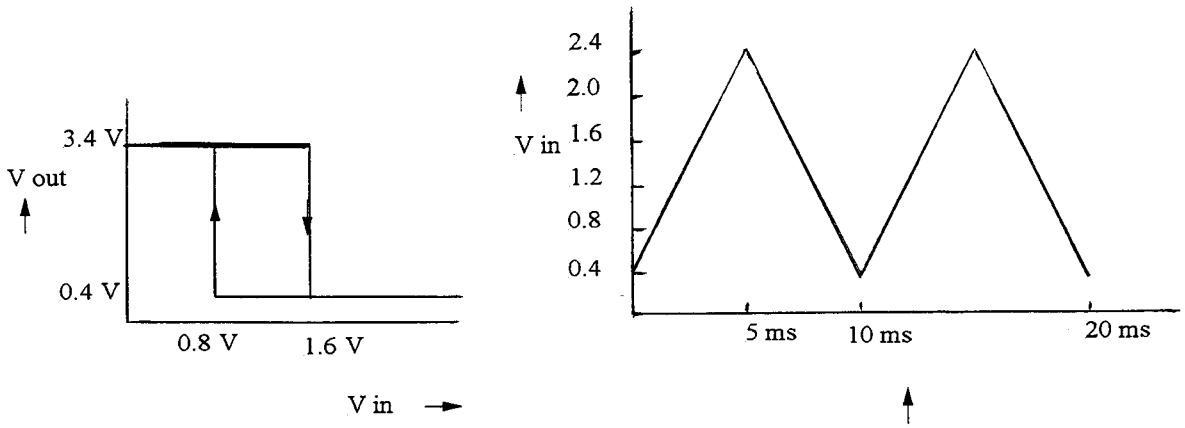


Rajah 5

...6/-

(c) Ciri-ciri suatu songsang Schmitt (Schmitt Inverter) di beri dalam Rajah 6a. Jika bentuk gelombang di Rajah 6b diberi sebagai input kepada litar Schmitt ini, lakarkan ouput V_{out} dan tentukan kitar tugasnya.

(6 markah)



(a) (b)

Rajah 6

4. (a) Jelaskan fungsi Penyahmultipleks melalui gambrajah-gambarajah yang sesuai.

(5 markah)

(b) Terangkan penggunaan 74138 sebagai penyahmultipleks.

(5 markah)

(c) Rekabentuk penyahmultipleks 16 – bit dengan menggunakan 74138.

(10 markah)

...7/-

5. (a) Lukiskan litar get asas TTL dan terangkan operasinya.

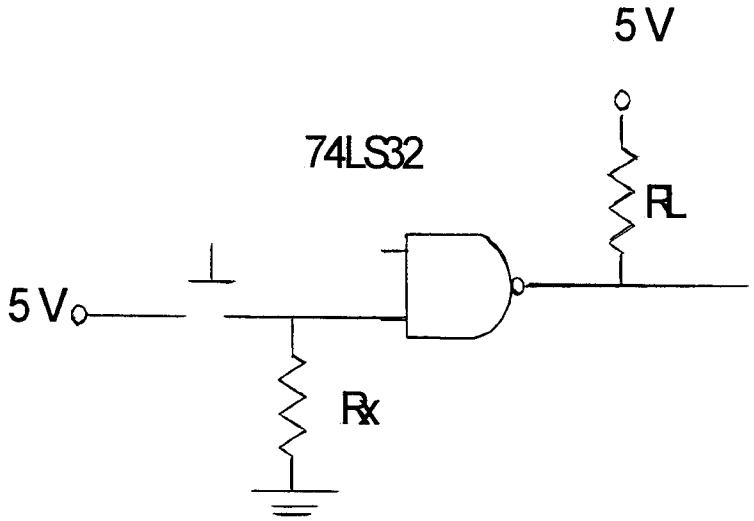
(7 markah)

(b) Jelaskan konsep-konsep "Current Sourcing" dan "Current Sinking"

(5 markah)

(c) Tentukan had perintang R_L dan R_X di Rajah 7.

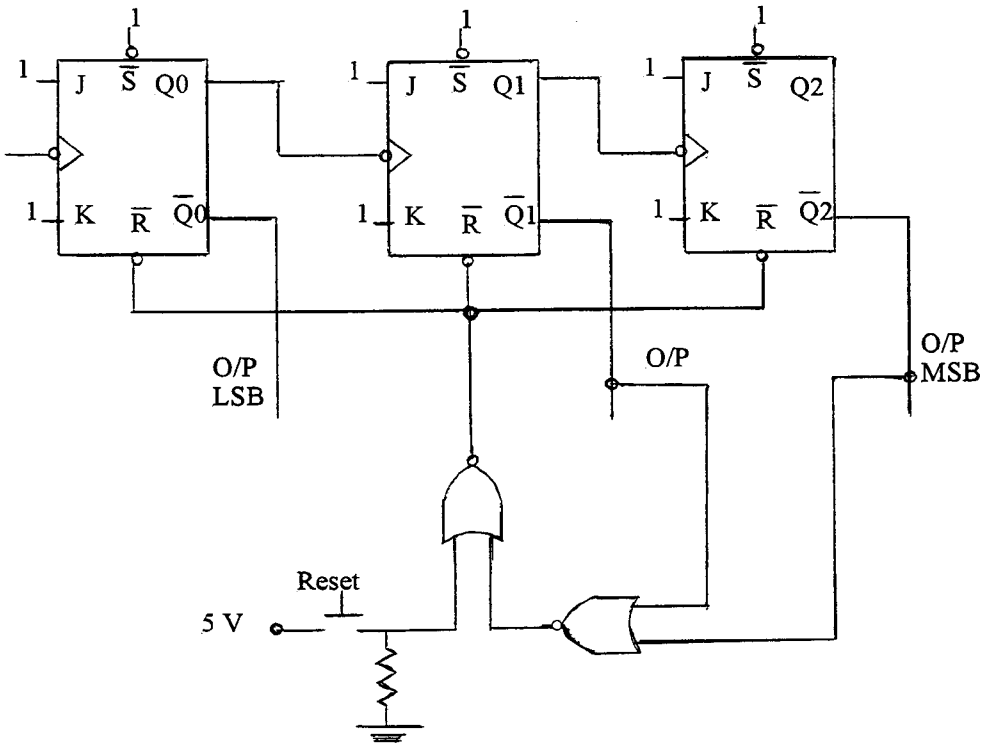
(8 markah)



Rajah 7

6. (a) Jelaskan operasi Pembilang dalam Rajah 8 dengan menggunakan Rajah-Rajah yang sesuai.

(10 markah)



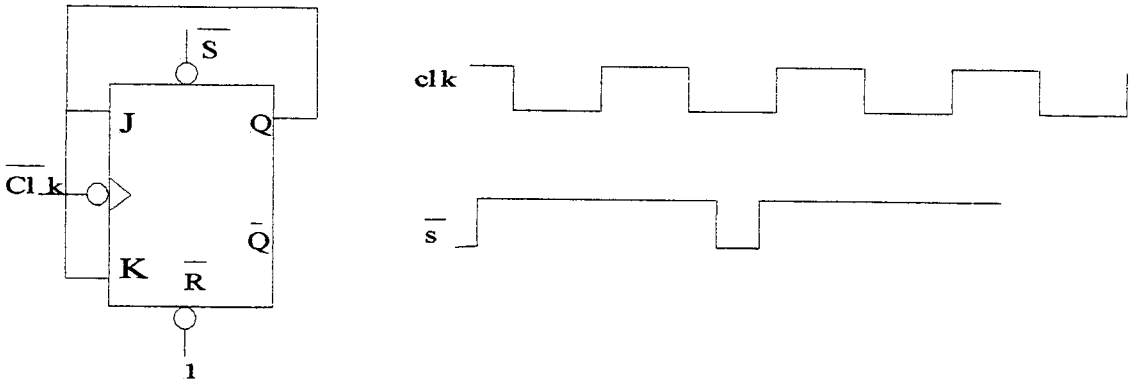
Rajah 8

(b) Rekabentuk suatu pembilang MOD-12 dengan menggunakan 74293.

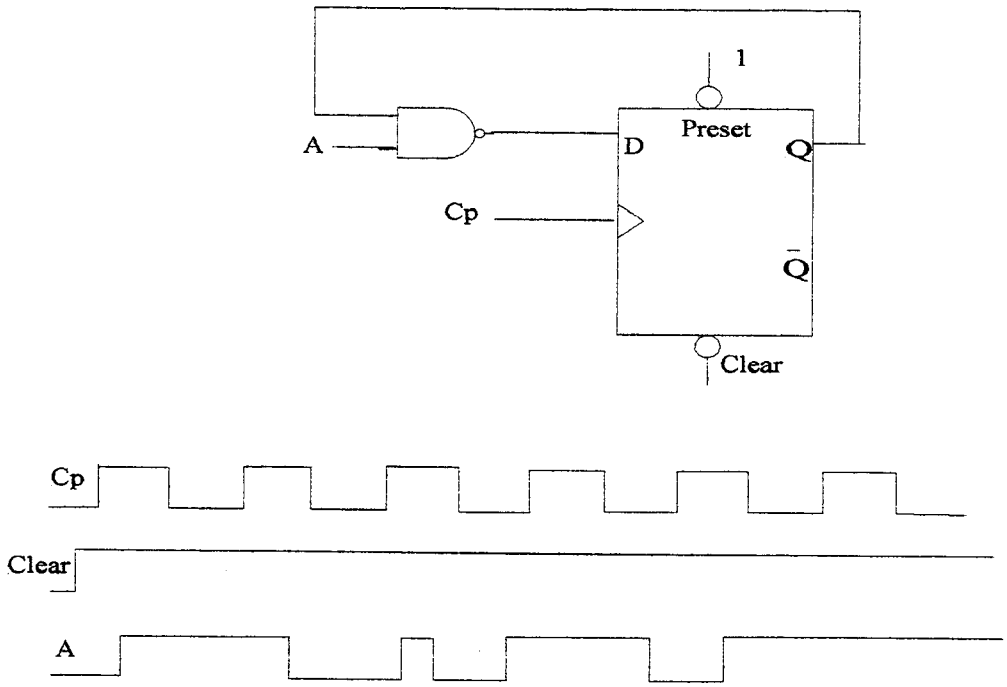
(10 markah)

...9/-

APPENDIX A

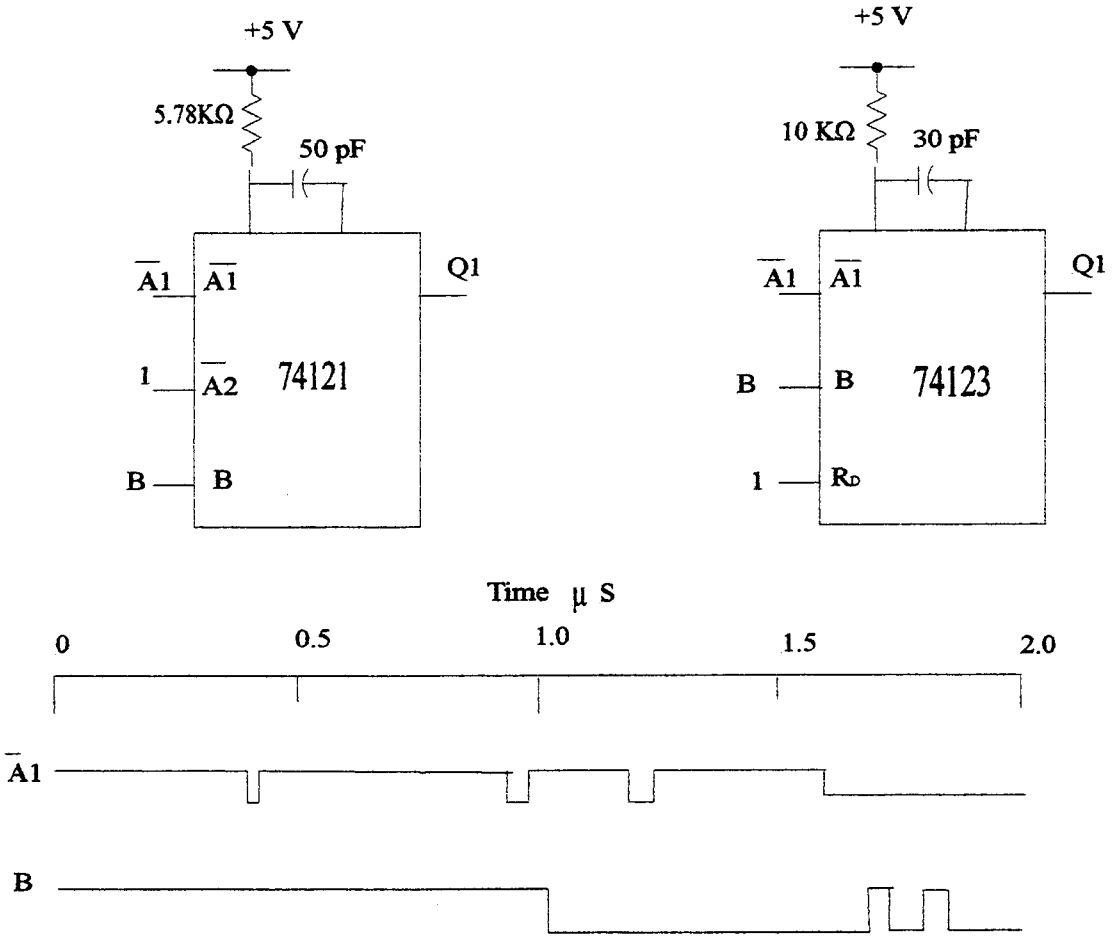


Rajah 3



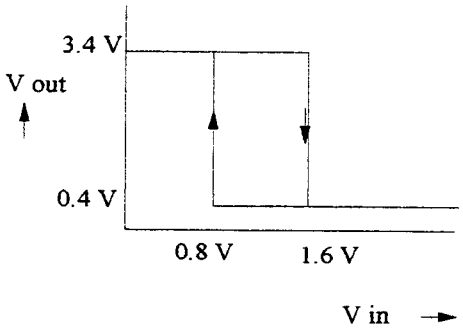
Rajah 4

...10/-

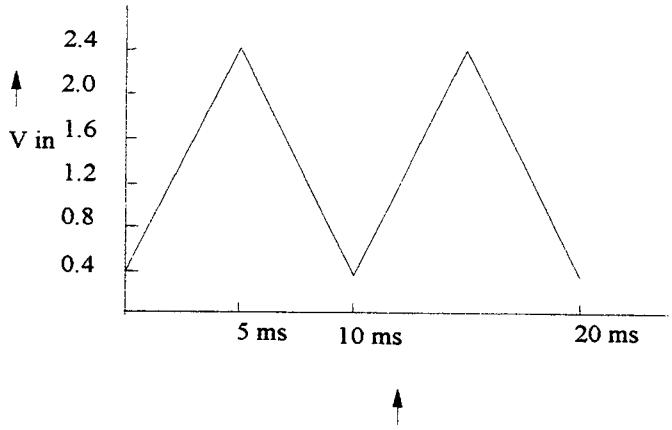

+5 V
5.78KΩ
50 pF
$\overline{A1}$
$\overline{A1}$
Q1
1
$\overline{A2}$
74121
B
B
+5 V
10 KΩ
30 pF
$\overline{A1}$
$\overline{A1}$
Q1
B
B
74123
1
RD
Time μ S
0
0.5
1.0
1.5
2.0
$\overline{A1}$
B

Rajah 5

...11/-



(a)



Rajah 6

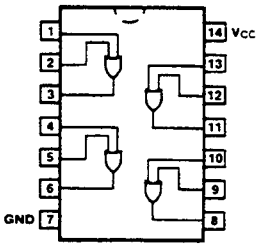
... 12/-

APPENDIX B

54/7432
54S/74S32
54LS/74LS32

QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3 for U.L. definitions

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		22		32		6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			38		68		9.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay	15		2.0	7.0		15	ns	Figs. 3-1, 3-5	
t_{PHL}		22		2.0	7.0		15			

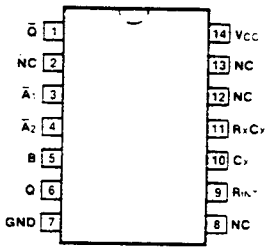
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

...13/-

54/74121

MONOSTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A



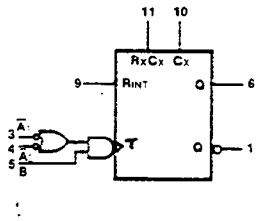
DESCRIPTION — The '121 features positive and negative dc level triggering inputs and complementary outputs. Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers.

When triggering occurs, internal feedback latches the circuit, prevents re-triggering while the output pulse is in progress and increases immunity to negative-going noise. Noise immunity is typically 1.2 V at the inputs and 1.5 V on V_{CC}.

Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application. A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent. Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor. Duty cycles beyond this range tend to reduce the output pulse width. Otherwise, output pulse width follows the relationship:

$$t_w = 0.69\ R_x C_x$$

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1$, $\bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2.0/2.0
Q, $\bar{Q}$	Outputs	20/10

...14/-

MOTOROLA

SN54/74LS122
SN54/74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

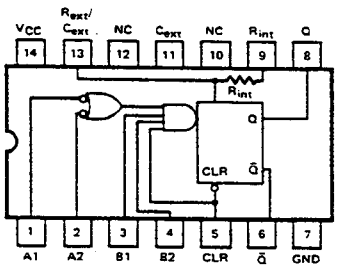
LOW POWER SCHOTTKY

DESCRIPTION — These d-c triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

The LS122 and LS123 have Schmitt trigger inputs to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

- OVERRIDING CLEAR TERMINATES OUTPUT PULSE
- COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS
- D-C TRIGGERED FROM ACTIVE-HIGH OR ACTIVE-LOW GATED LOGIC INPUTS
- RETRIGGERABLE FOR VERY LONG OUTPUT PULSES, UP TO 100% DUTY CYCLE
- INTERNAL TIMING RESISTORS ON LS122

SN54LS/74LS122
(TOP VIEW) (SEE NOTES 1 THRU 4)



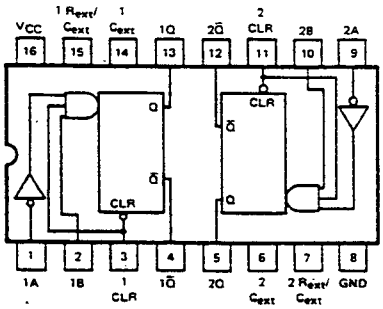
J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NC — NO internal connection

LS122
FUNCTIONAL TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⊔
H	L	X	H	↑	⎍	⊔
H	X	L	↑	H	⎍	⊔
H	X	L	H	↑	⎍	⊔
H	H	↑	H	H	⎍	⊔
H	↓	↓	H	H	⎍	⊔
H	↓	H	H	H	⎍	⊔
↑	L	X	H	H	⎍	⊔
↑	X	L	H	H	⎍	⊔

SN54LS/74LS123
(TOP VIEW) (SEE NOTES 1 THRU 4)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

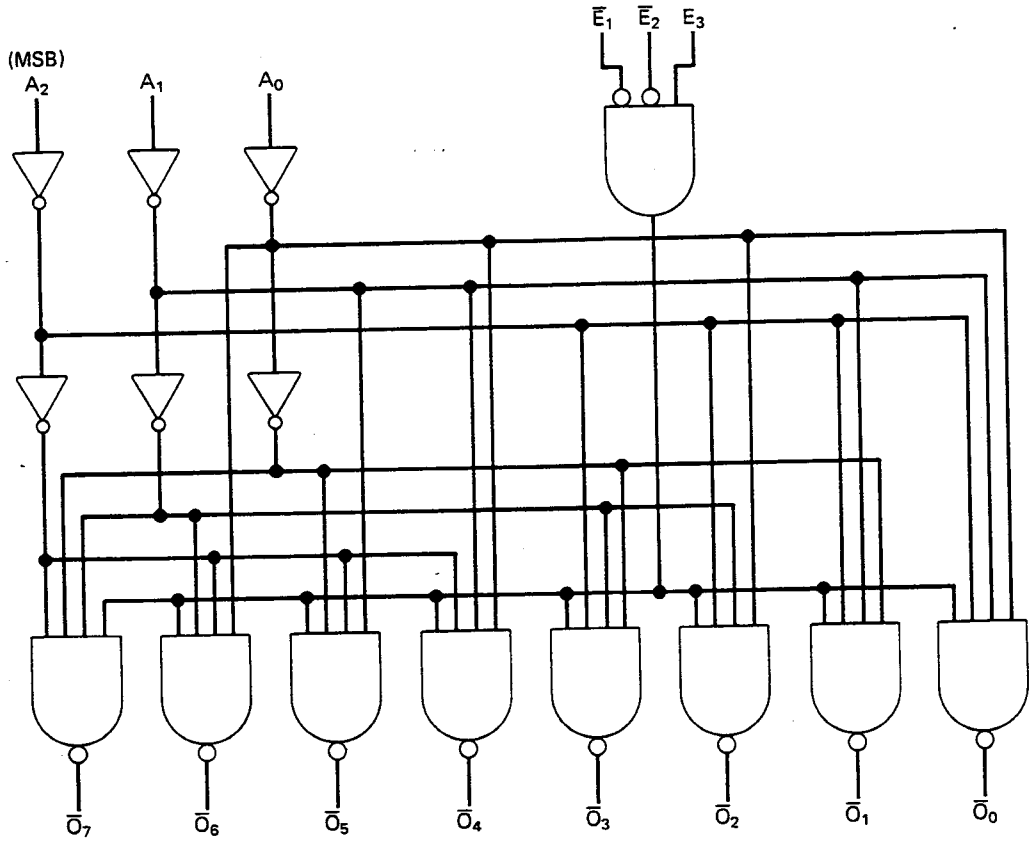
LS123
FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

NOTES:

1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of the LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int}/C_{ext} and V_{CC}.

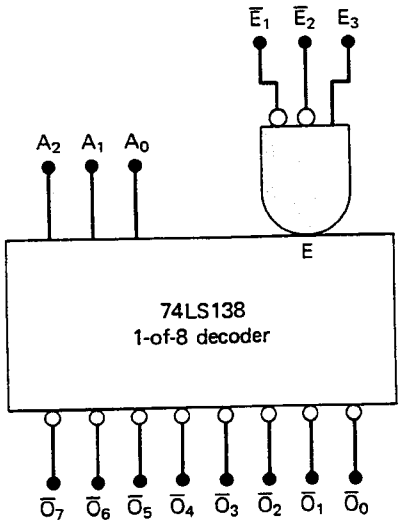
5



(a)

$\overline{E}_1$	$\overline{E}_2$	E_3	Outputs
0	0	1	Respond to input code $A_2A_1A_0$
1	X	X	Disabled – all HIGH
X	1	X	Disabled – all HIGH
X	X	0	Disabled – all HIGH

(b)



(c)

FIGURE 9-3 (a) Logic diagram for 74LS138 decoder; (b) truth table; (c) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

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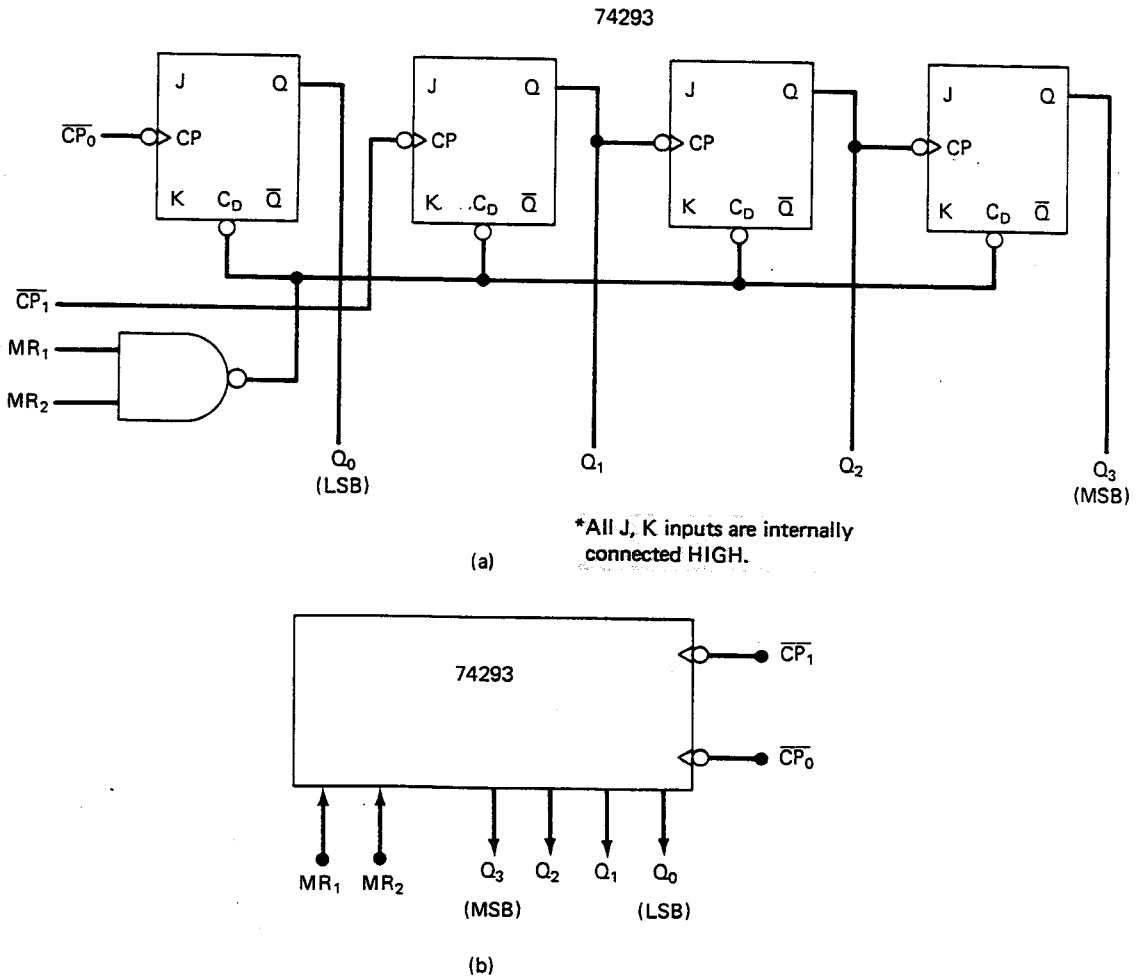

FIGURE 7-7 (a) Logic diagram for 7493 and 74293 asynchronous counter IC; (b) simplified symbol.
(Courtesy of Fairchild, a Schlumberger company)

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