UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 1997/98

September/Oktober 1997

IQK 211/3 - SISTEM DIGIT

[Masa: 3 jam]

Sila pastikan bahawa kertas soalan ini mengandungi **TUJUHBELAS (17)** mukasurat yang bercetak termasuk lampiran sebelum anda memulakan peperiksaan ini.

Sila Jawab **LIMA (5)** soalan. Soalan mesti dijawab di dalam Bahasa Malaysia.

Semua kertas Data *(Data Sheet)* disediakan di dalam Lampiran.

1. (a) Kurangkan persamaan Boolean yang berikut dengan menggunakan teorem Boolean dan syarat-syarat De Morgan.

(a) Minimize the following Boolean equation using Boolean theorems and De Morgan's laws.

$$Y = A(C\overline{D} + \overline{C}\,\overline{D}) + A\overline{B}D + \overline{A}\,\overline{B}C\overline{D}$$

(35 markah)

(b) Paparan tujuh ruas digunakan untuk memaparkan angka perpuluhan (Rajah 1). Setiap ruas dikawal secara berasingan dan apabila kesemua ruas 'on' angka 8 dipaparkan. Ruas bawah kiri di on apabila angka-angka 0, 2, 6 dan 8 di paparkan.

(b) Seven segment displays are used to display decimal digits (Figure 1). Each segment is controlled separately, and when all the seven segments are on, the number 8 is displayed. The lower left segment comes on when displaying the numbers 0, 2 ,6, and 8.

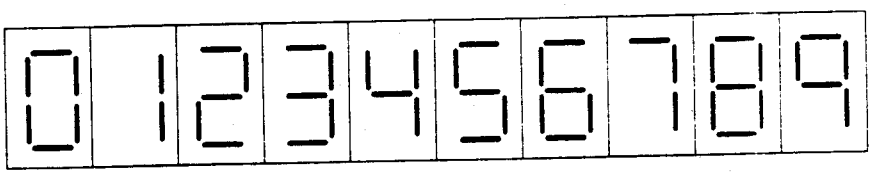
(i) Rekabentuk sebuah litar yang mengeluarkan HIGH (1) apabila sebuah kod BCD 4-bit diterjemahkan kepada suatu nombor yang menggunakan ruas bawah kiri.

(i) Design a circuit that outputs a HIGH (1) whenever a 4-bit BCD code translates to a number that uses the lower light segment.

(ii) Lakarkan litar anda dengan menggunakan get-get NAND berinput 2.

(ii) Draw your circuit using 2 input NAND gates.

(65 markah)



Rajah 1

2. (a) Apakah input-input taksegerak sebuah flip-flop JK? Bagaimanakah input-input ini memberi kesan terhadap output? Sila beri satu penggunaan input-input taksegerak ini.

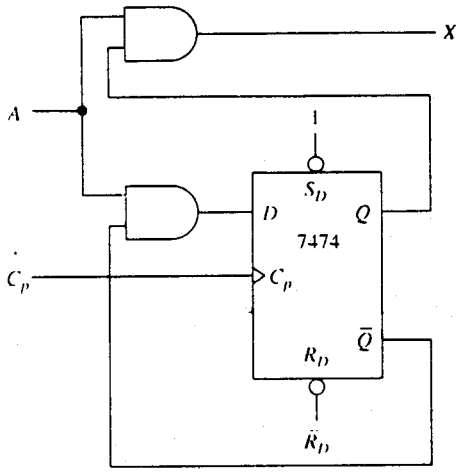
(a) What are the asynchronous inputs of a JK flip-flop? How do they effect the output? Give an application of these asynchronous inputs.

(40 markah)

(b) Litar di Rajah 2 menunjukkan sebuah flip-flop *D* dipicu tepi positif. Bentuk gelombang - betuk gelombang diberi pada *A* dan C_P. Lakarkan bentuk gelombang - bentuk gelombang pada *D*, *Q*, $\overline{Q}$ dan *X*.

(b) The circuit in Figure 2 shows a positive edge-triggered D flip-flop. The waveforms shown are applied to the inputs at A and C_P. Sketch the resultant waveforms at D, Q, $\overline{Q}$ and X.

(60 markah)



Rajah 2

3. (a) Secara ringkas, jelaskan yang berikut dengan bantuan bentuk gelombang-bentuk gelombang yang sesuai.

(i) Pemultigetar dwistabil

(ii) Pemultigetar monostabil

(iii) Pemultigetar astabil

(a) *Explain briefly the following with the help of relevant waveforms.*

(i) Bistable Multivibrator

(ii) Monostable multivibrator

(iii) Astable multivibrator

(40markah)

(b) Degan menggunakan IC 74121, rekabentuk sebuah litar untuk menukar 50 Khz, 80% kitar tugas bentuk gelombang empat segi kepada 50 Khz, 50% kitar tugas bentuk gelombang empat segi.

(b) Design a circuit using a 74121 to convert a 50 -Khz, 80% duty cycle square wave to a 50 Khz 50% duty cycle square wave.

(60markah)

4. (a) Secara ringkas, jelaskan fungsi litar dalam Rajah (3).

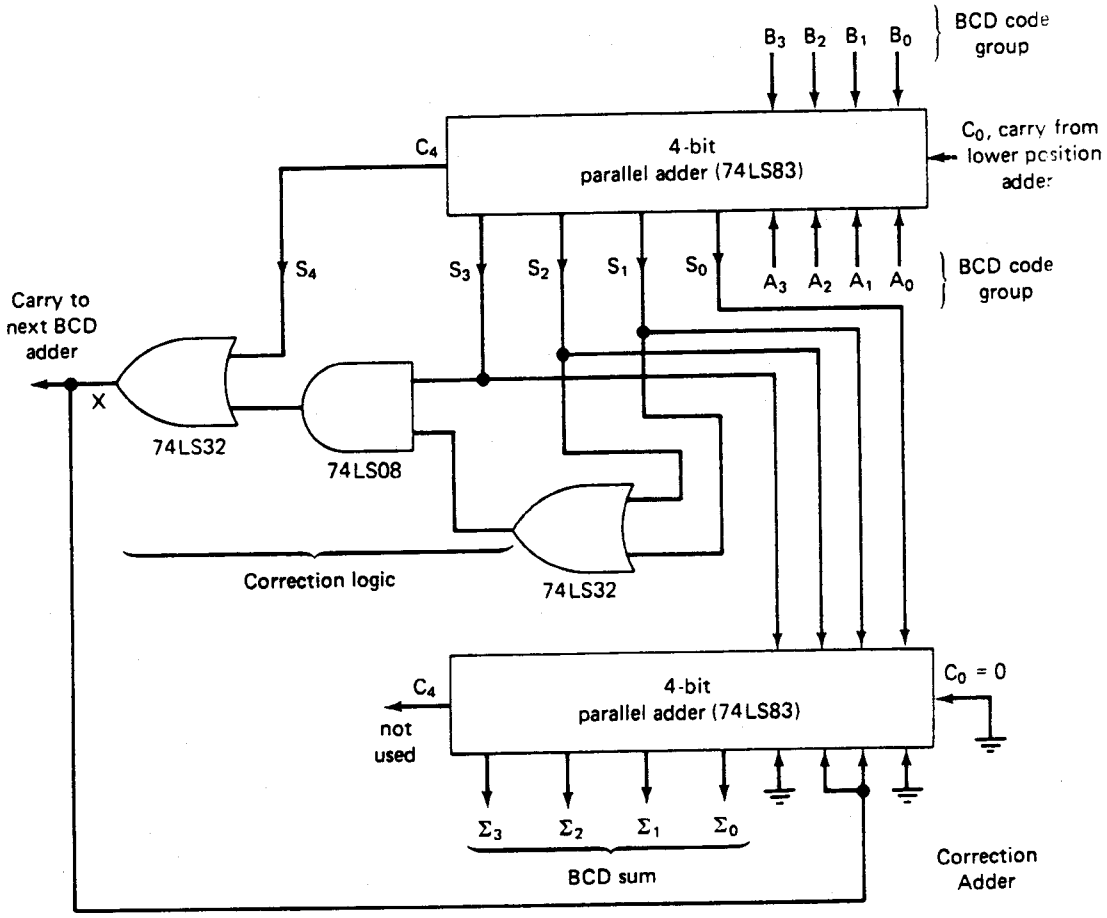
(a) Briefly explain the function of the circuit in Figure 3.

(40 markah)

(b) Dalam Rajah (3), anggap input-input yang berikut pada [A] = 0101, [B] = 1001, $C_0 = 0$. Apakah paras-paras logic pada [S], X, [Σ] dan CARRY.

(b) Assume the following inputs in Figure 3: [A] = 0101, [B] = 1001, $C_0 = 0$. Determine the logic levels at [S], X, [Σ] and CARRY.

(20 markah)

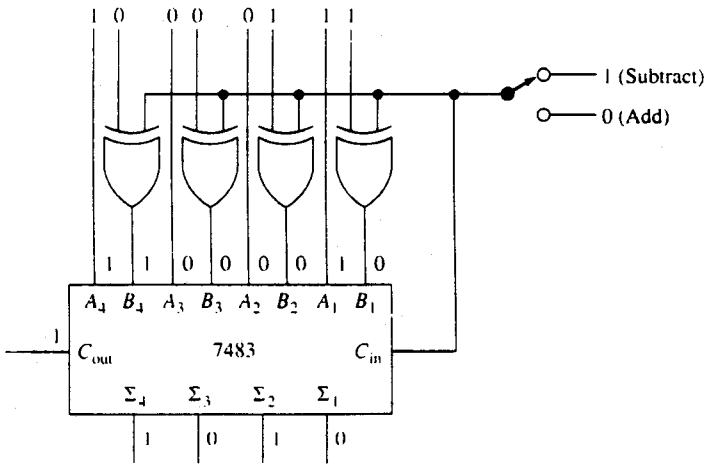

B3 B2 B1 B0
BCD code group
C4
4-bit parallel adder (74LS83)
C0, carry from lower position adder
S4
S3 S2 S1 S0
A3 A2 A1 A0
BCD code group
Carry to next BCD adder
X
74LS32
74LS08
Correction logic
74LS32
C4
not used
4-bit parallel adder (74LS83)
C0 = 0
Σ3 Σ2 Σ1 Σ0
BCD sum
Correction Adder

Rajah 3

(c) Rajah (4) menunjukkan sebuah "4-bit 2's complement adder/subtractor". Litar ini cuba menolak 9 - 3 (1001 - 0011) tetapi mendapat jawapan 10 (1010) iaitu suatu jawapan yang salah. Keadaan logik yang direkod pada nod-nod yang tertentu adalah seperti yang ditunjukkan di rajah. Kenalpasti bahagian-bahagian rosak di litar ini.

(c) *Shown in Figure (4) is a 4-bit 2's complement adder/subtractor. This circuit is attempting to subtract 9 - 3 (1001 - 0011) but keep getting the wrong answer of 10 (1010). Each test node is labeled with the logic state observed using a logic probe. Find the faulty parts in the circuit.*

(40 markah)



Rajah 4

5. (a) Spesifikasi-spesifikasi IC yang manakah digunakan untuk mengenalpasti jumlah get sebuah keluarga logik yang dapat di dorong oleh output daripada get logic daripada keluarga logik yang berlainan?

(a) What IC specifications are used to determine how many gates of one family can be driven from the output of a logic gate of another family?

(50 markah)

(b) Sebuah songsang 74HCT04 perlu digunakan untuk mendorong get-get yang berikut: 7400 (NAND), 7402 (NOR), 74LS08 (AND), dan 74AL32 (OR). Lakarkan litar dan label voltan dan arus keadaan terburuk pada setiap input dan output. Adakah serasian voltan dan arus yang penuh dalam litar ini? (Sila rujuk kepada Jadual 1 di Appendix untuk data-data yang berkaitan.)

(b) *One 74HCT04 inverter is to be used to drive one input to each of the following gates: 7400 (NAND), 7402 (NOR), 74LS08 (AND), and 74AL32 (OR). Draw the circuit and label input and output worst-case voltages and currents. Will there be total voltage and current compatibility? (Please refer to Table 1 in Appendix for relevant data.)*

(50 markah)

6. (a) Secara ringkas jelaskan dan bandingkan yang berikut:

(i) Pembilang taksegerak

(ii) pembilang segerak

(a) Briefly explain and compare the following:

(i) Asynchronous counters

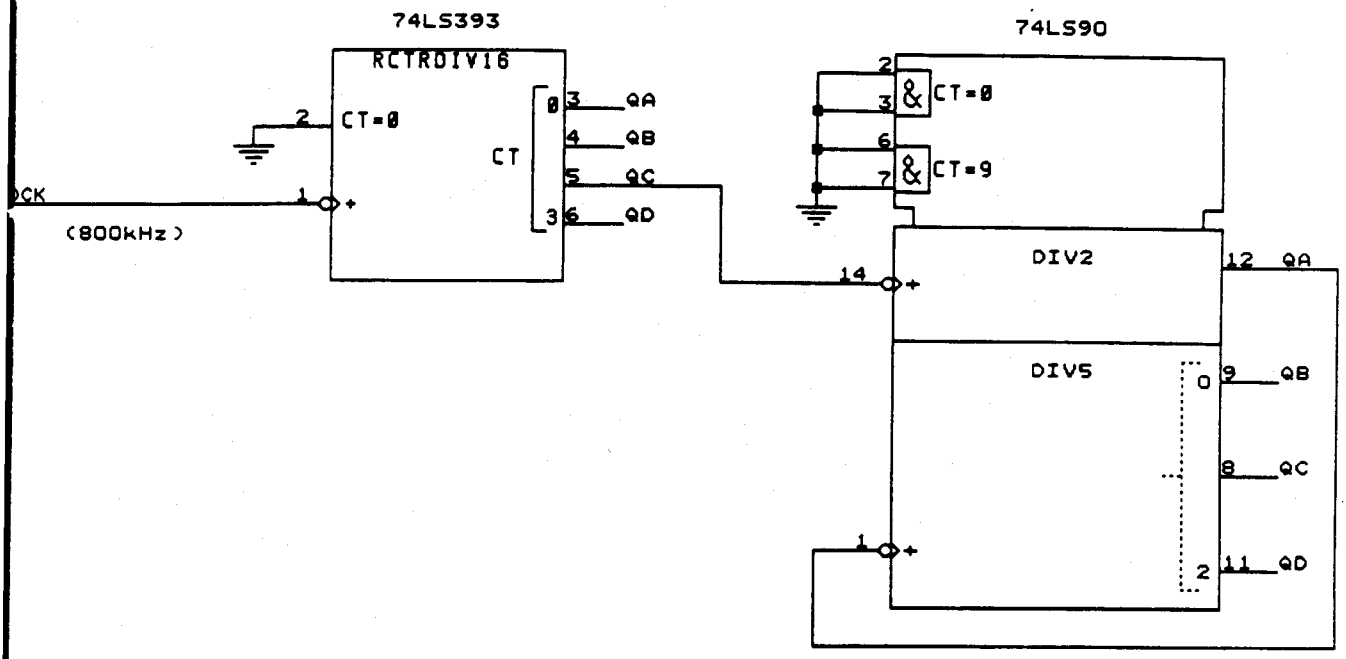
(ii) Synchronous counters

(50 markah)

(b) Jelaskan operasi litar dalam Rajah (5). Lakarkan bentuk gelombang pada Q_B di 74LS393 dan Q_C di 74LS90. Tentukan kitar tugas output pada Q_C di 7490.

(b) Explain the operation of the circuit shown in Figure (5). Sketch the following waveforms: Q_B of 74LS393 and Q_C of 74LS90. Determine the duty cycle of the ouput at the Q_C of the 7490.

(50 markah)



Rajah 5

oooooOOOOOooooo

54/74121

MONOSTABLE MULTIVIBRATOR

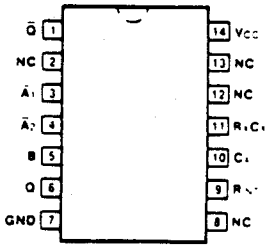
DESCRIPTION — The '121 features positive and negative dc level triggering inputs and complementary outputs. Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers.

When triggering occurs, internal feedback latches the circuit, prevents re-triggering while the output pulse is in progress and increases immunity to negative-going noise. Noise immunity is typically 1.2 V at the inputs and 1.5 V on V_{CC}.

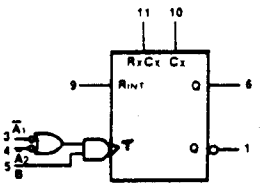
Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application. A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent. Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor. Duty cycles beyond this range tend to reduce the output pulse width. Otherwise, output pulse width follows the relationship:

$$t_w = 0.69\ R_x C_x$$

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1$, $\bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2.0/2.0
Q, $\bar{Q}$	Outputs	20/10

JADUAL I

Worst-Case Values for Interfacing Considerations[a]

Parameter	4000B CMOS	74HCMOS	74HCTMOS	74TTL	74LSTTL	74ALSTTL
V_{IH} (min.) (V)	3.33	3.5	2.0	2.0	2.0	2.0
V_{IL} (max.) (V)	1.67	1.0	0.8	0.8	0.8	0.8
V_{OH} (min.) (V)	4.95	4.9	4.9	2.4	2.7	2.7
V_{OL} (max.) (V)	0.05	0.1	0.1	0.4	0.4	0.4
I_{IH} (max.) (μA)	1	1	1	40	20	20
I_{IL} (max.) (μA)	−1	−1	−1	−1600	−400	−100
I_{OH} (max.) (mA)	−0.51	−4	−4	−0.4	−0.4	−0.4
I_{OL} (max.) (mA)	0.51	4	4	16	8	4

[a]All values are for $V_{supply} = 5.0$ V.

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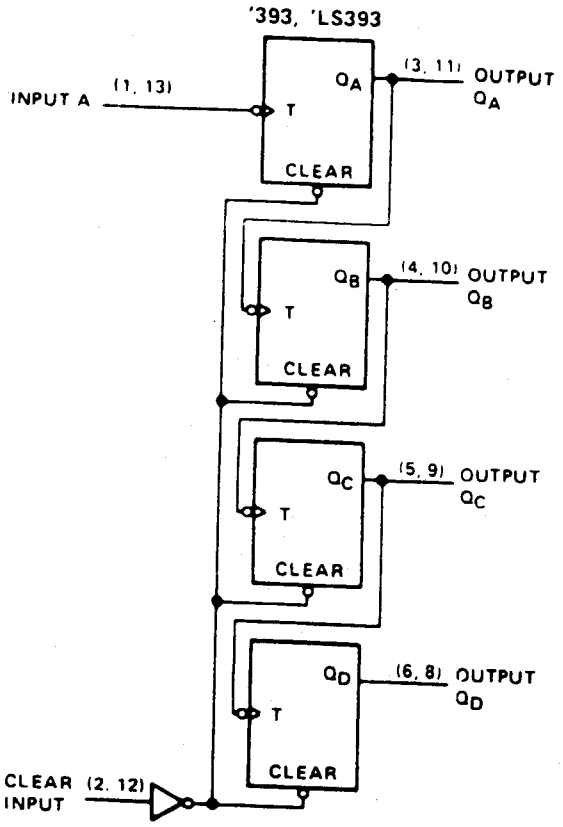
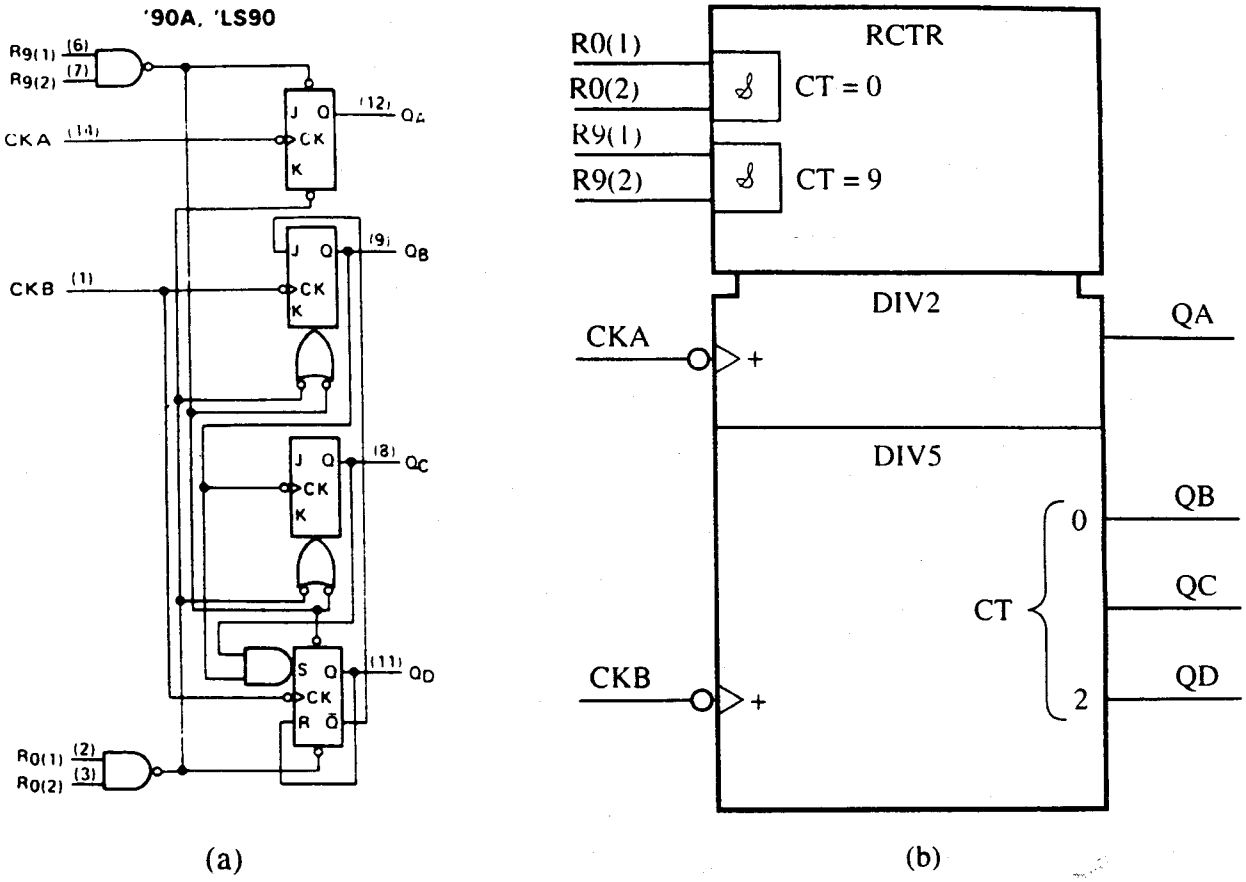
74LS393



One of the two counters in the 74LS393 package. Note that each flip-flop's output is used as the clock input (T) to the next flip-flop in line. (Reprinted by permission of Texas Instruments.)

74LS90



(a) Logic diagram and (b) IEC symbol for the 74LS90 decade counter. (Reprint by permission of Texas Instruments.)