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Investigation of Charge Conduction Mechanisms in Dielectric based on Wide-Bandgap Semiconductor

by

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INVESTIGATION OF CHARGE CONDUCTION MECHANISMS IN DIELECTRIC BASED ON WIDE-BANDGAP SEMICONDUCTOR

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by

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ABSTRACT

Results of the work have been presented in three major parts in this report: (1) effects of thermal nitrided gate-oxide thickness and post grown annealing on 4H SiC-based metal-oxide-semiconductor characteristics, (2) MOS characteristics of diluted N_2O grown SiO_2 gate on 4H-SiC, and (3) MOS characteristics of sol-gel derived SiO_2 gate on GaN. The investigated MOS characteristics covered the physical, chemical, and electrical properties of the gate oxides and much attention has been given to charge-conduction mechanisms through the investigated oxides.

The effects of thermal nitrided gate-oxide thickness on n-type 4H silicon carbide-based metal-oxide-semiconductor characteristics have been reported. Seven different thicknesses of oxide (t_{ox}), ranging from 2 to 20 nm, have been investigated. It has shown that effective oxide charge (Q_{eff}) and total interface-trap density (N_{it}) have demonstrated a cyclic trend as t_{ox} is increased. These observations have been explained in this report. Correlations of Q_{eff} and N_{it} with oxide breakdown field and current transport mechanism in these oxides have also been established and explained. The seven different thicknesses (2 – 20 nm) of nitrided SiO_2 on n-type 4H-SiC have been employed to investigate the charge conduction mechanism through these oxides. Several potential mechanisms have been identified. The mechanisms are depending on electric field and oxide thickness. A relationship plot among these three parameters has been established. Nitrided SiO_2 has been thermally grown on n-type 4H SiC substrate. The effects of post deposition annealing temperature (650 to 950 °C) in vacuum on physical properties of the oxides have been reported. Based on Fourier transform infra-red analysis, Si-O-Si bonding of the oxide has been weakened as the annealing temperature has been increased. The increment in annealing temperature has caused the

have been reported.

In this report, we have also reported the electrical and physical characteristics of MOS device fabricated using GaN film grown on sapphire, with spin-on-glass SiO_2 as the gate oxide. The electrical characteristics of the MOS device were characterized via C-V and I-V measurements. On the other hand, the morphology and compositions of the oxide were studied using FESEM, EDX, and fluorescent x-ray.

temperatures due to increase of power density. This self-heating phenomenon in compact Si devices degrades transistor gain and efficiency. Therefore, the devices are designed to be less compact to reduce heating effects [4].

Silicon carbide (SiC) and gallium nitride (GaN) are considered as the third generation semiconductor, after silicon (as the 1st generation), gallium arsenide and indium phosphide (as the 2nd generation) [5]. These wide-bandgap semiconductors are emerging as the potential and promising semiconductor materials that can revolutionize both the optoelectronic and electronic devices due to their superb intrinsic properties, such as high critical breakdown field, low intrinsic carrier density, and high melting point compared with their conventional silicon (Si) counterpart [6]. Therefore, these materials and its combinations can be used for high temperature, high power, high frequency electronic and optoelectronic devices as well as for non-volatile memory [7]–[11]. In order to utilize these wide-bandgap semiconductors for the above-mentioned usage, their surface must be well passivated electronically by a dielectric layer.

However, the role that carbon in SiC plays during oxide growth has been a major obstacle to the formation of a high quality oxide on SiC [12]. There are a few ways to oxidize SiC but thermal oxidation in a wet or dry atmosphere has resulted in residual carbon in the oxide layer and carbon clusters at the oxide-SiC interface. Nevertheless, it has been found that oxidation or post oxidation annealing in a nitrogen-containing atmosphere has two beneficial effects, which are enhanced removal of carbon and passivation of silicon dangling bonds [12]. Direct growth of oxide in nitrous oxide (N_2O) has proven to be effective because N_2O breaks down into oxygen (O_2), nitrogen (N_2) and nitric oxide (NO) at the oxidation temperature, especially at

dielectric [18]–[21]. This unintentional current conduction in dielectric contributes to current leakage in semiconductor and electronic devices which may deplete the function of these devices [22].

Thermally growth nitrided SiO_2 and low pressure chemical vapor deposited SiO_2 on SiC and GaN, respectively are among the best dielectrics–semiconductor system that have been reported so far [23]–[25]. Unlike Si–SiO_2 system, the mechanisms of current conduction in SiC– and GaN–SiO_2 systems are not extensively investigated and understood. It is believed that the current transport mechanisms would be difference between narrow-bandgap semiconductor (Si) and wide-bandgap semiconductor. In Si–SiO_2 system, the current conduction mechanisms have been systematically and extensively investigated, explained, predicated, and modeled. In general, current conducts in 7 different mechanisms in that system, namely Fowler-Nordheim (FN) tunneling, Schottky effect, field ionization of trapped electrons, hopping of thermally excited electrons, trap-assisted tunneling, shallow-trap-assisted tunneling, and band-to-band tunneling, depending on the magnitude of applied electric field, the oxide composition, processing, and thickness [18]–[20]. However, in SiC–SiO_2 system, only three mechanisms, i.e. FN tunneling, electron facilitated by FN tunneling, and interface-trap assisted FN tunneling, have been reported and among that the later two mechanisms have been discovered and reported recently [21]. To our knowledge, there has been limited report on current-conduction study in GaN–SiO_2 system up to date. Therefore, by discovering the fundamentals of current transport from these wide-bandgap semiconductors through dielectric; it would enable a better understanding of charge (electron and/or hole) transport in a dielectric based on reliable physical or mathematical models.

1.2 Research Objectives

The objectives of this research are:

1. To discover all of the possible current conduction mechanisms in SiO_2 deposited/grown on SiC or Ga.
2. To explore the effects of oxide thickness and rapid thermal annealing ambient conditions on current conduction mechanisms.
3. To establish reliable and novel mathematical or physical models representing the current conduction mechanisms in SiC–SiO_2 or GaN–SiO_2 systems.

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CHAPTER 2

LITERATURE REVIEW

2.1 SILICON CARBIDE (SiC)

2.1.1 Introduction

Silicon carbide (SiC) was first used as an abrasive and cutting material. The first SiC light-emitting-diode (LED) was already produced in 1907. For the past sixteen years, there has been a significant interest in the development of microelectronic devices for blue and UV emission, solar blind UV detection, high power, high temperature, high frequency and radiation hard applications, and sensors that are able to operate in harsh environments. The need for such devices has led to considerable research and development efforts in wide bandgap semiconductor materials, especially SiC and gallium nitride (GaN) [1].

2.1.2 Advantages of Silicon Carbide

The commercial availability of semi-insulating SiC wafer with high thermal conductivity has enabled the development of SiC as the third generation semiconductor material. Due to its wide bandgap, the potential advantages of SiC include higher junction temperatures and narrower drift regions (due to a high critical electrical breakdown field value ten times higher than Si) that can result is much lower device on-resistance than is possible in Si [1]. In other words, SiC is a well-suited semiconductor material for high-temperature circuit operation from 350 °C to 500 °C. It is desired for use in aerospace applications (turbine engines and the more electric aircraft initiative), nuclear power instrumentation, satellites, space exploration and

silicon. However, there is an exception that the processing temperatures of SiC are generally higher [3].

Table 2.1: Comparison of the properties for selected important semiconductors at 300 K [4], [5].

ELECTRICAL & PHYSICAL PROPERTY	Si	GaAs	SiC		
			4H	6H	3C
Bandgap (eV)	1.12	1.42	3.26	3.02	2.39
Relative dielectric constant	11.9	13.1	9.7	9.7	9.7
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.8×10^{6}	$\sim10^{-7}$	$\sim10^{-5}$	$\sim10^{-1}$
Breakdown field (MV/cm) @ $N_D = 10^{17}$ cm^{-3}	0.6	0.6	3.0	3.2	>1.5
Saturated electron velocity (10^7cm/s)	1.0	1.2	2.0	2.0	2.5
Electron mobility (cm^2/V-s) @ $N_D = 10^{16}$ cm^{-3}	1200	6500	800^A 800^B	60^A 400^B	750^A
Hole mobility (cm^2/V-s) @ $N_A = 10^{16}$ cm^{-3}	420	320	115	90	40
Thermal conductivity (W/cm-K)	1.5	0.5	3 - 5	3 - 5	3 – 5
Melting Point (K)	1690	1510	~3100	~3100	~3100
TECHNOLOGICAL PROPERTY					
Native oxide	Yes	No		Yes	
Complementary device	Yes	No		Possible	

^{A}: parallel to c-axis

^{B}: perpendicular to c-axis

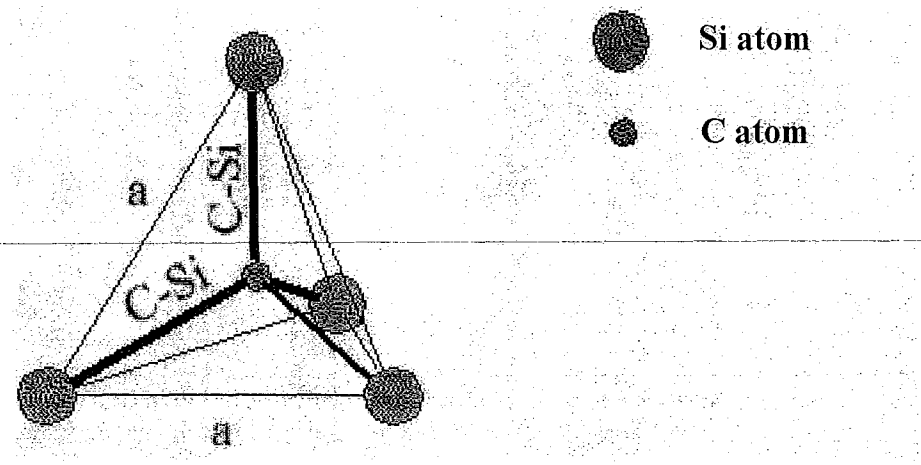


Figure 2.1: The tetragonal bonding of a carbon atom with the four nearest silicon neighbours.

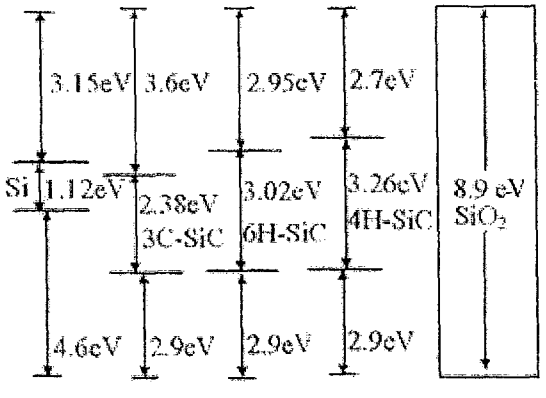
The distance, a, between neighbouring silicon and carbon atoms is approximately 3.08 Å for all polytypes. The position of carbon atom at the center of mass of the tetragonal structure is outlined by the four neighbouring Si atoms so that the distance between the C atoms to each of the Si atoms is the same. The distance between C-Si is approximately equal to 1.98 Å whereas the distance between two silicon planes is around 2.52 Å. On the other hand, the height of a unit cell, c, varies between the different polytypes. Thus, the ratio c/a differs from polytype to polytype, but is always close to the ideal for a closed packed structure. For instance, this ratio is approximately 1.641, 3.271 and 4.908 for 2H, 4H and 6H-SiC polytypes respectively. At the mean time, the equivalent ideal ratios for these polytypes are $(8/3)^{1/2}$, $2(8/3)^{1/2}$ and $3(8/3)^{1/2}$ respectively. The difference between these polytypes is the stacking order between succeeding double layers of carbon and silicon carbons.

Commonly observed polytypes in the sublimation bulk growth is shown in Fig. 2.2.

With large bandgap, high electron saturation drift velocity and mobility, 4H-SiC polytype has gained much attention in recent years for device applications [6]. It consists of an equal number of cubic and hexagonal bonds [2]. On the other hand, 6H-SiC are used in volume production of blue LEDs as substrate material for GaN heteroepitaxy [6]. This polytype is composed of two-thirds cubic bonds and one-third hexagonal bonds. In short, these 6H-SiC and 4H-SiC are the only SiC polytypes currently available in bulk wafer form [2].

2.1.4 Gate Oxides Requirements on SiC

There are two major requirements for the gate dielectric of metal-oxide-semiconductor (MOS) devices that are high barriers for electron and hole injection and good oxide quality. The gate dielectric should have sufficiently high energy barriers to block the charge carriers (holes and electrons) between the channel and the gate of a metal-oxide-semiconductor field effect transistor (MOSFET). In order to prevent thermally stimulated injection, the energy barriers for both electrons and holes in a semiconductor have to be high enough. Figure 2.3 shows the energy band parameters for the interfaces of SiO_2 with Si and four SiC polytypes (Dimitrijev *et al.*, 2004b).



electronics devices [7]-[13]. This is due to their direct and wide band gap energy, which lies between 3.4 and 6.2 eV [7]. GaN is one of the candidates of group III-V, which has attracted much attention due to its wide band gap (3.4 eV), high breakdown electric field (~0.2 - 109 V/m) and high electron saturation velocity (~ 2.7 – 104 cm/s) [14],[15]. In addition, the specific on-state resistance of field-effect transistor (FET) for GaN is expected to be lower than Si or GaAs [14]. These materials have replaced silicon which has dominated high-voltage power electronics applications for quite sometimes [11]. Unlike other III-V compounds, nitride based epitaxial layers exhibit wurtzite crystal structure. This wurtzite crystal structure will result in a much larger piezoelectric field in nitride based heterostructures, as compared to other III-V compounds [15]. This characteristic is essential in obtaining low-loss power-switching devices, such as an inverter. The ability of this material will allow large performance enhancements in a wide variety of applications such as switching of electric power in utility industry grid systems; control of power in the electrical sub-systems of emerging automobile, ship, and aircraft technology; and for power microwave generation [12], [16]. However, green-house effect is generated due to the generation of carbon dioxide from the power generation plants. This is as a result of burning fossil fuels as to generate electricity. To achieve environmental friendly condition, the usage of electricity needs to be reduced by replacing the traditional power device substrates or materials with GaN. These devices help to attain a cleaner environment by reducing energy consumption, decreasing time consumption and generating low sound. Thus, there is an enormous interest in developing GaN high power devices [17].

However, it is rather difficult to find a lattice-matched substrate that allows the growth of GaN on the substrate. The most frequently used substrates are (0001) sapphire and SiC which have about 16 % and 3.5 % lattice mismatch to GaN [18]. Nevertheless, the calculated lattice mismatch between GaN and sapphire is larger than 30 %. There is a large variation (14 %) between the calculated lattice mismatch and the actual mismatch. This is due to the rotation of the small cell of Al atoms. The best films are grown with relatively small in- and out-of plane misorentation on this plane [19]. GaN films grown on sapphire provide a much better advantages compared to SiC. This is due to the GaN films grown on SiC substrates are limited in size [20] because the diameters of SiC substrates are below 4 inches. This limitation can be overcome by introducing sapphire substrates with its availability at large diameters as a substitution

higher dielectric film is demanding to replace the conventional SiO_2, promising equivalent capacitances with reduced leakage and threat of electrical breakdown [29].

2.3 MOS CAPACITOR

2.3.1 Introduction

The industry trend of increasing memory density dictates a trend of increased capacitance density. One of the challenges that the memory chip manufacturers is facing now is that they need to strive for reducing the size of capacitors while ensuring the capacitors and nearby transistors are adequately isolated from each other. Down sizing of the MOS devices brings a lot of improvements in the performance of devices and circuits. Smaller devices can be implemented in a smaller area with fewer materials and will consume less amount of power. As a consequence, this lead to a large decrease in the per-transistor and per-function costs of integrated circuits. When the device becomes smaller, the carrier transport distance from the source to drain will be reduced accordingly. Nevertheless, the capacitances associated with the devices as well as the interconnections will also be reduced. These effects result in the higher operation speed of smaller-size devices. Moreover, more components per chip are feasible with smaller devices; hence more powerful functions can be implemented and further enhancement of the system response [30]. Substantial increased density can be achieved by increasing both the area of the capacitor and the dielectric constant (high-k), as well as decreasing the thickness of the insulating film of capacitor.

2.3.2 The MOS Capacitor Structure

The MOS structure consists of a semiconductor substrate with a thin oxide layer and a top metal contact which is also known as the gate. A second metal layer forms an Ohmic contact to the back of the semiconductor, also referred to as the bulk. Figure 2.4

Dielectric layers are just indispensable to integrated circuit fabrication as the semiconductor itself. Silicon dioxide (SiO_2) is one of the most commonly encountered substances in electronic manufacturing. The whole planar electronics processing and the modern integrated circuit (IC) industry has been made possible by the unique properties of silicon dioxide that are:

- Silicon dioxide is the only native oxide of a common semiconductor which is stable in water and at elevated temperatures.
- An excellent electrical insulator.
- A mask to common diffusing species.
- Capable of forming a nearly perfect electrical interface with its substrate.

2.4.2 The Properties of Silicon Dioxide

Silicon dioxide is sufficiently important in the semiconductor field due to its widespread uses. Device engineers call it oxide without ambiguity. As an insulator, silicon dioxide has a band gap of 8.9 eV. Its thermal expansion coefficient is 5×10^{-7} K^{-1}, which is sufficiently close to that of silicon (2.6×10^{-6}) to prevent thermally induced stresses causing crystal defects in the underlying silicon in most circumstances [32]. Table 2.2 summarizes some of the important properties of silicon dioxide at room temperature.

Table 2.2: Important properties of pure silicon dioxide [33].

Structure	**Amorphous**
Melting point	Approximately 1600 °C
Density	2.0 – 2.3 g/cm^3
Refractive index	1.46 (thermal oxide)

chemical properties such as hygroscopicity (tendency to react with ambient water) also vary tremendously depending on the structure [33].

2.4.4 The Importance of Silicon Dioxide Film

Since silicon dioxide is a good insulator, it is used to provide electrical isolation between devices on the chip. Moreover, the thin oxide film can form the dielectric layer of a capacitor. For this particular application, where the resistive character of the dielectric is essential, the chemical purity of the oxide film determines its effectiveness [34].

Besides, one of the most common uses of silicon dioxide is as a doping mask, or barrier, against dopant diffusion into semiconductor substrate. Through the methods of photolithography, certain regions of an oxide film are protected against etching. The openings ("window") subsequently etched in the oxide permit the entrance of dopants into the substrate. Oxide which is unetched retards the diffusion of dopant atoms; hence the dopants are segregated precisely into the desired region of the substrate [34].

As a glass-like material, silicon dioxide is resistive to intrusion of moisture and most ambient or environmental chemicals encountered in the neighborhood of electronic devices. For this reason, an encapsulating film of silicon dioxide is often used to provide a protective covering over the completed device [34].

Lastly, silicon dioxide also plays an important role as an electronic surface passivation. It is noted that oxidation of a crystalline silicon surface produces an important alteration of the electronic state of that interface. The surface of a bare silicon

oxidation therefore serves primarily as an accelerator of the oxidation process, resulting in thicker oxide layers per unit of time. Depending on which oxidant species is used (O_2 or H_2O), the thermal oxidation of SiO_2 may either be in the form of dry oxidation (wherein the oxidant is O_2) or wet oxidation (wherein the oxidant is H_2O) [35].

The basic thermal oxidation setup is shown in Fig. 2.8.

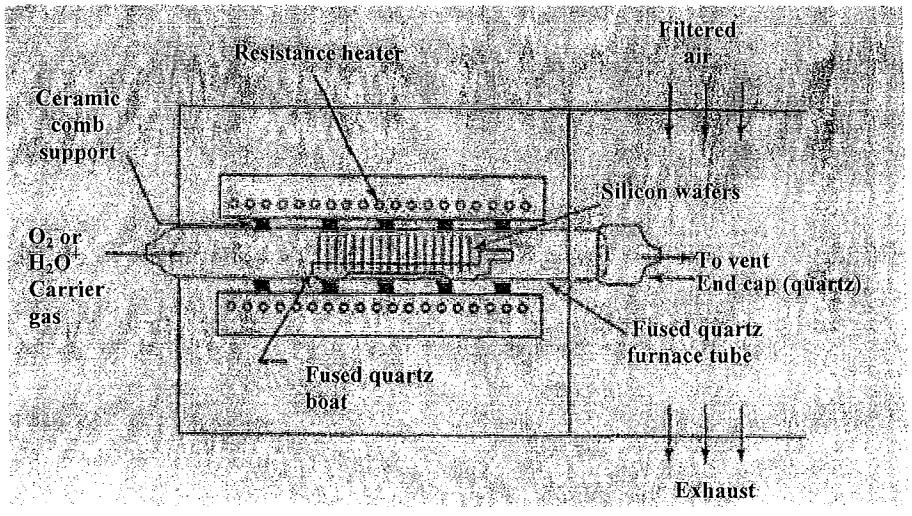


Figure 2.8: Schematic cross section of a resistance-heated oxidation furnace [35].

The reactor consists of a resistance-heated furnace, a cylindrical fused-quartz tube containing the wafers held vertically is a slotted quartz boat and a source of either pure dry oxygen or pure water vapor. The loading end of the furnace protudes into a vertical flow hood where a filtered flow of air is maintained. Flow is directed as shown by the arrow in Fig. 2.8. The hood reduces dust and particulate matters in the air surrounding the wafers and minimizes contamination during wafer loading. Generally, the oxidation temperature is in the range of 900 °C – 1200 °C and the typical gas flow rate is about 1 liter/min. This oxidation system uses microprocessors to regulate the gas flow sequence, to control the automatic insertion and removal of wafers, to ramp the temperature up (i.e., to increase the furnace temperature linearly) from low temperature

oxidation or post oxidation in a nitrogen-containing atmosphere has two beneficial effects that are enhanced removal of carbon and passivation of silicon dangling bond [37]. Other effects of nitridation include reductions in SiC-SiO_2 interface and in near interface-trap densities, increments in effective SiC-SiO_2 barrier height and in metal-oxide-semiconductor (MOS) field-effect-transistor's carrier mobility and improvements in oxide reliability and in non-equilibrium charge-retention time [38].

2.6.2 Effects of Nitrogen at the SiO_2-SiC Interface

There are two sets of mechanism involved at the SiO_2-SiC interface during nitridation:

- Creation of strong Si≡N bonds that passivate interface traps due to dangling and strained bonds.
- Removal of carbon and the associated complex silicon-oxycarbon bonds.

The mechanisms leading to the creation of strong Si≡N bonds are completely analogous to the case of the SiO_2-Si interface. In the case of both the SiO_2-Si and the SiO_2-SiC interfaces, there are dangling Si bonds that are passivated by N, and strained Si-O bonds that are replaced by strong Si≡N bonds during the nitridation. In both cases, the creation of these bonds improves the reliability of the oxide gate [3].

However, there is an important difference between these two cases. In the case of SiC, not only the reliability is improved by the strong Si≡N bonds but also the initial interface-trap density is significantly reduces. This interface-trap reduction is analogous to the well-established interface-trap reduction in Si due to creation of Si-H bonds (interface passivation). This hydrogen-based passivation is not effective on the case of

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Table 2.3: Historical comparison of various nitridation techniques and their effects on electrical properties [37].

Process	Effect on oxide quality
Annealing in N_2O	Deterioration of electrical properties
Annealing in NO (thin oxides, no epi layer)	Improvements in electrical properties
Direct growth in N_2O	Improvement in electrical properties
Direct growth in NO	Shown as the best process in terms of interfacial properties and oxide reliability
Diluted N_2O	Good oxide reliability; comparable to NO-grown
High-temperature growth in N_2 (> 1200 °C)	Reduce interface states and increase MOSFET electron mobility
Jet vapour deposition (JVD)	Reduced D_{it} in upper half of energy gap. Reduced sub-oxides and dangling bonds at interface
$NO/O_2/NO$ sandwich process	MOSFETs with low field mobility = 48 cm^2/Vs; D_{it} = 3 X 10^{11} $cm^{-2}eV^{-1}$; oxide breakdown = 9 MV/cm
Nitrogen radical treatment	Improved field effect mobility in 4H- and 6H-SiC

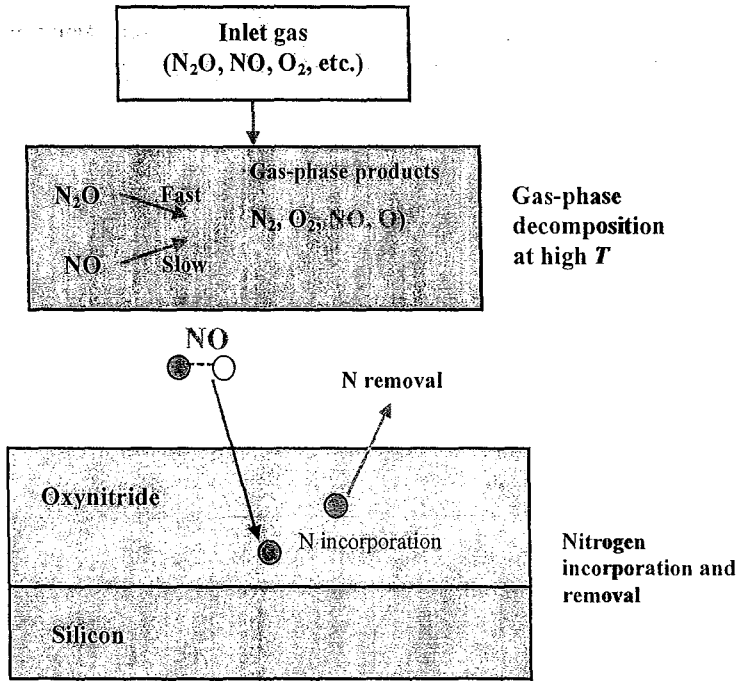

Figure 2.10: Schematic diagram of silicon nitridation in NO or N_2O [39].

The main products of the N_2O decomposition are N_2, O_2 and NO (with the equilibrium concentration of NO increasing with temperature). Since N_2 is much less reactive than O_2 and NO, it can be expected that a properly chosen mixture of NO and O_2 in the gas phase would produce an oxynitride film similar to that grown in N_2O. However, this is not the case. It is observed that oxynitridation in the mixture of NO and O_2 is in fact much more similar to NO oxynitridation than to N_2O oxynitridation. This suggests that there are other species present during N_2O decomposition which are important in the nitridation process. It is believed that atomic oxygen plays a key role in N_2O oxynitridation. Though the equilibrium concentration of oxygen is rather low, an intermediate concentration of atomic oxygen released in the first step of the decomposition process may be relatively high, especially if N_2O decomposition takes

2.6.5 Thermodynamics of the Si-N-O System

The bulk phase diagram of the Si-N-O system is shown in Fig. 2.11. The diagram consists of four phases: Si, SiO_2 (cristobolite, tridymite), Si_3N_4 and Si_2N_2O. The three compound phases have similar structural units: SiO_4 tetrahedra for SiO_2, SiN_4 tetrahedra for Si_3N_4, and slightly distorted SiN_3O tetrahedral for Si_2N_2O, implying that the phases can be converted from SiO_2 to Si_2N_2O and finally Si_3N_4 by replacing oxygen with nitrogen. However, the nitride (Si_3N_4) and the oxide (SiO_2) phases never coexist in the bulk under equilibrium conditions. They are often separated by the oxynitride (Si_2N_2O), which is the only thermodynamically stable and crystalline form of silicon oxynitride.

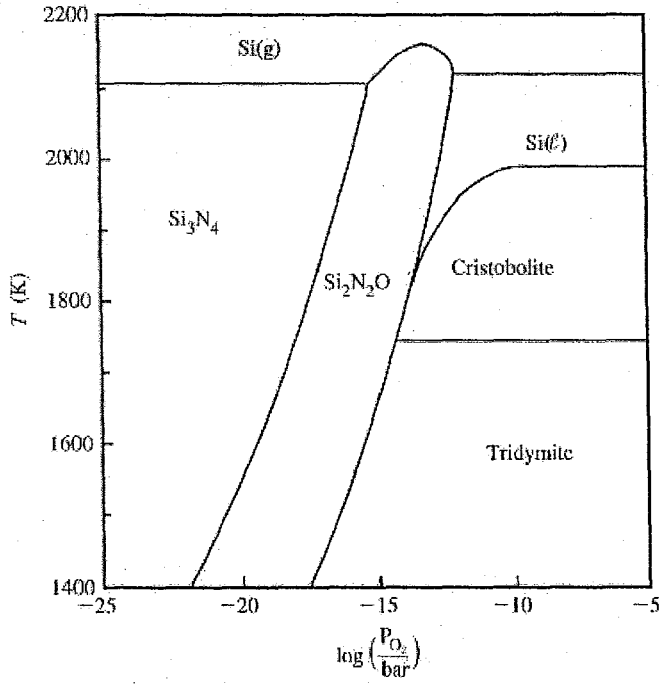

Figure 2.11: Thermodynamic phase diagram of the Si-O-N system [39].

According to thermodynamic equilibrium, nitrogen should not incorporate into SiO_2 film that is grown on silicon in almost any partial pressure of oxygen, i.e. > 10^{-17}

the past and much is known about factors that control coating deposition and final thickness of the deposit that results [40].

2.7.2 Spin-on-coating Physics

Spin coating is divided into four stages: deposition, spin-up, spin-off and evaporation. An excess of liquid is dispensed on the surface during the deposition stage. In the spin-up, stage, the liquid flows radially outward, driven by centrifugal force. In the spin-off stage, excess liquid flows to the perimeter and leaves as droplets. As the film thins, the rate of removal of excess liquid by spin-off slows down, because the thinner the film, the greater the resistance to flow, and because the concentration of the nonvolatile components increases raising the viscosity. In the fourth stage, evaporation takes over as the primary mechanism of thinning [41].

The physics of the substrate rotation leads to a fluid flow condition where the rotational accelerations are exactly balanced by the viscous drag felt within the solution. Meyerhofer [41] considered the fact that solvent evaporation is also occurring simultaneously out of the top surface of the solution. The Meyerhofer treatment is especially instructive because he split the spin coating run into two stages: one controlled predominantly by viscous flow and the second controlled by evaporation. With this approach he was able predict the final coating thickness, h, in terms of several key solution parameters, according to:

$$h = x(e/2(1-x)K)^{1/3} \tag{2.3}$$

where e is the evaporation, K is flow constants and x is the effective solids content of the solution. The evaporation and flow constants are defined, respectively, as:

$$e = C\sqrt{\omega} \tag{2.4}$$

2.8.2 Rapid Thermal Annealing (RTA)

The rapid thermal process (RTP) system is a single-wafer process which favours system for post-implantation annealing, silicide annealing and ultrathin silicon dioxide layer growth [43].

The most common application of RTP is the post-implantation rapid thermal annealing (RTA) process. After ion implantation, the crystal structure of wafer near the surface is heavily damaged by the energetic ion bombardment. It needs a high-temperature process to anneal the damage, to restore the single-crystal structure and activate the dopant [43].

A study on the effects of RTA on nitrided gate oxide grown on 4H-SiC had been reported last year by Cheong *et al.* [44]. It was found that the effects of annealing time (isothermal annealing) and annealing temperature (isochronal annealing) play important roles on the gate oxide quality. After rapid isothermal and isochronal annealings, there had been a significant increase in positive oxide-charge density and in oxide-breakdown time [44].

2.8.3 Post-Deposition Annealing in Vacuum

The purpose of using vacuum as an atmosphere is that it usually connotes space relatively free from matter. There are two outstanding features of a high vacuum atmosphere that are particular interest in vacuum heat treatment. Firstly, vacuum provides an atmosphere of rather low chemical activity, being almost inert because of the relatively low gas constituents. Due to this, the usual reactions that take place (gas-solid heat treatment reactions) such as carburization, decarburization, reduction or

Table 2.4: Thickness characterization techniques [46].

Property	Technique	Comments
Thickness	Stylus	Any film; need sharp step
	Interferometry	Dielectric films
	Ellipsometry	Dielectric films
	X-ray fluorescence spectrometry (XRFS)	Any film; do not need step; layer thickness in composite film
	Resistance change	Measure metallic film growth
	Scanning Electron Microscopy (SEM)	Cross section

In this research, *Filmetrics* F20 Thin-Film Analyzer is used to measure the thickness of the SiO_2 layer. Measured films must be optically smooth and within the thickness range set by the system configuration requirements. Commonly measured films include semiconductor process films such as oxides, nitrides, resists and polysilicon, optical coatings, flat panel display films such as polyimides, resist, and cell gaps finally, the various coatings used in CD and DVD manufacture.

One of the limitations of *Filmetrics* is that it is unable to measure rough films and also metal films. Besides that, as with most measurements, the uncertainty of the measured data increases as the number of simultaneously measured value increases. This is especially true, as changes in thickness (d) and optical constants (n and k) can often affect the measured reflectance spectrum in similar ways. Thus, it is best that as much information about the film structure as possible is provided.

insulating samples. This is because AFM operates by measuring the forces between a probe and the sample. These forces depend on the nature of the sample, the distance between the probe and the sample, the probe geometry and sample surface contamination [47]. Moreover, AFM has several advantages over the scanning electron microscope (SEM). Unlike the electron microscope which provides a two-dimensional projection or a two-dimensional image of a sample, the AFM provides a true three-dimensional surface profile. Additionally, samples viewed by AFM do not require any special treatments (such as metal or carbon coating) that would irreversibly change or damage the sample.

A disadvantage of AFM compared with SEM is the image size. The SEM can image an area on the order of milimetres by milimetres with a depth of field on the order of milimetres. The AFM can only image a maximum height on the order of micrometres and a maximum scanning area of around 150 by 150 μm. Another inconvenience is that at high resolution, the quality of an image is limited by the radius of curvature of the probe tip, and an incorrect choice of tip for the required resolution can lead to image artifacts.

An AFM is able to operate in several modes. One of them is the contact mode. In this mode, the sample topography is measured by scanning the tip, which contacts the surface, across the sample. Even though this mode is frequently used in AFM measurements, samples are typically covered with a thin layer of water or other contaminants. When the probe touches the surface, it is pulled towards the sample by capillary action. This force, when coupled with possible electrostatic forces, will create

that can plague conventional AFM scanning methods [47]. The advantages of this mode are:

- Higher lateral resolution on most samples.
- Lower forces and less damage to soft samples imaged in air.
- Lateral forces are virtually eliminated so there is no scraping.

The disadvantage of tapping mode is:

- Slightly lower scan speed than contact mode AFM.

Table 2.5 shows the definitions of terms and symbols commonly used in AFM measurements.

Table 2.5: Types of Data Analysis

Terms and Symbols	**Definitions**
Profile Mean Height (Ra)	This value represents the roughness curved line when clipping the assessment length L portion from the center direction of the roughness curved line and having the X-axis be the center line in the direction of the cut area and the Y-axis being the horizontal direction (perpendicular to the X-axis)
Surface Mean Height (Ra)	This term represents the three-dimensional expansion of the center line mean roughness Ra so that it is applicable to the measurement surface. The averaged absolute value of the deviation from the standard surface to the indicated surface.
Maximum Peak-to-Valley Height (P-V)	Difference between the maximum and minimum values of Z data within the indicated surface or section profile.

Table 2.5 continues.

Terms and Symbols	Definitions
(Section Roughness Parameter) n Point Mean Height (Rz)	This parameter represents Rz (cross-point mean roughness) expanded to n point (n: even number from 20~30). The value of Rz is expressed with the difference of the average value of the Z data of the peak from the maximum to the n/2-th and the average value of the Z data of the valley from the minimum to the n/2-th when measuring in the Z direction to a section profile from the line which is parallel to an average line and not cross a section profile.
(Surface Roughness Parameter) n Point Mean Height (Rz)	This parameter represents Rz (cross-point mean roughness) expanded to n point (n: even number from 2~30) and ultimately expanded to a three-dimension. The value of Rz is expressed with the difference of the average value of Z data of the peak from the maximum to the n/2-th and the average value of Z data of the valley from the minimum to the n/2-th in the indicated surface.

Table 2.5 continues.

Terms and Symbols	Definitions
Standard Deviation Size (STD DEV Size)	Standard deviation σ of the determined grain size after setting the threshold value for binary processing.
Count	Count of the determined grain after setting the threshold value for binary processing.
Normalized Count	Normalized grain count after converting the regulated area.
Grain Area	The sum of the grain size of the determined grain after setting the threshold value for binary processing.
Ratio of Grain Area	Ratio of grain contained in the indicated surface.
Threshold	This is the standard value of the image data binary processing prior to performing grain analysis. The value is input and set using either Auto Set or Manual.

the mass density of the film along the growth direction and finally, the interfacial structure [48].

One of the advantages of XRR is that it gives a non-destructive feature. This makes it a very suitable tool to probe interfacial structure since any destructive techniques, such as a cross-sectional transmission electron microscopy or depth profiling, will inevitably change the interfacial state to some extent. Moreover, XRR is particularly sensitive to the film electron density distribution normal to the surface. If the stoichiometry is known, the material density profile can also be found [49].

2.10 ELECTRICAL CHARACTERIZATION

2.10.1 Dielectric Constant of Dielectric (*C-V* Curve)

The term dielectric constant (ε) is more precisely referred to the relative permittivity of an insulator and it is one of the most important characteristics. In applications in which minimizing signal delay and cross talk is of paramount importance, such as in interconnections, ε should be as low as possible. However, there are other applications for which charge storage is important, ε should be as high as possible [46].

The value of ε, at different frequencies and temperatures, is determined from capacitance-voltage (*C-V*) measurements using parallel plate capacitor:

$$C = \frac{\varepsilon \varepsilon_0 A}{d} \tag{2.7}$$

2.11 CHARGE-CONDUCTION MECHANIMS

2.11.1 Introduction

In an ideal metal-oxide-semiconductor (MOS) capacitor, the conductance of the insulating film is assumed to be zero. However, when the electric field or temperature is sufficiently high, the real insulators show carrier conduction. To estimate the electric field in an insulator under biasing conditions, the equation is showed as below

$$\xi_i = \xi_s (\varepsilon_s/\varepsilon_i) \tag{2.8}$$

where ξ_i and ξ_s are the electric fields in the insulator and semiconductor. ε_i and ε_s are the corresponding permittivity for the insulator and semiconductor [35].

Mobile ions such as sodium can transport through the oxide and give rise to device instability and hysteresis effect. For ultrathin SiO_2 or under a very high electric field, tunneling will occur [35].

Table 2.6 summarizes basic conduction processes in insulators. For Schottky emission process, thermionic emissions across the metal-insulator interface or the insulator-semiconductor interface are responsible for carrier transport. The Poole - Frenkel emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band. For trap states with coulomb potentials, the expression is virtually identical to that of the Schottky emission. The barrier height, however, is the depth of the trap potential well, and the quantity $\sqrt{(q/\pi\varepsilon_i)}$ is larger than in the case of Schottky emission by a factor of 2, since the barrier lowering is twice as large due to the immobility of the positive charge. The tunnel emission is caused by field ionization of

The Schottky effect expresses the change in electrostatics at a metal/semiconductor(=SC)-interface. This change arises because charges will flow from one side to the other. For example electrons will flow from an n-type SC to the metal. Once part of the SC conduction electrons have traveled to the metal, the positive donor-atoms remain unscreened. They give rise to a region which is positively charged (ie the depletion region) of a few nanometers thick (measured from the interface). Because of Poisson's Law, the energy bands will be bent due to this positive space charge.

This positive space charge at the SC side of the interface will yield a negative image charge at the metal side of the interface. The positive region at the SC-side "attracts" electrons from the metal-side. These electrons will not flow back toward the SC because they do not have enough energy to do so. Higher electron density occurs at the metal side. This is the image charge and its effect is to lower the Schottky barrier height (SBH). This SBH is defined as the energy difference between the metal Fermi level and the bottom of the n-type SC conduction band [51].

There are two main processes, emission of electrons from negative electrode into the conduction band of dielectric caused by the lowering of the barrier by an applied electric field (Schottky effect) and the thermal ionization of traps, which is also caused by a strong electric field (the Poole-Frenkel effect). Thermal emission over the barrier lowered by a strong electric field (Schottky effect) is governed by the Richardson-Schottky relation. The density of current from a material with work-function (height of surface barrier) Φ is given as

$$i = i_0 \exp\left(-\frac{\beta_{PF} e F^{1/2}}{kT}\right). \quad (2.13)$$

The difference is in constant,

Si_3N_4 also used as the gate dielectric in the metal-insulator-semiconductor (MIS) devices. Si_3N_4 have many traps, isolated states and smaller band gap. Al-Si_3N_4-Si is bulk-controlled rather than electrode- controlled.

$$J = J_1 + J_2 + J_3 \quad (2.14)$$

where

$$J_1 = C_1 E \exp\{-q[\phi_1 - (qE/\pi\varepsilon_0\varepsilon_d)^{1/2}]/k_B T\}, \quad (2.14a)$$

$$J_2 = C_2 E^2 \exp(-E_2/E), \quad (2.14b)$$

$$J_3 = C_3 E \exp(-q\phi_3/k_B T). \quad (2.14c)$$

where

E =electric field,

q =electronic charge,

Φ_1= barrier height of Si_3N_4,

ε0 =permittivity of free space,

εd = dynamic dielectric constant of Si_3N_4,

kB = Boltzmann constant,

T= the temperature in K

Φ_3= the barrier height of isolated states in Si_3N_4.

C_1 = density of trap centers

E_2, C_2=effective e mass and the depth of the trap potential well

then the lowering factor of the potential barrier, the high frequency dielectric constant, and the refractive index of these glasses were determined. [53].

2.11.3 Shallow -trap-assisted tunneling

Electronic conduction in thin oxynitride films is governed by three different mechanisms according to the strength of the electric field ranging from 6 to 14 MV/cm. The current conduction is due to the tunneling of electrons into the shallow traps in the insulator (current conduction is trap-assisted at electric field lower than 8MV/cm) (Fig. 2.13). In the high field region (>10 MV/cm), Fowler-Nordheim (FN) effect becomes dominant. In the moderate-filed effect region, traps can be filled by both FN current and direct tunneling of electrons into the traps, results in quasi-saturation region in the leakage current. "Shallow trap" means that the electrons trap cannot be filled at the measured temperature whereas the "Deep trap" refers to the trap that can be filled at the temperature. When a positive V_g is applied to a metal/NO (nitrided oxide)/silicon structure, part of the electrons in the silicon conduction band may directly tunnel to the shallow traps inside the nitrided oxide. Since the shallow traps cannot be filled by the injected electrons, the electrons will be migrate to other shallow traps along the field direction until they reach the metal electrode. This phenomenon is called shallow-trapped-assisted tunneling (STAT). On the other hand, Deep-trap-assisted tunneling (DTAT) or two-step tunneling occurs as some injected electrons may firstly tunnel from the deep traps in the nitrided oxide and then tunnel from the deep traps into the conduction band of the nitrided oxide (Fig. 2.13).

trap peaks at about 1,200 C for the 400 nm thickness and at 1,100 C or lower for the 100 nm thicknesses. The occupation of shallow traps during cryogenic irradiation decreases the occupation of the deeper trap compared with room temperature irradiation. At high concentrations, the shallow traps decrease the tunneling field of the deeper trap by trap-assisted tunneling [55].

Thin films of silicon oxynitride (SiON) were grown on Si substrates by nitriding rapid thermally grown SiO_2 layers in microwave-excited nitrogen plasma and by subsequent re-oxidation. The enhanced leakage current in SiON at oxide fields 5–7 MV/cm is due to a trap assisted tunneling current. Trap assisted tunneling current analysis indicated a trap level of 1 eV below the conduction band edge, which is shallower than ~2.5 eV level reported for nitrogen related traps in thermally nitrided SiO_2. This shallower trap level suggests that its origin could be oxygen vacancies in the rapid thermal oxide, generated in the plasma nitridation.[7] Experimental results show that the deep trapping effects at room temperature are similar to the shallow-level trapping effects observed by others below room temperature [57].

2.11.4 Direct tunneling

Direct tunneling in MOS structures with ultra-thin oxide (< 4 nm) during which electrons from the conduction band in semiconductor are transferred across the oxide directly (i.e. without changing energy) into the conduction band of metal; probability of direct tunneling is a very strong function of the width of the barrier electron tunnels through (oxide thickness in MOS devices) (Fig. 2.14) [71].

Assuming that a single effective mass can be used for the electron in all three regions and integrating the Fermi–Dirac distribution function yields [9]:

$$J_T = \frac{4\pi q m_x^* kT}{h^3} \int_0^\infty P(E_x) S(E_x) \mathrm{d}E_x \qquad (2.16)$$

where h is Planck's constant, m_x^* is the electron effective mass in the direction perpendicular to the barrier, E_x is the electron kinetic energy in the direction perpendicular to the barrier, k is the Boltzmann constant, T is the temperature, and $S(E_x)$ is the ''supply'' function, which is derived from the integration of the Fermi–Dirac distribution function, and is given by [59]:

$$S(E_x) = \ln \left\{ \frac{1 + \exp[(E_{fs} - E_x)/kT]}{1 + \exp[(E_{fg} - E_x)/kT]} \right\} \qquad (2.17)$$

where E_{fs} and E_{fg} are the electron Fermi levels in the semiconductor and the gate, respectively. Note that the applied voltage is implicitly present in this equation through the difference between the Fermi levels. Calculation of the tunneling probability requires solving Schrodinger's equation for the electron wave function; typically this is done only in the direction perpendicular to the surface, and using the effective mass approximation, that is, assuming the electron is free and including the effect of the periodic lattice potential through the use of the effective mass.

The condition of a "slow" change of the potential means that the changes in the potential and its derivative on each electron wavelength, should be small compared to the energy of the particle. This is known as the Wentzel–Kramers–Brillouin (WKB) approximation. The tunneling probability is calculated by a modified Wentzel–Kramers–Brilliouin ~WKB approximation, which takes the reflections near the Si/SiO_2

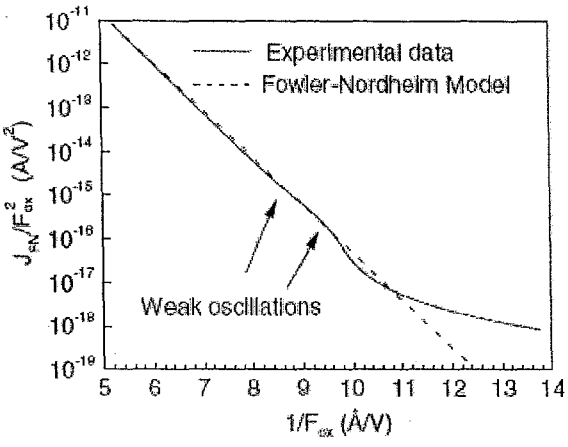

Figure 2.15: Fowler–Nordheim plot of measured tunneling current (solid line) in a MOS structure (t_{ox} = 40.5A °), showing weak oscillations around the straight line (dashed line) that is predicted by the Fowler–Nordheim equation [57].

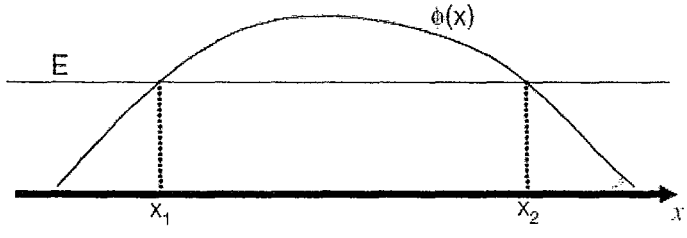

Figure 2.16: Arbitrary potential barrier, showing the classical turning points

The tunneling probability through a barrier of arbitrary shape is approximately given by (Fig. 2.16) [62]:

$$P \approx \exp\left(-2\int_{x_1}^{x_2} \kappa(x)dx\right) \qquad (2.20)$$

where x_1 and x_2 are the classical turning points, that is, the points at which the energy of the particle is equal to the potential, as shown in Figure 5. For direct tunneling through a trapezoidal barrier, the classical turning points are the metal– insulator and insulator semiconductor interfaces [63].

to reduce dynamic power consumption [70], and it will continue playing its role in the reduction of leakage power as well.

2.11.5 Fowler–Nordheim tunneling

Thermally grown SiO_2 films were widely used as the gate dielectric in early MOSFETs. In 1969, Lenzlinger and Snow have investigated the electrical conduction in SiO_2 grown in dry O_2 with thickness ranging from 64 to 500 nm [52]. As compare to other insulator, thermally grown SiO_2 is more likely to show electrode-limited conduction because it has an extremely wide bandgap and consequently a high energy barrier at its contact with an electrode. However, bulk-limited mechanisms are less likely to play a role because of the low trap density in the forbidden band and the relatively high electron mobility in the conduction band [52].

The energy-band diagram of a MOS structure is illustrated in Fig. 2.17. The energy barrier from the silicon conduction band to the oxide conduction band is 3.25 eV, while the barrier for holes ϕ_{sh} from the silicon valence band to the oxide valence band is 3.8 eV. However, the energy barrier ϕ_m from the metal Fermi level to the oxide conduction band depends on the type of metal [52].

The energy band diagram for a metal–oxide–p-type semiconductor, without applied voltage, is shown in Fig. 2.18 [72]. The bending is caused by the metal-semiconductor work function difference and the oxide fixed charge. The metal–semiconductor work function difference is presumed to be negative as for example in the case of the MOS device with an Al gate on a Si substrate.

always less than the silicon bandgap, for large applied voltage, the oxide field is approximately equal to the applied voltage divided by the oxide thickness.

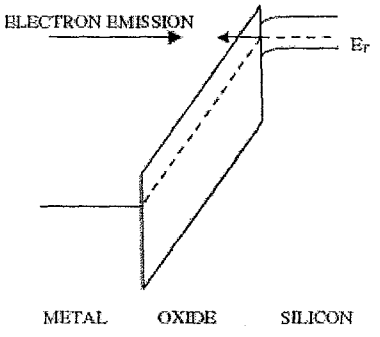

Figure 2.19: Energy-band diagram of a metal–silicon dioxide–silicon structure with large positive bias on the metal.

Figure 2.20 shows the energy-band diagram when a negative bias is applied to the metal electrode. In the dark and in the absence of bulk limitation, the current is due to either Schottky emission of electrons over the barrier ϕ_m, or FN tunneling of electrons through the triangular barrier into the oxide conduction band, with the latter mechanism dominating at room temperature. Emission of hole from the silicon valence band into the oxide valence band is also possible. However, because of the high barrier (ϕ_{sh} = 3.8 eV), hole emission is not expected to occur, except in the case of Au electrode.

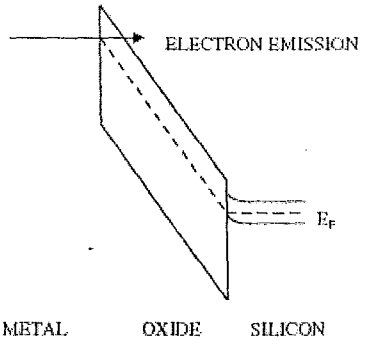

Figure 2.20: Energy-band diagram of a metal–silicon dioxide–silicon structure with large negative bias on the metal electrode.

Fowler–Nordheim plot which is the plot of J_{FN}/F_{ox}^2 versus $1/J_{FN}$ yields a straight line (Fig. 2.22). This plot give a good fit for experimental data with wide range of voltage for MOS structure that is relatively thick oxide and metal gate. However, this relatively simple Fowler–Nordheim model is not enough to take into account the effects of modern structure such as [72]:

- Direct tunneling through an approximately trapezoidal barrier for low applied voltages.
- Carrier quantization in the inversion/accumulation layer.
- Tunneling mechanisms other than conduction band tunneling of electrons (valence band hole tunneling and valence band electron tunneling).
- Effect of the finite temperature on the availability of carriers for tunneling.
- Depletion effects on the polysilicon gate.

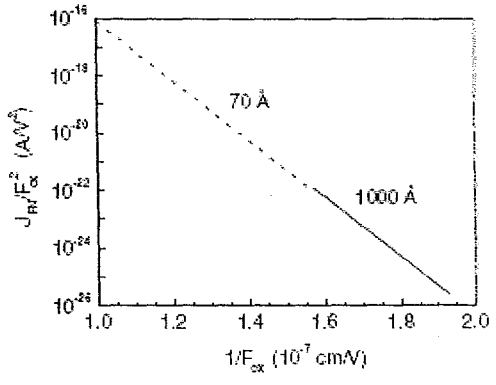

Figure 2.22: Fowler–Nordheim plot of tunneling data from (100) silicon into thick SiO_2 oxides. The two lines correspond to two sets of experimental data from different groups for two different oxide thicknesses; the slope and intersect of the Fowler–Nordheim plot are both independent of oxide thickness, as expected from (1) [72].

where the integration limit $x_1 = (V_{appl} - \phi_t)/E$, E is the electric field across the nitrided oxide film, N_t the concentration of electron traps in the nitrided oxide film. With the effect of image force and the lowering of Coulombic potential barrier associated with the traps neglected, electron tunneling probabilities from the metal to the trap (p_1) and from the trap to the conduction band of the nitrided oxide (p_2) [52].

For fairly high values of E and ϕ_t, equation (2) can be written as,

$$J_{dt} = \frac{2C_t N_t q \phi_t \exp[(-D/E)\phi_t^{3/2}]}{3E} \tag{2.25}$$

where $D = 4\sqrt{2q m_{ox}}/3h$ (2.26)

Further manipulating the equation leads to

$$\ln(J_{dt} E) = (-D\phi_t^{3/2})(1/E) + \ln(G) \tag{2.27}$$

where $G = 2C_t N_t q \phi_t / 3$.

ϕ_t can be easily extracted by plotting $\ln(J_{dt} E)$ vs $1/E$

where $\phi_t = (-\text{slope}/H)^{2/3}$ (2.28)

where H = 4.85 x 10^9 V/m for mox equal to 0.5 me [52]. The Y -intercept of the plot can be used to calculate N_t.

The two-step tunneling model can well describe the current transport of thermally nitrided oxide films with deep trap energy level of 2.1–2.75 eV [52], as shown by the good fitting between theory and experiment in Figs 2.23 and 2.24. However, this model does not account for the effect of bulk shallow trap in thermally nitrided oxide films, which is very important in the current transport of these dielectric films. Hence, the the two-step tunneling mechanism is inadequate for nitride oxide films with shallow-trap energy levels.

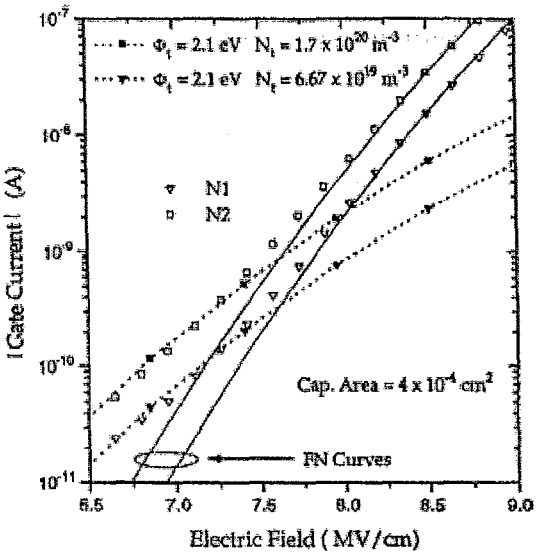

Figure 2.24. Theoretical and experimental plots of total currents for the samples of N1 and N2. For N1 sample (1.20 dilution, which represents the ammonia. nitrogen) for 15 min at 950 °C, ϕ_t = 2.1 eV, N_t = 6.7 x 10^1 cm^{-3}; and for N2 sample (1.10 the dilution), ϕ_t = 2.1 eV, N_t = 1.7 x 10^{20} cm^{-3}. Also included are the FN curves associated with the experimental data [71].

2.11.7 Band-to-band tunneling

As MOSFET shrinks, the thickness of its gate dielectric has been reduced to below 20 Å [52]. In the sub-20 Å regime, the gate-oxide thickness (T_{ox}) is close to or less than the FN direct-tunneling thickness, the transport current in gate dielectric is mainly contributed by the electron and hole tunnelings from one energy-band to another [52]. Figure 2.25 shows that when a negative voltage is applied to the poly-silicon gate, the electrons from the conduction band of the gate can tunnel to the conduction band of the silicon substrate directly (ECB). On the other hand, the electrons in the valence band of the gate can directly tunnel to the conduction band of the silicon substrate (EVB). In addition, the holes in the valence band of the silicon

Table 2.7: Model parameters for different tunneling processes [52].

Table 7
Model parameters for different tunneling processes [41]

Parameters	ECB	EVB	HVB
m_{ox}	$0.4m_0$	$0.3m_0$	$0.32m_0$
ϕ_b (eV)	3.1	4.2	4.5
ϕ_{bo} (eV)	3.1	3.1	4.5
α	0.6	1.0	0.4

N indicates the density of the tunneling carrier for ECB and EVB or the receiving energy state for EVB.

In both the inversion and accumulation regimes, the ECB and EVB tunneling processes are given by

$$N = \frac{\varepsilon_{ox}}{T_{ox}}\{S \cdot \ln[1+e^{(V_{ge}-V_{th}/S)}] + V_t \cdot \ln[1+e^{(-V_g-V_{FB}/V_t)}]\} \tag{2.31}$$

where S is the sub-threshold swing, V_{th} the threshold voltage, V_{FB} the flat-band voltage, $V_t = (kT/q)$ the thermal voltage and V_{ge} the gate voltage minus the gate depletion voltage (V_g - V_{poly}) [52].

For the EVB tunneling process:

$$N = \frac{\varepsilon_{ox}}{T_{ox}}\left\{3V_t \cdot \ln\left[1+e^{\frac{q|V_{ox}|-E_g}{3kT}}\right]\right\} \tag{2.32}$$

where E_g is the energy band gap and 3 is a fitting parameter. V_{ox} is a function of V_g as described in [52]. Note that through the ϕ_b and ϕ_{bo} and V_{FB} terms, this model is applicable to N^+ and P^+ poly-Si gates as well as other gate materials such as SiGe [52].

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CHAPTER 3

EFFECTS OF THERMAL NITRIDED GATE-OXIDE THICKNESS AND POST GROWN ANNEALING ON 4H SIC-BASED METAL-OXIDE-SEMICONDUCTOR CHARACTERISTICS

3.1 INTRODUCTION

Thermal nitrided silicon dioxide (SiO_2) has been widely accepted as the best quality gate oxide used in silicon carbide (SiC) based MOS devices [1]-[4]. With this gate oxide, it enables SiC to be used as a substrate for MOS-based devices in high power, high frequency, high temperature, and non-volatile memory applications [5],[6]. In these applications, thickness of the nitrided oxide (t_{ox}) is different due to the difference in their device structures and requirements. It may range from *ultra-thin oxide*, commonly used as a buffer insulator in gas sensor (t_{ox}=1.5 nm) [7] and in stacking high dielectric-constant gate (t_{ox}<8 nm) [8], to *thin oxide* as the gate insulator for non-volatile memory devices (12 nm<t_{ox}<20 nm) [9], and to *thick oxide* as the gate insulator for high power metal-oxide-semiconductor field-effect transistor (50 nm<t_{ox}<70 nm) [5]. Currently, most of the studies on nitrided oxide are concentrating on thin-oxide region approximately 12-22 nm. Using this knowledge, the quality of ultra-thin and thick nitrided oxide is assumed to be the same as the thin oxide. However, according to Si–SiO_2 system, charge transport mechanism in the oxide, oxide breakdown field, and oxide reliability are strongly depending on the oxide thickness [10], [11]. While flatband voltage (V_{FB}) and interface-trap density (D_{it}) are not [10], [11]. Therefore, the assumption used in SiC–SiO_2 system is questionable and it is

20 nm) and post grown annealing on SiC-based MOS characteristics has been reported. From this study, correlation of effective oxide charge (Q_{eff}) and *total* interface-trap density (N_{it}) with oxide breakdown field (E_B) and current transport mechanism in the oxide have be established. Detail analysis of the mechanisms on n-type 4H SiC-based nitrided SiO_2 as a function of nitrided oxide thickness and electric field has also been reported.

3.2 EXPERIMENTAL PROCEDURES

N-type, 8° off (0001) oriented, 4H–SiC wafers with 10-μm thick epilayer doped with (1-4)×10^{16} cm^{-3} of nitrogen were used to fabricate the MOS-capacitor test structures. After underwent a standard wafers cleaning process, seven different thicknesses of thermal nitrided SiO_2, ranging from 2 to 20 nm were grown on the wafers in a horizontal tube furnace with 10%-N_2O ambient at 1175°C. The samples were loaded in the furnace at 1175 °C. The oxidation/nitridation time was adjusted to obtain the required t_{ox}. After the oxide growth, the furnace was cooled down to 800 °C in high-purity N_2, approximately at 10 °C/min, before the samples were removed. Subsequently, aluminum was sputtered on the oxides to form gate electrodes. The areas, A, (1.30×10^{-3} cm^2) for the MOS capacitors were then defined by photolithography. Finally, a large area of aluminum back contact was sputtered on the n^+ substrate. A computer controlled *Semiconductor Parameter Analyzer* (HP-4156) was used to measure leakage current of the capacitor. The gate current (I_G) as a function of forward gate-voltage sweep, V_G, (ramping rate = 0.3 V/s) was recorded. The I_G-V_G plot was then transformed into *J-E* plot. Post-metallization annealing was not performed, so as to avoid masking the effects of the oxides. The subsequent methods of characterizations and extractions of Q_{eff}, D_{it}, N_{it}, and E_B have been described elsewhere

Figure 3.1 shows the results of t_{ox}, with two distinguish regions labelled as A and B, as a function of oxidation/nitridation time, t. Region A demonstrates a linear oxide growth with a rate constant of 5.2 nm/hr, which is comparable with the literature (~6.0 nm/hr) [22]. However, for t_{ox}<8 nm (region B), the linear growth of the oxide has been suppressed by an accelerated initial oxide growth [23]. The combination of these two growth rates (dt_{ox}/dt) in this *ultra-thin* region can be well fitted in the following model [23]:

$$\frac{dt_{ox}}{dt} = C + a_0 e^{-t/\tau} e^{-E_A/kT} \tag{3.1}$$

where the first and second terms are representing the linear- (C) and initial-rate constants. a_0, τ, E_A, k, and T are constant, time constant, activation energy, Boltzmann's constant, and temperature, respectively. The linear-rate constant in this region (5.4 nm/hr) is very close to the value obtained in region A, by considering E_A = 2.8 eV [22], T = 1448.15 K and no oxide is grown at t = 0 min. The extracted τ value is 65.8 min^{-1} and it is associated with the time needed to produce an equilibrium oxide thickness [23].

These observations are different from those reported in Si–SiO2 system [10],[11], as there is an extra alternative layer of carbon in SiC that will be removed during nitridation process. During initial oxidation (t_{ox} = 2-5 nm), carbon is probably accumulated at SiC–SiO_2 interface (increasing trend of N_{it}) and a non-equilibrium and disordered oxide is grown. When t_{ox} increases, the accumulated carbon at the bulk and interface is reduced as the oxidation and nitridation processes are in equilibrium. However, the reduction has a limitation. As the t_{ox} increases further, the well passivated interface has to be de-passivated in order for the subsequent oxidation to proceed. The forming and breaking of the bonds may affect arrangement of the bulk SiO_2 network. As a result, Q_{eff} again demonstrated a negative value. This cycle continues as the oxide gets thicker and thicker.

In Fig. 3.2(a), the changes of gradient, G, of high-frequency capacitance-voltage curves from flatband to depletion capacitance of the oxides has been extracted. Commonly, G is qualitatively associated with N_{it}. The higher the G value, the lower the N_{it}. However, in this work, we have demonstrated that it is not valid for samples with t_{ox}<6 nm [Fig. 3.2(b)].

The effect of t_{ox} on current transport mechanism has been presented in current density (J)-electric field (E) plots [Fig. 3.3(a)]. Any E that enables $J \geq 10^{-6}$ A/cm^2 is defined as oxide breakdown field, E_B. This parameter as a function of t_{ox} is presented in Fig. 3.3(b). From the shape of the J-E plot, one can conclude that the current transport mechanisms in the investigated oxides are the same except for those with the thinnest oxide. Fowler-Nordheim (FN) and direct (DT) tunnelling [11] are the major conduction paths of electron injecting from SiC substrate through the oxide with t_{ox}>2.1 nm and ≤2.1 nm, respectively. From FN plots, barrier height, Φ_B, between conduction band edge of SiC and nitrided

oxide as a function of t_{ox} have been extracted [Fig. 3.3(b)]. The extremely small value of Φ_B obtained from t_{ox}=2.1 nm is another good indicator showing that the current conduction mechanism in this oxide in not dominated by FN, but by others (here we have proven that it is via DT). The effects of t_{ox} on these parameters (E_B and Φ_B) can be correlated with Q_{eff} and N_{it} and it will be discussed in the following paragraphs.

Figure 3.4(a) shows the correlation graph of E_B with Q_{eff} and N_{it}. A good correlation of E_B with Q_{eff} has been established for $7.4 \leq E_B \leq 8.5$ MV/cm. It has suggested that Q_{eff} is the dominating factor affecting E_B value at this range. As Q_{eff} value becomes more positive, more injected electrons from SiC substrate are able to be captured and trapped in the positive trap centres rather then use to break the network of bulk SiO_2. These trapped centres are neutralized by the electrons so that more electrons are required for the oxide breakdown process and attributed to the increase of E_B. In addition to that, reduction of N_{it} is also enables the oxide breakdown strength to be improved, in particular for $6.5 \leq E_B \leq 7.6$ MV/cm. However, N_{it} has become a secondary factor for the improvement at $7.6 \leq E_B \leq 8.5$ MV/cm if compared with Q_{eff}. For $E_B \leq 6.5$ MV/cm, further investigation is needed to identify which factors are affecting the oxide breakdown process as no concrete evidence has been demonstrated in this work.

The correlation graph between Φ_B and Q_{eff} has been established in Fig. 3.4(b). The Φ_B value that is associated with sample having t_{ox}=2.1 nm was ignored in this establishment as it was not a reliable value. Those samples with $Q_{eff} = (5\text{-}10)\times10^{11}$ cm^{-2} are having Φ_B values comparable with the theoretical one (2.7 eV) [24]. When Q_{eff} value becomes more positive, Φ_B is increased. In contrast, Φ_B is lowered when negative Q_{eff} is

obtained in the sample. These observations are agreeable to the theory suggested in Si–SiO_2 system where the effective positive charge in the bulk may convert into neutral electron traps and the effective negative charge in the bulk may increase the number as electrons are injected via FN tunnelling [11],[25]. In the figure, a correlation between N_{it} and Φ_B was not established. Therefore, we conclude that Φ_B value is only strongly dependence on Q_{eff} and not on N_{it}.

3.3.2 Charge Conduction Mechanisms through Different Nitrided Oxide Thickness

Figure 3.5(a) shows a typical plot of current density, J, ($J=I_G/A$) as a function of electric field, E, [$E \cong (V_G-V_{FB})/t_{ox}$] for some of the investigated oxides, which have been fitted with Ohm's law [$J_{ohm} = qn_0\mu E$] and trap-filled limit (TFL) [$J_{TFL} = BE^m$] process. The symbols J_{ohm}, J_{TFL}, V_{FB}, q, n_0, μ, B, and m are current density governs by Ohm's law, current density governs by TFL process, flatband voltage, electronic charge, density of thermal generated free carriers, electronic mobility in the oxide, a constant, and a trap distribution and temperature related constant [26]. These are the two out of three conduction mechanisms governing a space-charge limited (SCL) process. From the curve fitting results, the third SCL mechanism – Child's law – was not revealed in all of the oxides. The gradient, S, of the J-E plots obtained from the above two mechanisms are presented in Fig. 3.5(b). The legends "Ohm's (1)", "TFL", and "Ohm's (2)" in the figure refer to the governing conduction mechanism by Ohm's law at initiate electric field, follows by trap-filled limit, and subsequently take over again by Ohm's law. This observation was only limited to oxides with thickness of 5.0 and 9.6 nm. The dominate conduction mechanism of the remaining oxide thicknesses is either by Ohm's law or Ohm's law followed by TFL process. It is clear that the extracted S values from Ohm's law as a function of t_{ox} are closed to its theoretical value of 1. For current conduction obeying Ohm's law, at this extremely low electric field, the density of thermally excited electrons from trap centres located at bulk oxide is much larger than the density of injected electrons from SiC. This is because, at this electric field, electrons from semiconductor are unable to be injected into the oxide, even through its concentration is much higher than concentration of trapped electron. Since, this is happened in an electrically quasineutral state, the empty traps are unable to be filled by any weak injected electron from SiC.

Therefore, the detected leakage current density from this conduction mode is ultra-low [Fig. 3.5(a)] [27]. As E is further increased, more electrons are able to be supplied and injected from SiC. The injected electron may be captured in trap centres located at the bulk oxide. When trapping of electron happens, TFL process, which is a charge compensation-free is started to reveal. The electric field that enables the electron-trapping process is refers to E_{on}. As the electric field is further increases, more electrons are being injected into trap centres located deeper below Fermi level. This trapping process is continue until all of the deep traps are completely filled. At a higher electric field, no further electrons are able to be trapped. The extracted S value from the TFL process is between 2 and 5 [Fig. 3.5(b)]. At E_{on}, transit time of electron (τ_e) is equal to the relaxation time of dielectric and it is estimated by $\tau_e = \varepsilon(E/J)$, where ε is the dielectric constant of oxide and E/J is the inverse gradient of J-E plot for Ohm's Law. The τ_e values estimated are in the ranging of $(1.8\text{-}5.0)\times10^{-7}$ s, depending on the oxide thickness. By knowing the value of τ_e and E_{on}, the value of μ ($\tau_e=t_{ox}/\mu E_{on}$) could be computed. Since only samples with t_{ox}=2.0, 5.0, 9.6, and 16.6 nm have revealed the transition electric field from Ohm's law to TFL process (E_{on}), therefore, these are the only oxides with μ values that have been calculated (Fig. 3.6). The calculated μ value is similar to those obtained from Ohm's Law. Even though all of the oxides were grown in same process and condition, the extracted μ and S values are much different in this process.

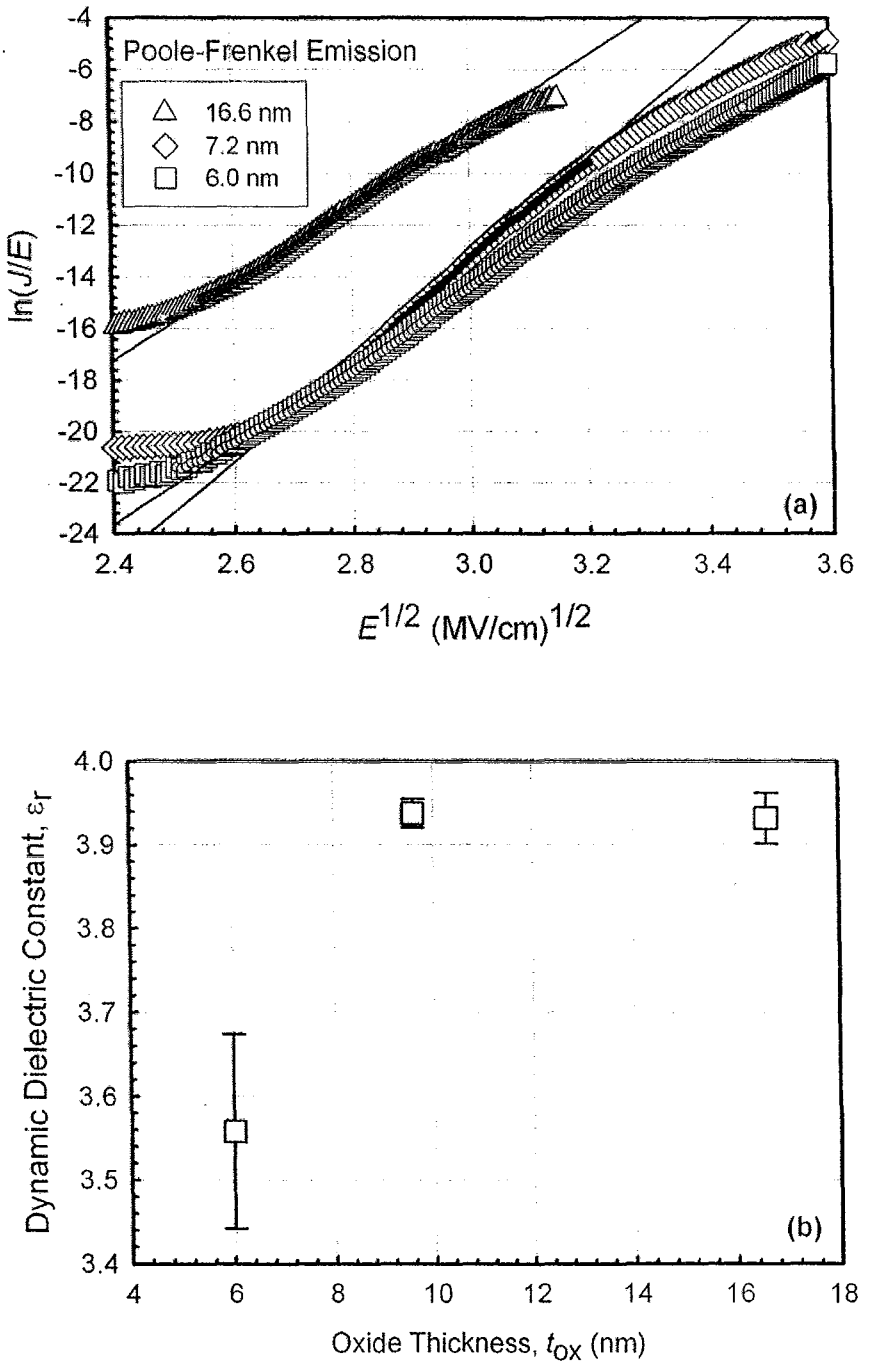

Fig. 3.7. (a) Poole-Frenkel (PF) [$\ln(J/E)$-$E^{1/2}$] plot of oxides with different oxide thicknesses. Solid symbols represent data points for PF emission linear fitting. (b) The extracted dynamic dielectric constant, ε_r, as a function of oxide thickness.

MOS-based devices operate at or below 3 MV/cm is govern by Ohm's law or/and TFL process and not FN tunneling.

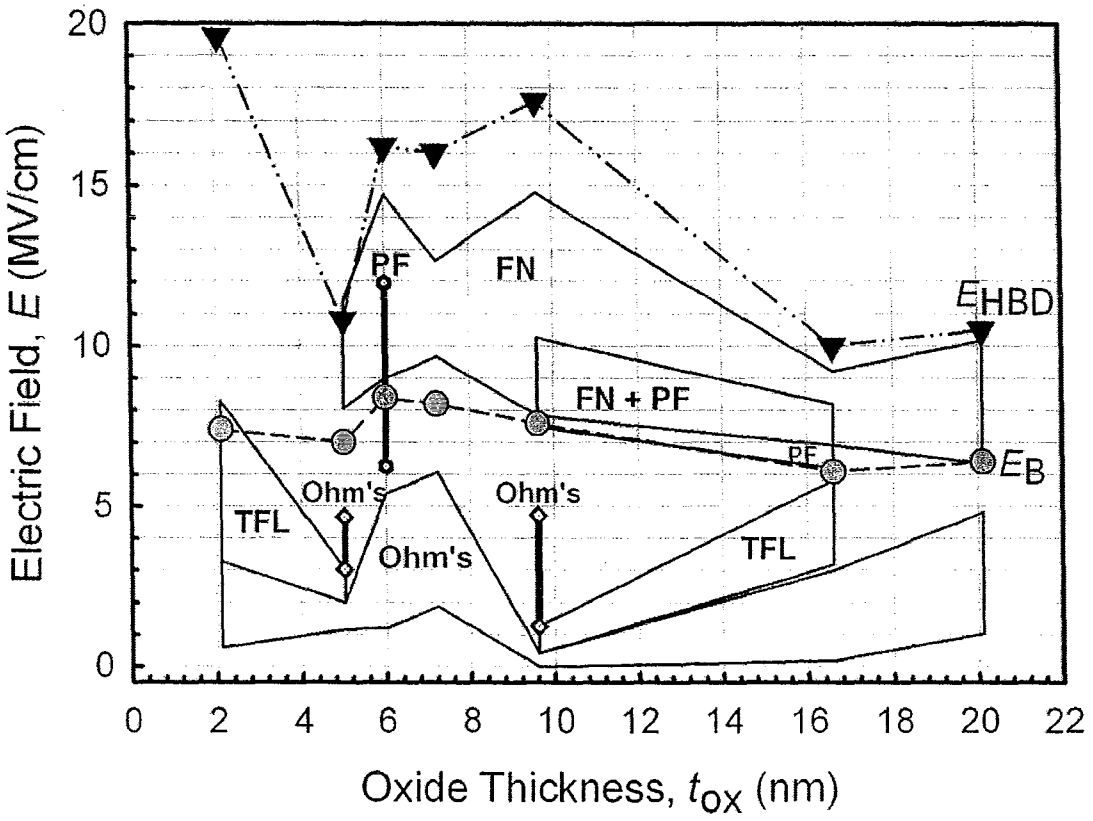

Fig. 3.8. A relationship plot among electric field, E, oxide thickness, t_{ox}, and potential charge conduction mechanisms for thermally grown nitrided on n-type 4H SiC. Breakdown field (E_B) and hard breakdown field (E_{HBD}) of oxide have been included in the plot.

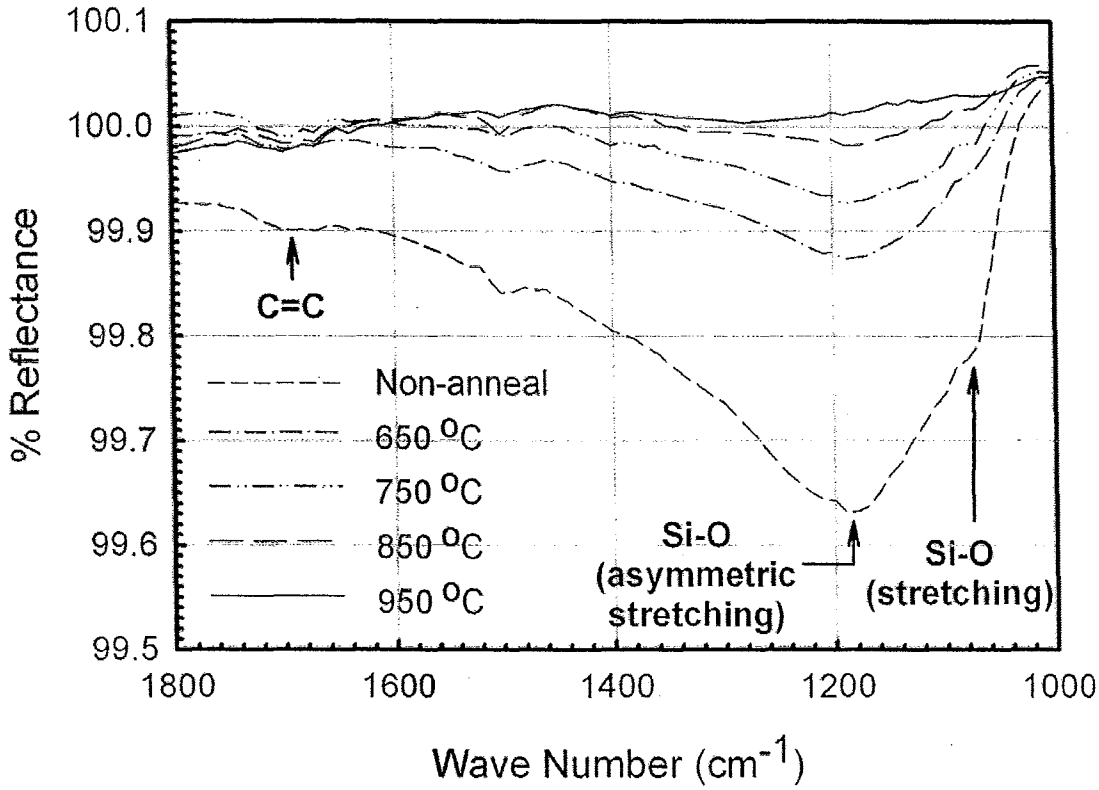

Fig. 3.9. Fourier transform infra-red spectra of annealed and non-annealed oxides obtained from reflectance mode.

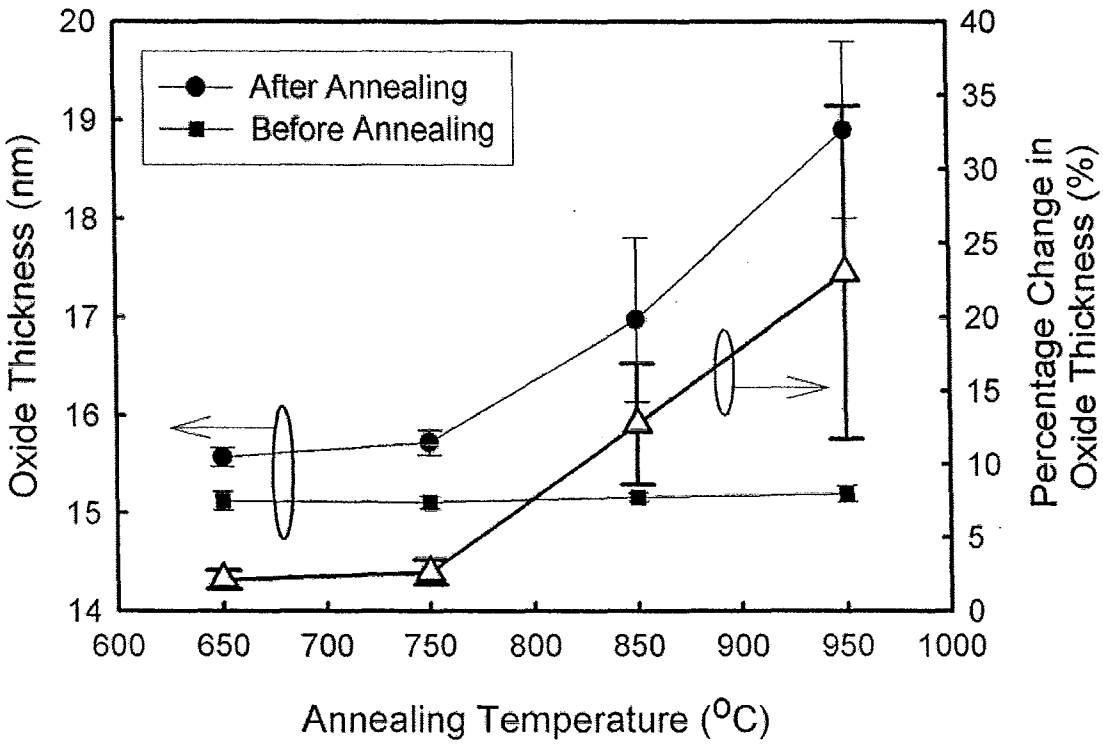

Fig. 3.11. Effects of vacuum annealing on the changes in absolute and percentage change of oxide thickness. The error bar represents median and standard deviation of the changes in absolute and percentage change of the oxide thickness.

The measurements of oxide thickness were carried out using a *Filmetrics* system at a wavelength of 632.8 nm. Other than measuring the thickness of the oxide, *Filmetrics* was also employed to measure the refractive indices (n) of the samples. Before vacuum annealing was carried out, the initial oxide thickness was 15.3 nm (Fig. 3.11). However, after being exposed to high-temperatures vacuum annealing, its thickness was increased. The percentage change in oxide thickness was increased slightly until the sample has been

respect to the annealing temperature. This suggested that the surface structure of the SiO_2 film may be changed after being annealed in vacuum. The change of surface structure probably is related to the weakening of Si-O-Si bonding in the bulk oxide. The transformation of surface topography as a function of annealing temperature will be presented in the subsequent paragraph. The density (ρ), porosity (Π), and dielectric constant (k) of the samples can be determined from the measured n value. The ρ value has be calculated using the following relationship [33]:

$$\rho = (n-1)/0.202 \quad (1)$$

From the calculated film density, Π and k values can also be obtained from the following relationships [33]:

$$\Pi = 1 - \rho/\rho_s \quad (2)$$

where Π is the film porosity and ρ_s (thermally grown conventional SiO_2 film) = 2.27 g/cm^3 and

$$k = 1 + 1.28\,\rho \quad (3)$$

The effects of vacuum annealing on the film density and porosity are shown in Fig. 4. The film density and porosity are reduced and increased, respectively, as a function of annealing temperature. The theoretical value of film density for pure SiO_2 is around 2.0 – 2.3 g/cm^3 [32]. The calculated density values of sample without annealing and annealed at 650 °C are in the theoretical range and the values for other samples are reduced gradually. This reduction is also associated with the increment of porosity in the annealed films. The increment of porosity may be attributed to the weakening of Si-O-Si bonding in bulk structure of SiO_2. Figure 3.12 also presents the calculated results of k as a function of annealing temperature. Theoretically, the k value of SiO_2 is 3.9 [32]. From the observation, control sample and sample annealed at 650 °C are the two samples that possessed the average k value near to the theoretical value. The k value is reduces as the annealing

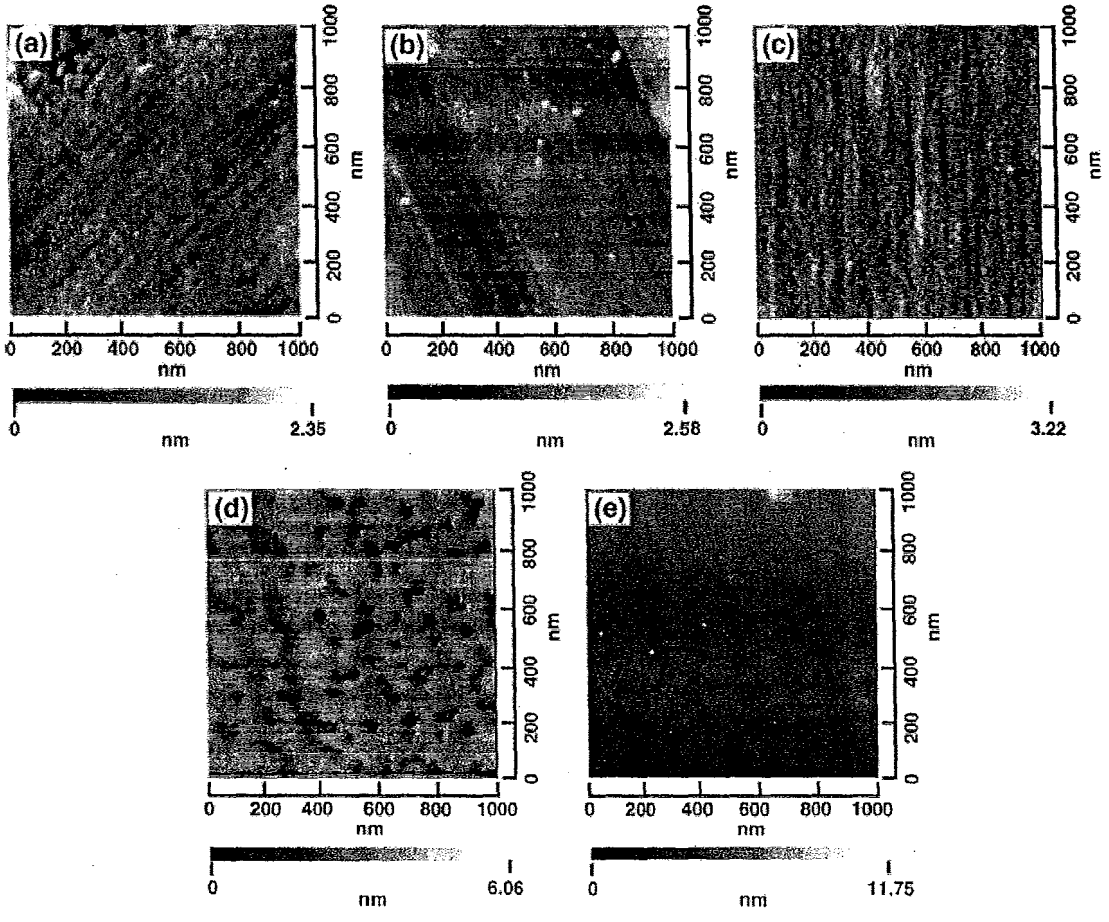

Fig. 3.13. Two-dimensional surface topography of (a) non-annealed oxide, (b) 650 °C-, (c) 750 °C-, (d) 850 °C-, and (e) 950 °C-annealed oxides.

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among thermal nitrided SiO_2 directly grown in 1, 10, and 50% N_2O at 1175°C has been performed. It has shown that the lowest leakage current density (J) has been revealed by 10%-N_2O grown oxide for an applied electric field (E) not larger than 7 MV/cm. However, beyond this field, a higher J value and lower dielectric breakdown field has been revealed by this oxide. In order to explain this observation, electronic and physical properties of the nitrided oxides and charge-conduction mechanisms through these oxides have been investigated. By understanding the MOS characteristics, it enables the gate oxides to be applied in a high voltage field effect transistor [2].

4.2 EXPERIMENTAL PROCEDURE

Nitrided SiO_2 was directly grown on a pre-cleaned [4] n-type, 8° off (0001) oriented, 4H–SiC wafers with 10-μm thick epilayer doped with $(1\text{-}4)\times10^{16}$ cm^{-3} of nitrogen, in a horizontal tube furnace at atmospheric pressure. Three types of nitrided oxides were grown using three different percentages of N_2O gas, i.e. 1, 10, and 50% N_2O mixed with 99, 90, and 50% of high purity N_2 gas, at 1175°C with the flow rate of approximately 200 ml/min. The oxide thickness (t_{ox}), calculated from high-frequency (100 kHz) capacitance-voltage (HF C-V) curve, was 9-11.5 nm. After the oxide growth, the furnace was cooled down to 800°C at a rate of 10°C/min in a high-purity N_2 gas flow, before the samples were removed. Subsequently, the MOS capacitors with an area (1.30×10^{-3} cm^2) was fabricated [4]. A computer controlled *Semiconductor Parameter Analyzer* (HP-4156) was used to measure leakage current of the capacitor at temperature ranging from 25 to 140°C. The same temperature range was used to obtain the HF C-V curve (not shown). The deviation of flatband voltage shift (ΔV_{FB}) as a function of temperature was minute. From ΔV_{FB}, effective oxide charge density (Q_{eff}) has been

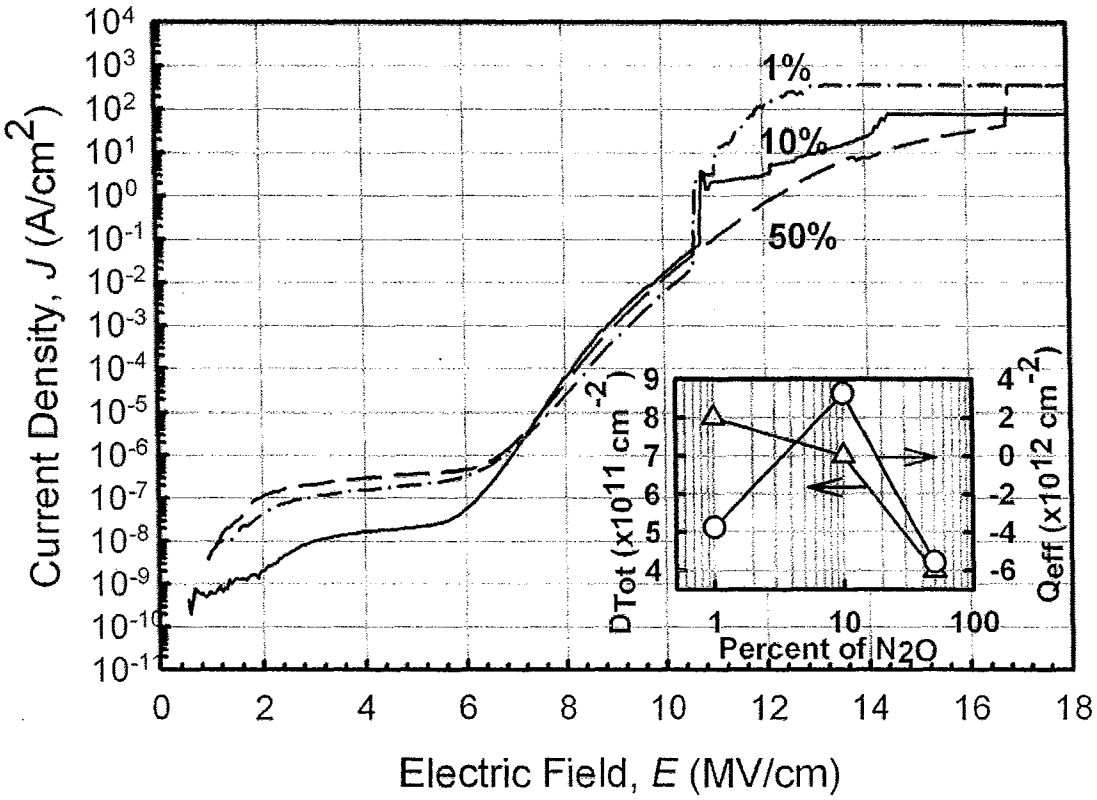

Fig. 4.1. A comparison of current density (J) as a function of electric field (E) for the three investigated oxides measured at room temperature. Total interface trap density (D_{Tot}) and effective oxide charge density (Q_{eff}) as a function of N_2O concentration is shown in the inset of the figure.

From the slope and interception of $\ln(JE)-1/E$ plot (Fig. 4.2), Φ_t and N_t were estimated (inset of Fig. 4.2) using a linear curve fitting method. A total of 25 samples from each type of oxides were measured and fitted. The fitting is acceptable when it is having a coefficient

The identification of oxide-SiC interfacial layer compound and thickness provide a quantitative characterization of the investigated oxides. Figure 4.3 shows the photoelectron spectra of O 1s and N 1s of the investigated oxides. An ordinary Gaussian function (solid line) was used in the deconvolution of the measured results (open circle). The O 1s region is well fitted with Si-O and Si-O-N at a binding energy of 532.7 and 531.7 eV, respectively [16]. The former component is attributed to bulk SiO_2 and there is no shift in the binding energy of the three oxides. However, the intensity is different with the highest being shown in 1%-N_2O grown oxide. The other component (Si-O-N) is originated from the interfacial layer of SiO_xN_y, which is caused by the nitridation process. When the amount of N is reduced, this component is shifted to a higher binding energy. It will eventually coincide with the binding energy of Si-O when N is zero. Similar observation has been obtained from N 1s spectra [Fig. 4.3(b)]. The Si-O-N component (reference binding energy is 398.3–399.0 eV [17]) is shifted to a lower binding energy as the concentration of N_2O is reduced. Another component lying at a binding energy approximately 1.3 eV lower is corresponded to Si-N [17]. As the N_2O concentration is reduced, a deviation of Si-N peak to a smaller binding energy is revealed. The Si-N component of 10%-N_2O grown oxide (396.90 eV) is corresponds to Si≡N (396.97 eV) and it is in agreement with literature [2],[3]. However, this component is shifted to a lower or higher binding energy as the concentration of N_2O is reduced to 1% or increased to 50%, respectively. This may be attributed to the amount of N being incorporated into the interface and subsequently affecting the orientation and bonding of Si-N compound [18].

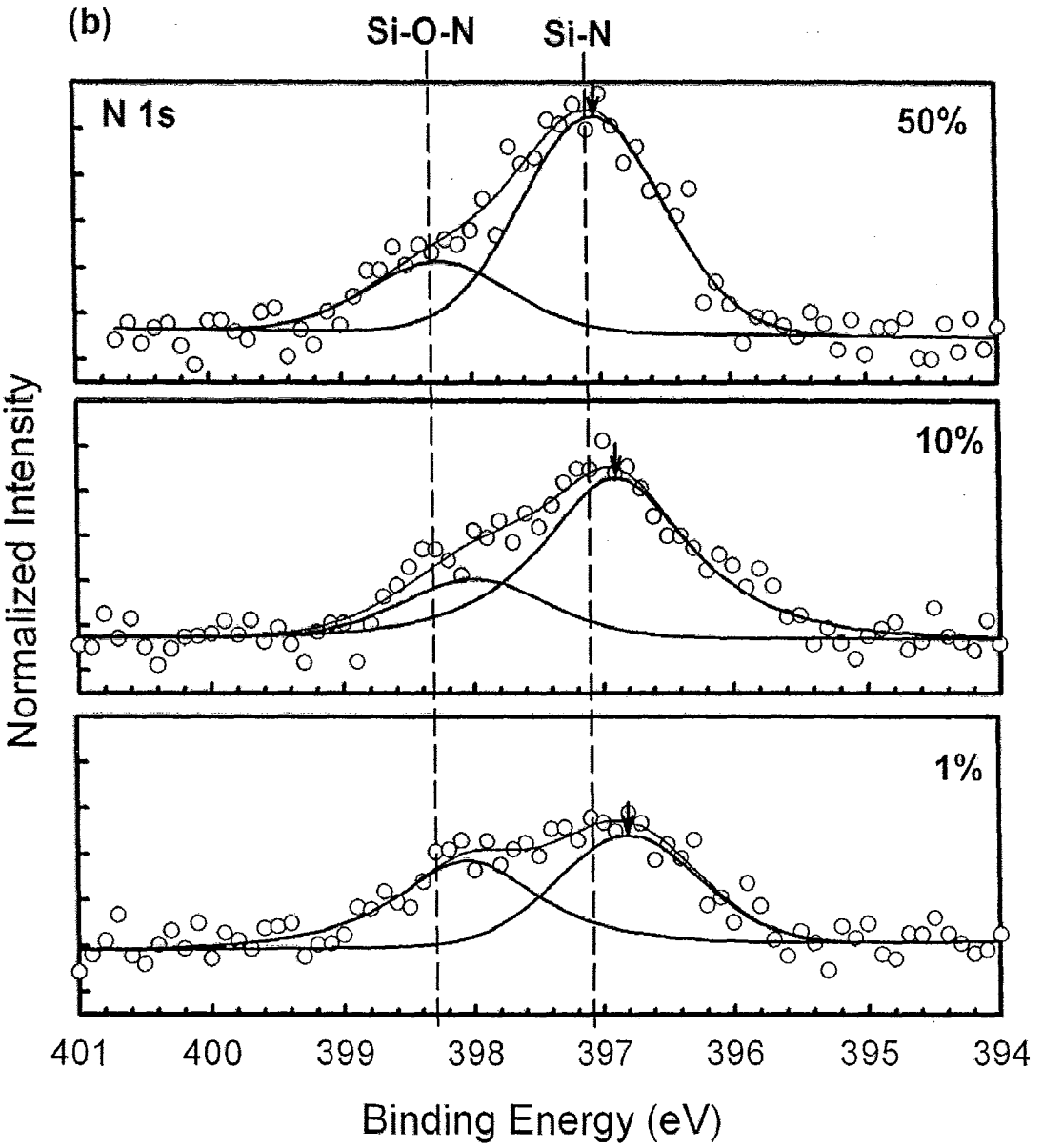

Fig. 4.3(b): continue.

Table. 4.1. Calculated thicknesses of Si-N, Si-O-N, and Si-O layers on 4H-SiC after grown by diluted N_2O gas.

N_2O %	Si-N thickness (nm)	Si-O-N thickness (nm)	Si-O thickness (nm)
1	0.98	1.01	1.51
10	1.15	0.88	1.08
50	1.17	1.08	1.55

X-ray reflectivity (XRR) was used to analyze oxide thickness, interface roughness, and electron density, which was related to oxide density. The XRR measurements were performed by a PANalytical X'Pert PRO MRD in a scattering angle range of $0 \leq 2\theta \leq 2°$ after the metal electrode gate has been etched. The X-ray source is a Cu Kα wavelength of $\lambda = 1.54$ Å using tube current of 40 mA and a voltage of 40 kV. The measurement was carried out using a set-up consisted of X-ray multilayer mirror at the incident beam and parallel plate collimator at the scatter beam. The measured results were analyzed using X'Pert Reflectivity version 1.1 software based on Paratt formulae. The fitting of the investigated nitrided SiO_2 film was performed using a three-slab model namely L1, L2 and L3 (Fig. 4.4), assuming that L1, L2, and L3 are the interfacial layer of SiC-SiO_2, bulk SiO_2, and unpassivated and exposed SiO_2 out most layer, respectively (inset of Fig. 4.5).

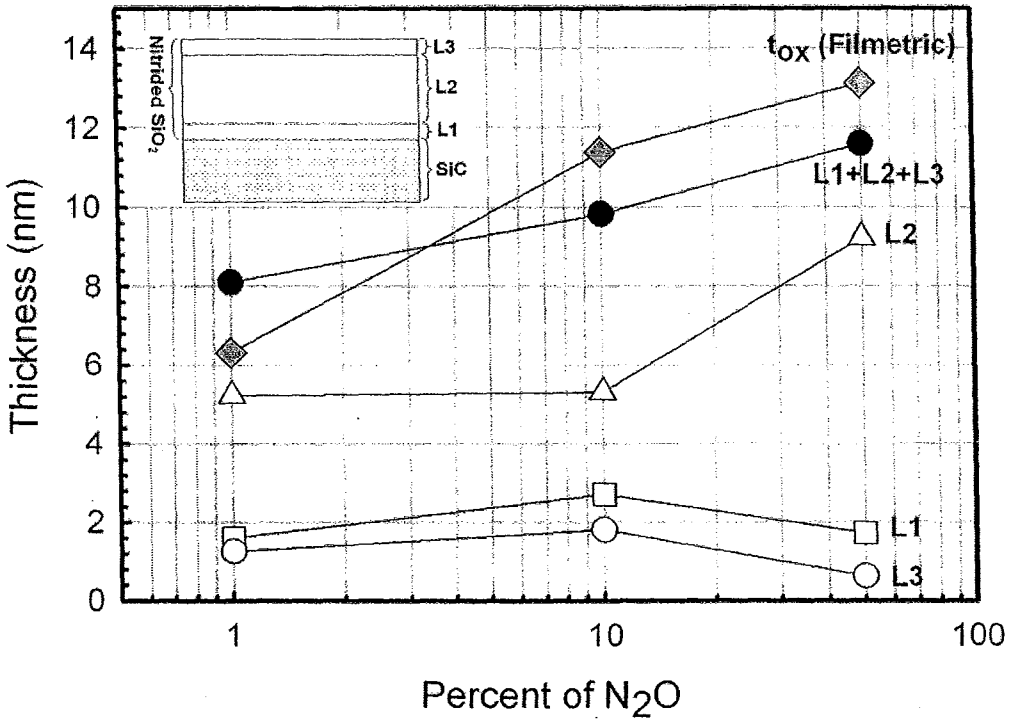

Fig. 4.5: Simulated thickness of respective oxide layers. Inset of the figure shows the notation used.

The t_{ox} is assumed to be the addition of the L1, L2, and L3. The fitted t_{ox} is in agreement with the thickness measured by Fourier and Filmetric measurement (Fig 4.5). L1, which is the closest to the SiC substrate, is an interfacial layer between the substrate and bulk nitrided oxide. The interfacial-layer thickness is approximately 2-nm thick and it is in agreement with the reported value [23]. The thickest L1 is recorded by 10%-N_2O grown oxide, whilst the thinnest is grown in 1% N_2O. The thickness of L1 is associated with a transition layer that is consisted of Si oxycarbide, oxynitride and nitride. The density of this layer has been estimated (Fig. 4.6) and it has revealed that 10%-N_2O grown oxide has the highest density (3.24 g/cm^3) if compared with others. Its density is in

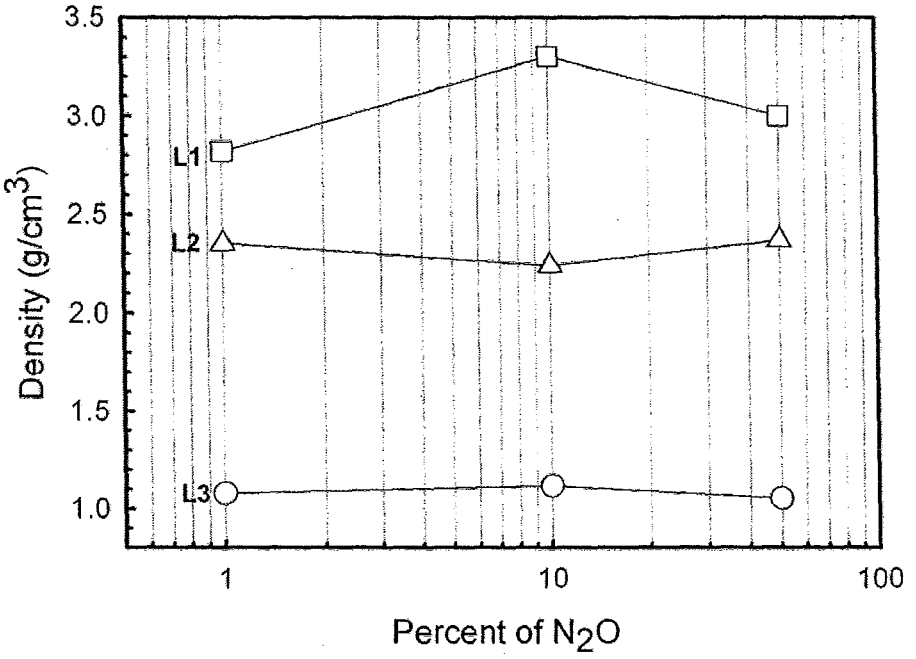

Fig. 4.6: A comparison of oxide density as a function of N_2O percentage.

The cumulative failure percentage of hard oxide breakdown field (E_{HDB}) has been calculated (Fig. 4.8). E_{HDB} is defined as an instantaneous increment of J at a specific E and caused a permanent oxide failure. A total of 25 capacitors has been evaluated for this time-zero dielectric breakdown reliability test. It is obvious that oxide grown in 50% N_2O has demonstrated the highest reliability. In order to understand these observations, various current conduction mechanisms through the oxides have been analyzed using linear curve fitting method [21].

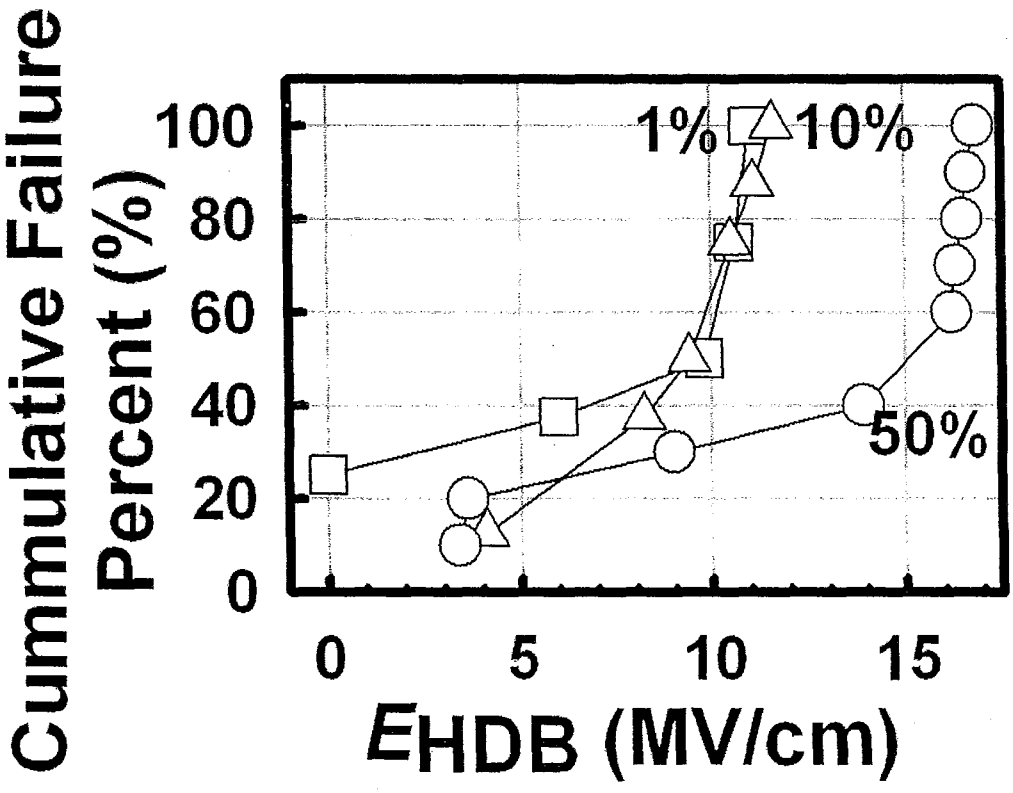

Fig. 4.8: Cumulative failure percentage of hard oxide breakdown field (E_{HDB}) of the three investigated oxides.

generation of free carriers located in the bulk oxide. The density of this carriers is much larger than the density of injected electrons from SiC substrate due to the applied electric field. At higher E, TFL mechanism is occurred as more injected electrons are supplied and they are able to be captured in trap centres located in the bulk oxide. As E is further increases, *trap-free* space charge limited or Child's Law is governing the conduction mechanism. From these three limiting mechanisms, parameters n_0, μ, trap density (N_t), and capture cross section of traps (σ) were calculated [22]. The n_0 value of 10%-N_2O grown oxide is slightly higher ($7.5x10^{12}$ cm^{-3}) than others (1% N_2O = $5.3x10^{12}$ cm^{-3}; 50% N_2O = $4.3x10^{12}$ cm^{-3}) but its μ is lower (1, 10, and 50% N_2O is 7.9x, 4.0x, and $9.4x10^{-13}$ cm^2/Vs, respectively) and σ is smaller (1, 10, and 50% N_2O is 5.7x, 3.5x, and $6.1x10^{-21}$ cm^2, respectively) than the rest. The order of magnitude obtained from this calculation is acceptable if one is assuming that the conductivity of a fused SiO_2 is in the order of 10^{-18} $(\Omega cm)^{-1}$ and the carrier density, n, is in the order of 10^{12} cm^{-3}, by applying, the charge mobility, μ (μ=conductivity/qn) in an *insulator* is in the order of 10^{-12} cm^2/Vs. The calculated capture cross section of trap is also reasonable as it is in agreement with those reported by others [21].

In this work, the calculated N_t value obtained from this investigated electric field range is comparable ($2.0x10^{13}$ cm^{-3}) for all oxides. Even though, 10% N_2O grown oxide is having a relatively high n_0, its ability to move freely is limited as shown by its lower mobility value. Therefore, it is showing the lowest current density if compared with others. The N_t values for TFL and Child's Law controlled mechanisms are comparable for all oxides but the σ value is approximately two times smaller in 10%-N_2O grown oxide; suggesting that the trapping and de-trapping of electron is more difficult. This may partly

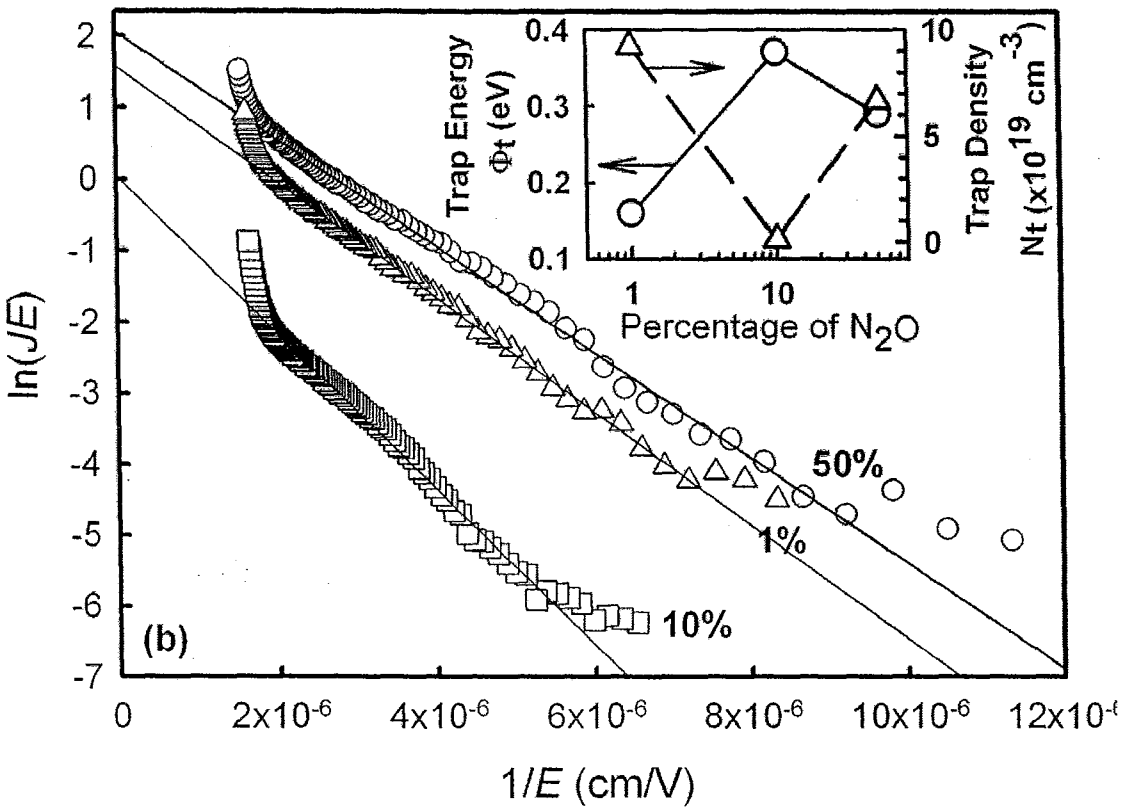

Fig. 4.10. Trap-assisted tunneling (TAT) plot of the three investigated oxides and the inset shows the trap energy (Φ_t) and trap density (N_t) as a function of N_2O percentage.

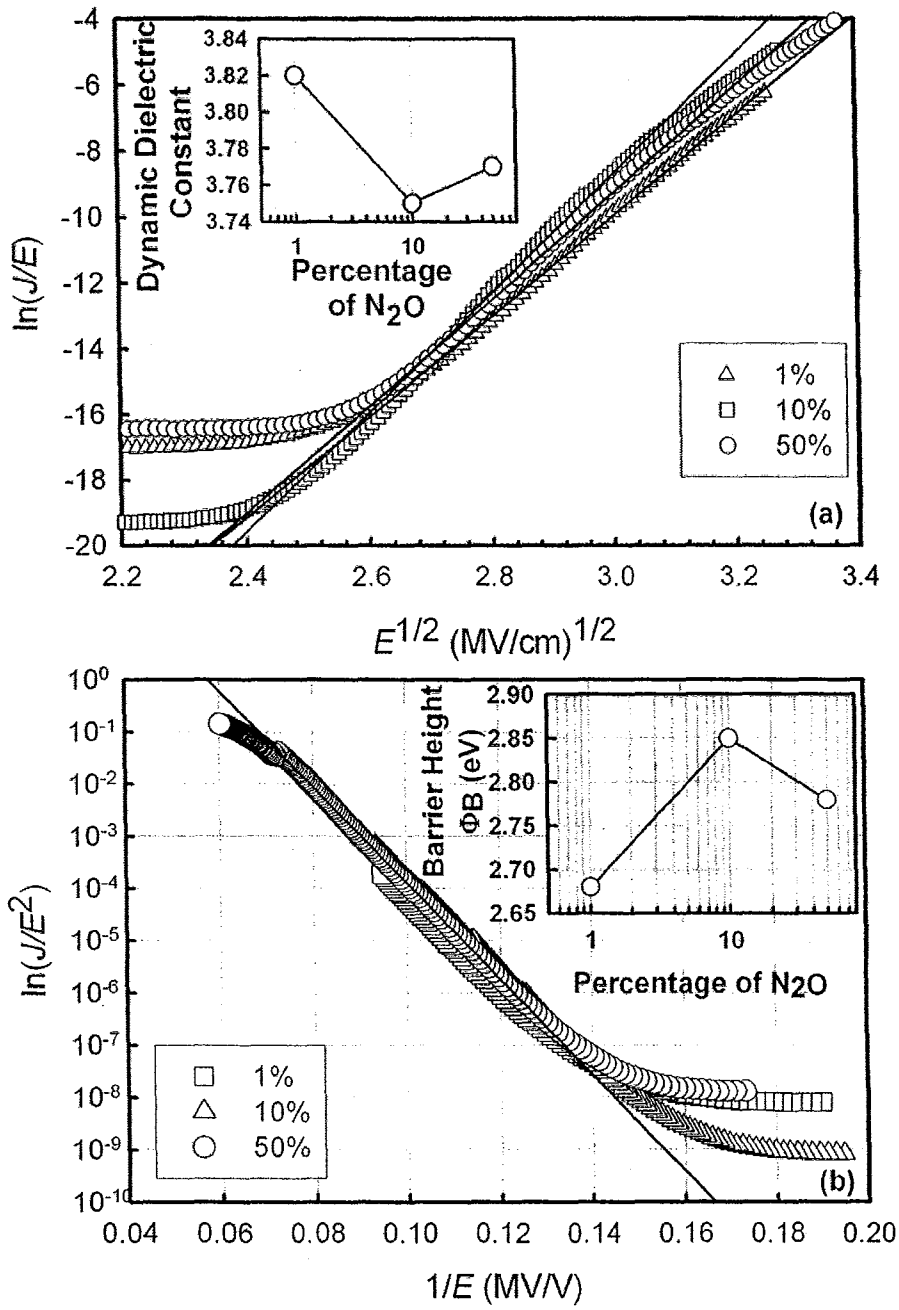

Fig. 4.11. (a) A comparison of Poole-Frenkel (PF) emission plot of the three investigated oxides. Inset of the figure shows the extracted dynamic dielectric constant (k_{dyn}) as a function of N_2O percentage. (b) Fowler-Nordheim (FN) tunneling plot of the three investigated oxides and the estimated barrier height (Φ_B) is presented in the inset of the figure.

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contacts. The fabricated device was characterized using capacitance-voltage (C-V) and current-voltage (I-V) approaches with computer aided measurement system. On the other hand, the morphology of the oxide was inspected under a high power microscope and Carl Zeiss 40VP Field Emission Scanning Electron Microscope (FESEM), while the composition was analyzed using an Inca Energy Dispersive X-ray (EDX) and Seiko SEA1000A Energy Dispersive Fluorescent X-ray Analyzer.

5.3 RESULTS AND DISCUSSION

The wafer thickness t was measured as 0.430 mm using a Digimatic Micrometer. Through a four-point-probe, voltage V and current I of the wafer were found to be 11.40 mV and 1 mA, respectively. By using the relationship [4]

$$Rs = 4.53 \times (V/I) \qquad (5.1)$$

the sheet resistance of the wafer, Rs was obtained as 51.642 V/A. By substituting the values of Rs and t into [4]

$$\rho = Rst \qquad (5.2)$$

the resistivity of the wafer, ρ, was calculated to be 2.22 Ωcm.

A thin layer of oxide with an area of 5 x 5 mm^2 and thickness of 25 nm was deposited on GaN. The outlook of the completed GaN-based MOS devices is shown in Fig. 5.1 and its cross section view is depicted in Fig. 5.2. Fig. 5.3 and Fig. 5.4 illustrate the compositions of the GaN film and the oxide layer, respectively. The weight percentages of Si and O acquired from quantitative analysis (Table 5.1) are 19.37 % and 41.29 %, respectively, giving Si-to-O ratio of approximately 1:2. This implies that the deposited oxide layer is SiO_2.

Table 5.1: Quantitative analysis result of sol-gel derived SiO_2 on GaN.

Element	Line	App. Conc	k ratio	Intensity corrn.	Weight%	Weight% sigma	Atomic%
C	K_SERIES	1.02	0.0047	0.6232	9.23	0.52	16.20
N	K_SERIES	0.35	0.00353	0.4196	4.76	0.66	7.16
O	K_SERIES	11.74	0.04214	1.6072	41.29	0.60	54.43
Si	K_SERIES	3.50	0.02819	1.0197	19.37	0.36	14.54
Ga	L_SERIES	3.30	0.03093	0.7338	25.36	0.50	7.67
Totals					100.00		

Our study obtained a fixed oxide charge density of 3.0×10^{9} cm^{-2}, which is approximately 100 times lower than the one reported by other researchers (6.8×10^{11} cm^{-2}) [1]. As the name implies, this charge is fixed and cannot be charged or discharged over a wide variation of surface potential during electrical test. Hence, it is believed that this relatively lower fixed oxide charge density is contributed by the proper annealing treatment process [5].

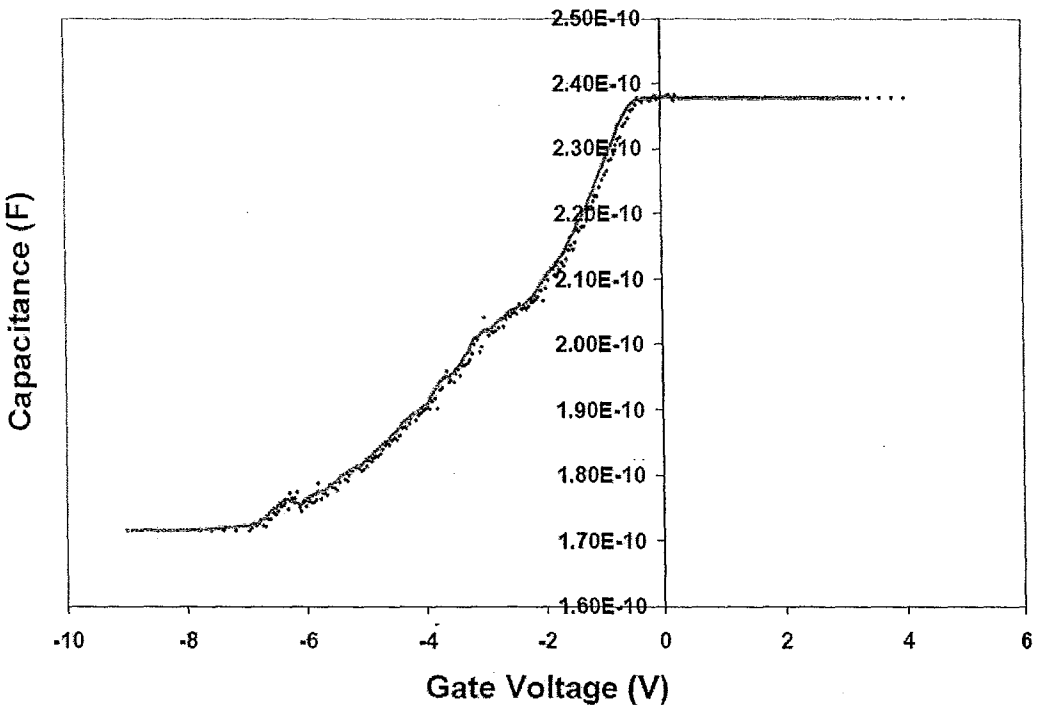

Fig. 5.5: Capacitance-voltage characteristic of the MOS device.

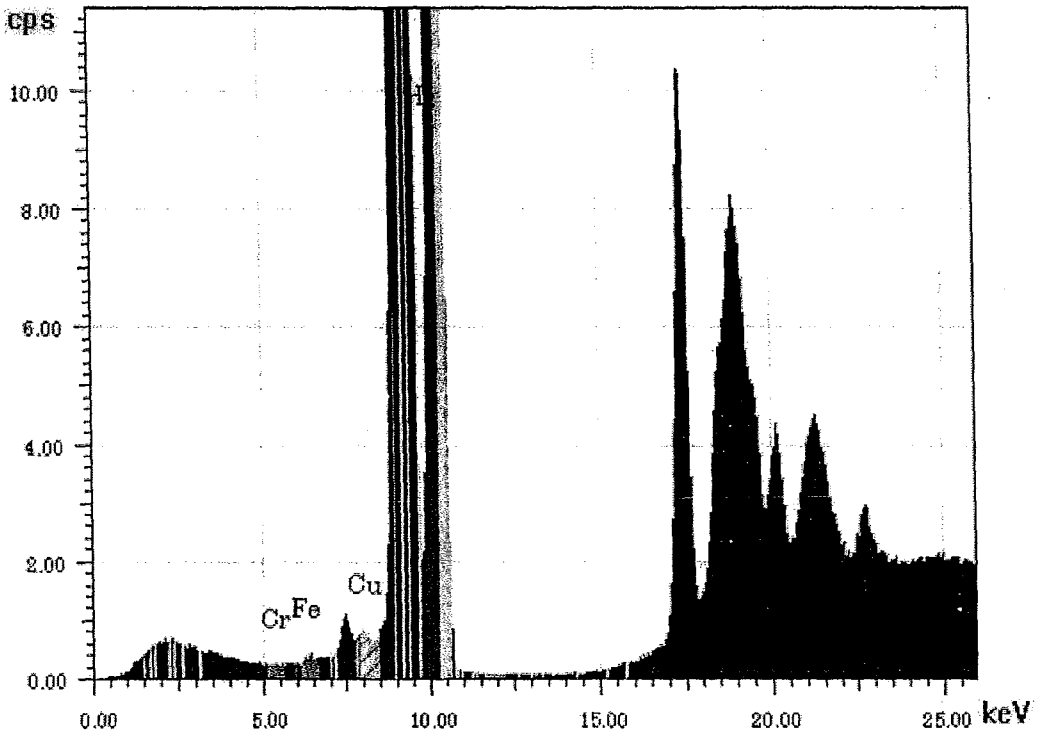

Fig. 5.6: Concentration vs. energy for the metallic charges detected by Energy Dispersive Fluoresent X-Ray Analyzer in the oxide layer.

I-V characteristic of the device is shown in Fig. 5.7. At lower biasing voltages, current is independent of gate voltage. This is complied with the theory that no carriers transport through the oxide under dc biasing. Nevertheless, it is noticed that the leakage current increases abruptly at higher voltages ($\geq$ 3V). With bare eyes, the oxide structure looks fine. However, when viewed under high power microscope and FESEM, it is found that the grown oxide layer is inhomogeneous. In other words, at certain areas the GaN surface is not covered by oxide and thus it is exposed to the air (Fig. 5.8 & Fig. 5.9). Therefore, current might leak from GaN to Al through these flaws during high voltage biasing, causing rise in gate leakage current. Fig. 5.3 reveals that Ga and N are the only two elements that are existed on the wafer surface

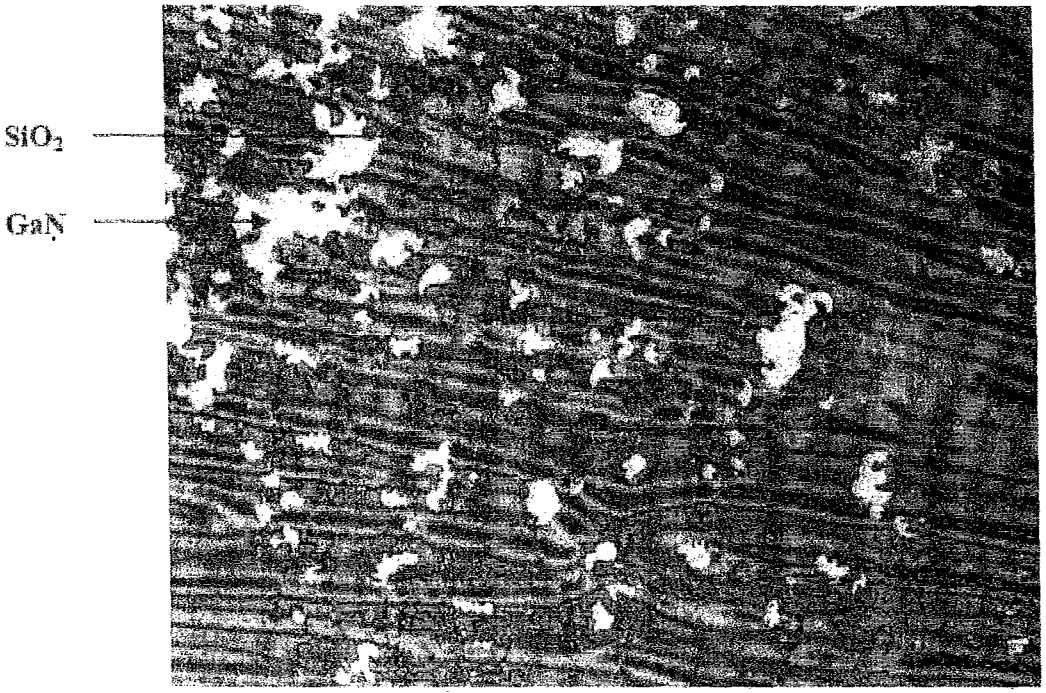

Fig. 5.8: Optical image of the deposited SiO_2 (50x).

Fig. 5.9: SEM image of the deposited SiO_2 (50 x).

CHAPTER 6

CONCLUSIONS

In this work, we have reported the effects of nitrided oxide thickness (t_{ox}) on SiC-based MOS characteristics. A cyclic trend of Q_{eff} and N_{it} as a function of t_{ox} has been observed. Correlation of these parameters with E_B and current transport mechanism in the oxide has been established and reported.

In addition, analysis of charge-conduction mechanism in thermally grown nitrided SiO_2 with different thicknesses on n-type 4H SiC has been systematically performed and reported. Ohm's law, trap-filled-limited, Poole-Frenkel emission, and Fowler-Nordheim tunneling have been identified as the potential current leakage paths in the oxides with various thicknesses (2-20 nm). A relationship plot among oxide thickness, electric field, and type of conduction mechanism has been established.

The effects of vacuum annealing at different temperatures (650 – 950 °C) on the physical properties of thermally grown nitrided-SiO_2 on n-type 4H SiC were also investigated. Weakening of Si-O-Si bonding was detected from FTIR analysis as the annealing temperature was increased. The increase in annealing temperature also attributed to the increase of oxide thickness and to the gradually reduction of refractive index. Similarly, a reduction trend had been recorded in the calculated oxide density and dielectric constant as a function of annealing temperature. However, the oxide porosity was increased as the temperature increased. These may be associated with the weakening

resulting in current leakage under high electrical bias. It is thus proposed that, deposition of dielectric materials onto the GaN surface, which is produced via sputtering process, is preferable to achieve more homogeneous and superior dielectric properties in GaN-based MOS device.

Effects of thermal nitrided gate-oxide thickness on 4*H* silicon-carbide-based metal-oxide-semiconductor characteristics

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The effects of thermal nitrided gate-oxide thickness on *n*-type 4*H* silicon-carbide-based metal-oxide-semiconductor characteristics have been reported. Seven different thicknesses of oxide (t_{ox}), ranging from 2 to 20 nm, have been investigated. It has been shown that effective oxide charge (Q_{eff}) and total interface-trap density (N_{it}) have demonstrated a cyclic trend as t_{ox} is increased. These observations have been explained in the letter. Correlations of Q_{eff} and N_{it} with oxide breakdown field and current transport mechanism in these oxides have also been established and explained. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2430308]

Thermal nitrided silicon dioxide (SiO_2) has been widely accepted as the best quality gate oxide used in silicon carbide (SiC) based metal-oxide-semiconductor (MOS) devices.[1–4] With this gate oxide, it enables SiC to be used as a substrate for MOS-based devices in high power, high-frequency, high temperature, and nonvolatile memory applications.[5,6]. In these applications, thickness of the nitrided oxide (t_{ox}) is different due to the difference in their device structures and requirements. It may range from *ultrathin oxide*, commonly used as a buffer insulator in gas sensor [t_{ox}=1.5 nm (Ref. 7)] and in stacking high dielectric-constant gate ($t_{ox}<8$ nm),[8] to *thin oxide* as the gate insulator for nonvolatile memory devices (12 nm$<t_{ox}<$20 nm),[9] and to *thick oxide* as the gate insulator for high power metal-oxide-semiconductor field-effect transistor (50 nm$<t_{ox}<$70 nm).[5] Currently, most of the studies on nitrided oxide are concentrating on thin-oxide region approximately 12–22 nm. Using this knowledge, the quality of ultrathin and thick nitrided oxide is assumed to be the same as the thin oxide. However, according to the Si–SiO_2 system, charge transport mechanism in the oxide, oxide breakdown field, and oxide reliability are strongly dependent on the oxide thickness, while flatband voltage (V_{FB}) and interface-trap density (D_{it}) are not.[10,11] Therefore, the assumption used in SiC–SiO_2 system is questionable and it is extremely important to investigate in depth the dependence of oxide quality on its thickness. In this work, a systematic investigation on the effects of thermal nitrided SiO_2 thickness (focusing on $t_{ox}\leqslant$20 nm) on SiC-based MOS characteristics has been conducted and its intriguing results are presented in this letter. From this study, the correlation of effective oxide charge (Q_{eff}) and *total* interface-trap density (N_{it}) with oxide breakdown field (E_B) and current transport mechanism in the oxide has been established.

n-type, 8° off (0001) oriented, 4*H*-SiC wafers with 10-μm-thick epilayer doped with $(1-4)\times10^{16}$ cm^{-3} of nitrogen were used to fabricate the MOS-capacitor test structures. After undergoing a standard wafer cleaning process, seven different thicknesses of thermal nitrided SiO_2, ranging from 2 to 20 nm, were grown on the wafers in a horizontal tube furnace with 10%-N_2O ambient at 1175 °C. The samples were loaded in the furnace at 1175 °C. The oxidation/nitridation time was adjusted to obtain the required t_{ox}. After the oxide growth, the furnace was cooled down to 800 °C in high-purity N_2, approximately at 10 °C/min, before the samples were removed. Subsequently, aluminum was sputtered on the oxides to form gate electrodes. The areas for the MOS capacitors were then defined by photolithography. Finally, a large area of aluminum back contact was sputtered on the n^+ substrate. Postmetallization annealing was not performed, so as to avoid masking the effects of the oxides. The subsequent methods of characterizations and extractions of Q_{eff}, D_{it}, N_{it}, and E_B have been described elsewhere.[4,12]

Figure 1 shows the results of t_{ox}, with two distinguished regions labeled as A and B, as a function of oxidation/nitridation time t. Region A demonstrates a linear oxide

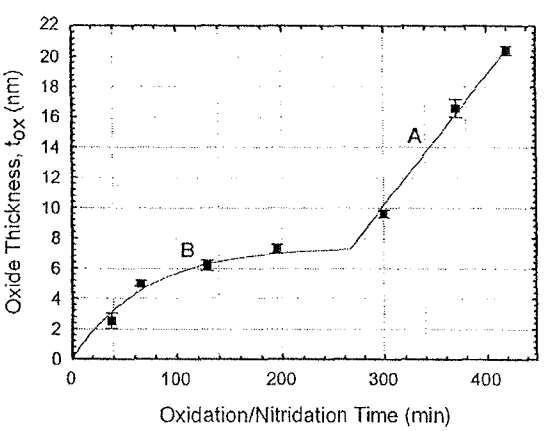

FIG. 1. Thermal nitrided SiO_2 thickness as a function of oxidation/nitridation time. The thickness has been extracted from accumulation capacitance of high-frequency capacitance-voltage curves. Three samples from each thickness have been investigated and the capacitor area of the samples is 1.30×10^{-3} cm^2. The solid line in region B has been fitted using the model presented in (1).

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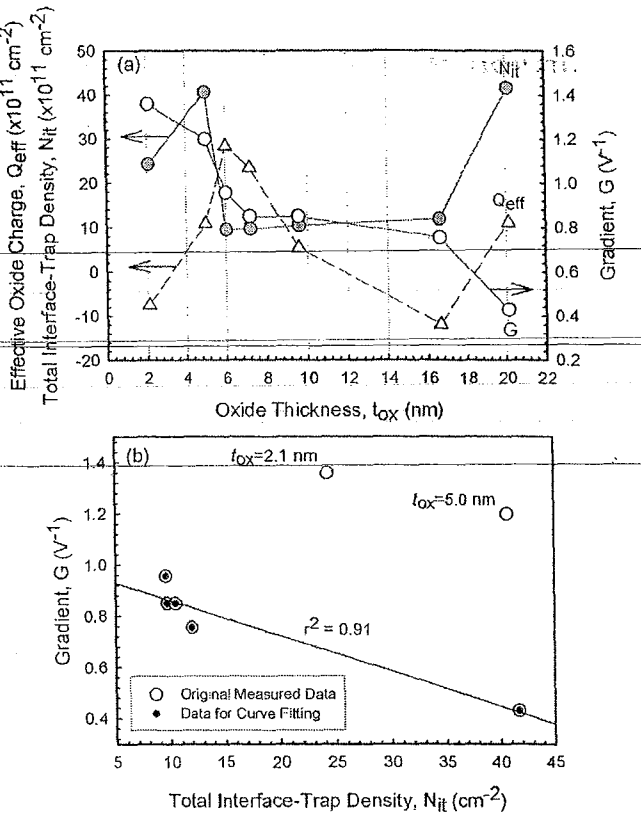

FIG. 2. (a) Effective oxide charge (Q_{eff}), total interface-trap density (N_{it}), and gradient of high-frequency capacitance-voltage curve from flatband to depletion capacitance (G) as a function of oxide thickness. The various types of lines are used to guide the eyes. N_{it} is obtained from the area below the plots of D_{it}-(E_C–E), where E_C and E are the conduction band-edge and interface trap level, respectively. The D_{it} is measured by simultaneous high-low C-V method. (b) A Correlation graph between the gradient and total interface-trap density. The coefficient of determination r^2 is shown in the plot to represent the goodness of the fitted data. Data from t_{ox}=2.1 and 5.0 nm were not used for the linear curve fitting.

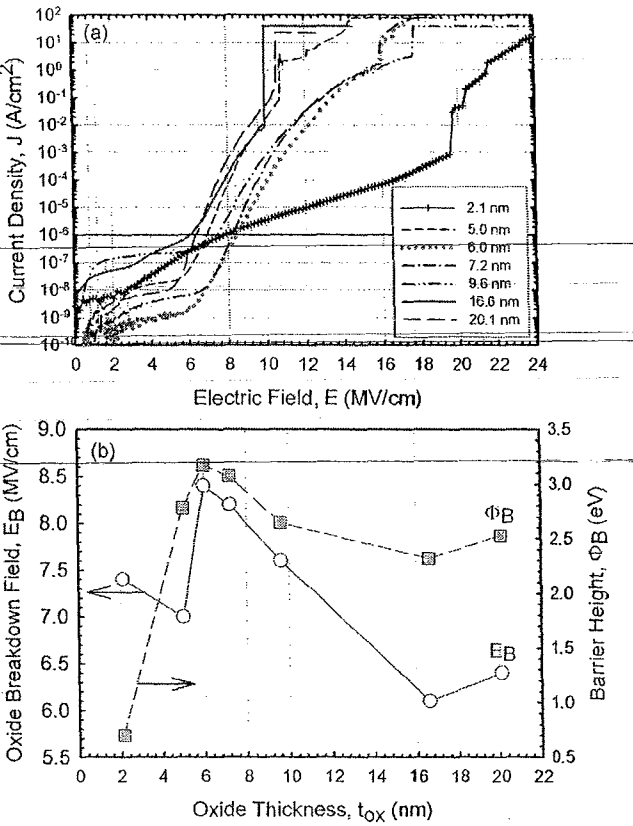

FIG. 3. (Color online) (a) Comparison of current density-electric–field-plots of the investigated samples with different oxide thicknesses. (b) Oxide breakdown field and barrier height as a function of oxide thickness. The solid and dash lines are used to guide the eyes.

growth with a rate constant of 5.2 nm/h, which is comparable with the literature (~6.0 nm/h).[13] However, for $t_{ox}<8$ nm (region B), the linear growth of the oxide has been suppressed by an accelerated initial oxide growth.[14] The combination of these two growth rates (dt_{ox}/dt) in this ultrathin region can be well fitted in the following model:[14]

$$\frac{dt_{ox}}{dt} = C + a_0 e^{-t/\tau} e^{-E_A/kT}, \tag{1}$$

where the first and second terms are representing the linear-(C) and initial-rate constants, respectively. a_0, τ, E_A, k, and T are constant, time constant, activation energy, Boltzmann's constant, and temperature, respectively. The linear-rate constant in this region (5.4 nm/h) is very close to the value obtained in region A, by considering E_A=2.8 eV (Ref. 13) T=1448.15 K, and no oxide is grown at t=0 min. The extracted τ value is 65.8 min^{-1} and it is associated with the time needed to produce an equilibrium oxide thickness.[14]

A cyclic trend of Q_{eff}, changing from $-Q_{eff}$ to $+Q_{eff}$, as a function of t_{ox} has been shown in Fig. 2(a). Similarly, results of N_{it} (total D_{it} from 0.2 to 0.7 eV below conduction band edge of 4H-SiC) as a function of increased t_{ox} is also demonstrating a cyclic trend. These observations are different from those reported in Si–SiO2 system,[10,11] as there is an extra alternative layer of carbon in SiC that will be removed during nitridation process. During initial oxidation (t_{ox}=2–5 nm), carbon is probably accumulated at SiC–SiO_2 interface (increasing trend of N_{it}) and a nonequilibrium and disordered oxide is grown. When t_{ox} increases, the accumulated carbon at the bulk and interface is reduced as the oxidation and nitridation processes are in equilibrium. However, the reduction has a limitation. As the t_{ox} increases further, the well passivated interface has to be depassivated in order for the subsequent oxidation to proceed. The forming and breaking of the bonds may affect arrangement of the bulk SiO_2 network. As a result, Q_{eff} again demonstrated a negative value. This cycle continues as the oxide gets thicker and thicker.

In Fig. 2(a), the changes of gradient G of high-frequency capacitance-voltage curves from flatband to depletion capacitance of the oxides have been extracted. Commonly, G is qualitatively associated with N_{it}. The higher the G value, the lower the N_{it}. However, in this work, we have demonstrated that it is not valid for samples with $t_{ox}<6$ nm [Fig. 2(b)].

The effect of t_{ox} on current transport mechanism has been presented in current density (J)-electric field (E) plots [Fig. 3(a)]. Any E that enables $J \geq 10^{-6}$ A/cm^2 is defined as oxide breakdown field E_B. This parameter as a function of t_{ox} is presented in Fig. 3(b). From the shape of the J-E plot, one can conclude that the current transport mechanisms in the investigated oxides are the same except for those with the thinnest oxide. Fowler-Nordheim (FN) and direct tunnelling (DT)[11] are the major conduction paths of electron injecting

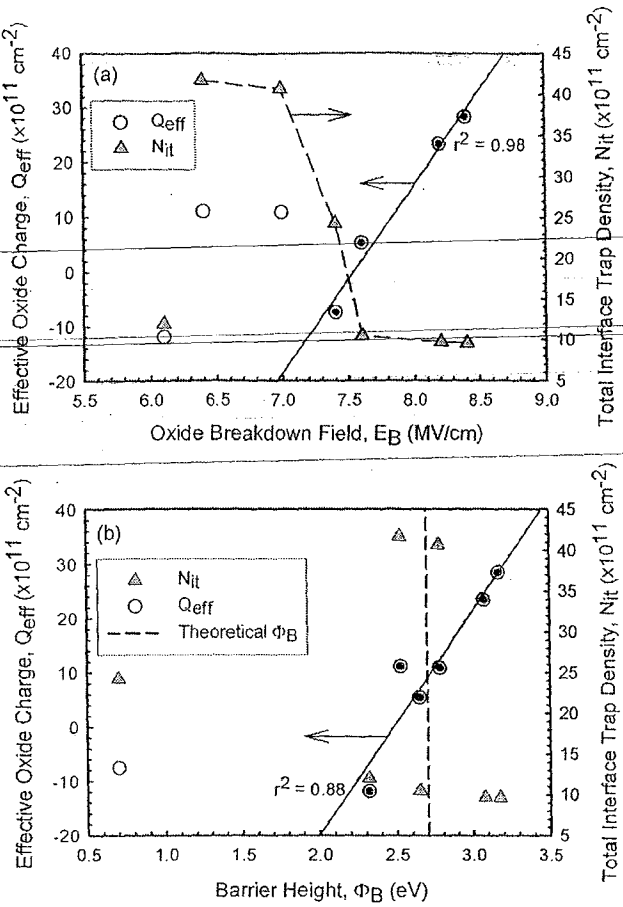

FIG. 4. Correlation graphs of (a) oxide breakdown field and (b) barrier height with effective oxide charge and total interface-trap density. The coefficients of determination r^2 are shown in the plots to represent the goodness of the fitted data. Data used for the linear curve fitting are indicated by solid filled circles.

from SiC substrate through the oxide with $t_{ox}>2.1$ nm and $\leqslant 2.1$ nm, respectively. From FN plots, barrier heights Φ_B between conduction band edge of SiC and nitrided oxide as a function of t_{ox} have been extracted [Fig. 3(b)]. The extremely small value of Φ_B obtained from $t_{ox}=2.1$ nm is another good indicator showing that the current conduction mechanism in this oxide in not dominated by FN, but by others (here we have proven that it is via DT). The effects of t_{ox} on these parameters (E_B and Φ_B) can be correlated with Q_{eff} and N_{it} and it will be discussed in the following paragraphs.

Figure 4(a) shows the correlation graph of E_B with Q_{eff} and N_{it}. A good correlation of E_B with Q_{eff} has been established for $7.4\leqslant E_B\leqslant 8.5$ MV/cm. It has been suggested that Q_{eff} is the dominating factor affecting the E_B value at this range. As Q_{eff} value becomes more positive, more injected electrons from SiC substrate are able to be captured and trapped in the positive trap centers rather than use to break the network of bulk SiO_2. These trapped centers are neutralized by the electrons so that more electrons are required for the oxide breakdown process and attributed to the increase of E_B. In addition to that, the reduction of N_{it} also enables the oxide breakdown strength to be improved, in particular, for $6.5\leqslant E_B\leqslant 7.6$ MV/cm. However, N_{it} has become a secondary factor for the improvement at $7.6\leqslant E_B\leqslant 8.5$ MV/cm if compared with Q_{eff}. For $E_B\leqslant 6.5$ MV/cm, further investigation is needed to identify which factors are affecting the oxide breakdown process as no concrete evidence has been demonstrated in this work.

The correlation graph between Φ_B and Q_{eff} has been established in Fig. 4(b). The Φ_B value that is associated with sample having $t_{ox}=2.1$ nm was ignored in this establishment, as it was not a reliable value. Those samples with $Q_{eff}=(5-10)\times 10^{11}$ cm^{-2} are having Φ_B values comparable with the theoretical one (2.7 eV).[15] When Q_{eff} value becomes more positive, Φ_B is increased. In contrast, Φ_B is lowered when negative Q_{eff} is obtained in the sample. These observations are agreeable to the theory suggested in $Si-SiO_2$ system, where the effective positive charge in the bulk may convert into neutral electron traps and the effective negative charge in the bulk may increase the number as electrons are injected via FN tunneling.[11,16] In the figure, a correlation between N_{it} and Φ_B was not established. Therefore, we conclude that Φ_B value is only strongly dependent on Q_{eff} and not on N_{it}.

In this letter, we have reported the effects of nitrided t_{ox} on SiC-based MOS characteristics. A cyclic trend of Q_{eff} and N_{it} as a function of t_{ox} has been observed. Correlation of these parameters with E_B and current transport mechanism in the oxide has been established and reported.

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Effects of heat treatment in vacuum on the physical properties of thermal nitrided silicon dioxide gate on 4H-silicon carbide

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Abstract

Nitrided SiO_2 has been thermally grown on n-type 4H silicon carbide substrate. The effects of post deposition annealing temperature (650 to 950 °C) in vacuum on physical properties of the oxides have been reported. Based on Fourier transform infra-red analysis, Si–O–Si bonding of the oxide has been weakened as the annealing temperature has been increased. The increment in annealing temperature has caused the increment in oxide thickness. Refractive index has been measured via Filmetric system and the index has been gradually reduced as a function of annealing temperature. This reduction trend is also being observed in the calculated values of film density and dielectric constant. In contrast, an increment trend has been recorded in film porosity as the annealing temperature increased. These observations may be attributed to the weakening of Si–O–Si bonding in the bulk oxide and roughening of the oxide surface, which has been demonstrated by atomic force microscopy.

Keywords: Vacuum annealing; Nitridation; Surface roughness

1. Introduction

Due to its wide bandgap, silicon carbide (SiC) has become a very promising material for use in high-power, high-frequency, high-radiation-resistant, and non-volatile memory applications [1–3]. Besides, SiC has become a favored material compared to other premier wide-bandgap semiconductors due to commercial availability substrates, known device processing techniques, and ability to grow native oxide that is silicon dioxide (SiO_2) [1,2,4]. In other words, SiC can be produced in much the same way as silicon but with higher processing temperatures. One of the issues in thermally grown SiO_2 is the residual carbon in oxide layer and also carbon cluster at the oxide-SiC interface. It has been found that oxidation or post oxidation in a nitrogen-containing atmosphere has two benefits that are enhanced removal of carbon and passivation of silicon dangling bond in Si-face SiC [5]. In the case of C-face and a-face SiC, hydrogen treatment is preferable [6,7]. Thus, it can be concluded that thermal nitrided or hydrogenated SiO_2 is the best quality gate oxide used in SiC [5–7].

To produce a good and functional metal-oxide-semiconductor (MOS)-based device, the wafer needs to go through numerous processing steps, which normally involve high temperatures and vacuum atmosphere; such as chemical vapour deposition. These processing steps may influence the product produced from the previous process. The effect of post nitridation rapid thermal annealing on the electrical properties of the MOS device has been reported, recently [8]. However, the effect of heat treatment at vacuum on the properties of SiC-based

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nitrided oxide has not been reported. Therefore, in this work, physical properties of the nitrided oxide on 4H SiC have been reported after the oxides have gone through vacuum annealing at different temperatures.

2. Experimental details

Five n-type Si-face 4H-SiC (7 mm × 7 mm) wafer were used as the substrate for the MOS test structures. Nitrided SiO_2 was thermally grown in a diluted N_2O environment at 1175 °C for a fix period, so that the obtained thickness was approximately 15 nm [9]. The flow rate of the N_2O gas was adjusted to 1 L/min. The reason of using N_2O as the nitridation source was due to its non-toxic property. After oxidation and nitridation, one of the samples was used as a control sample whereas the other four were vacuum-annealed (5–6 mTorr) at 650 °C, 750 °C, 850 °C, and 950 °C with a dwelling time of 30 min. The heating and cooling rate for all samples were 15 °C/min and 10 °C/min, respectively. All of the samples were withdrawn from the furnace at temperature around 50 °C.

After post-deposition vacuum annealing, oxide thickness was measured using a Filmetrics F20 Thin-Film Analyzer based on optical refraction principle. A total of four different locations from a same sample were measured. From this measurement, refractive index (n) of the annealed oxides was obtained and percentage of porosity and dielectric constant (k) were calculated. The surface roughness and topography of the top-most oxide layer was analyzed by an atomic force microscope (AFM) (Nano Navi SPI3800N) using a non-contact mode. The AFM has been equipped with a Si_3N_4 cantilever and three-dimensional AFM topographies were recorded on 1 μm × 1 μm scanned area. A total of three different areas have been investigated. The vibrations of individual atoms within the molecules, such as stretching, bending and rocking modes, could be obtained from Fourier transform infra-red (FTIR) analysis using Perkin Elmer Fourier transform infra-red system.

3. Results and discussion

Fig. 1 compares FTIR spectra for oxide with and without vacuum annealing. For all oxides, Si–O–Si stretching band can be detected [10]. It is also noticed that the Si–O–Si stretching

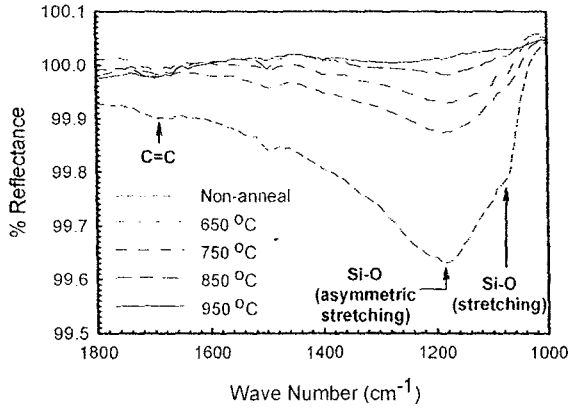

Fig. 1. Fourier transform infra-red spectra of annealed and non-annealed oxides obtained from reflectance mode.

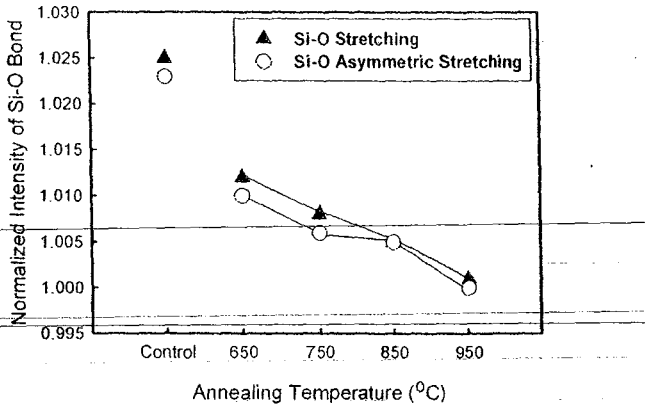

Fig. 2. Normalized intensity of Si–O stretching bond and Si–O asymmetric stretching bond at approximately 1080 cm^{-1} and 1170 cm^{-1}, respectively as a function of annealing temperature.

band is consisted of two bands and are located at about 1080 cm^{-1} and 1100 cm^{-1} [11]. In additional, Si–O asymmetric stretching and C–C stretching bonds are detectable at around 1170 cm^{-1} and 1200 cm^{-1} [10]. As a whole, it can be seen that the intensities of the spectra for every sample are becoming less significant as the annealing temperature is increased. This has been quantitatively shown in Fig. 2, whereby the trend of normalized intensity of Si–O stretching and Si–O asymmetric stretching bonds with respect to the intensity of Si–C bond (at approximately 930 cm^{-1}) is decreasing with the annealing temperature. One of the reasons that may explain this trend is these bonds had become weaker when the samples were exposed to high temperatures.

The measurements of oxide thickness were carried out using a Filmetrics system at a wavelength of 632.8 nm. Other than measuring the thickness of the oxide, Filmetrics was also employed to measure the refractive indices (n) of the samples. Before vacuum annealing was carried out, the initial oxide thickness was 15.3 nm (Fig. 3). However, after being exposed to high-temperatures vacuum annealing, its thickness was increased. The percentage change in oxide thickness was increased slightly until the sample has been annealed at 750 °C.

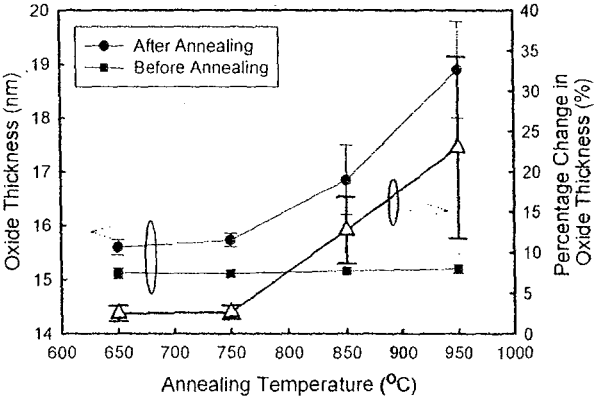

Fig. 3. Effects of vacuum annealing on the changes in absolute and percentage change of oxide thickness. The error bar represents median and standard deviation of the changes in absolute and percentage change of the oxide thickness.

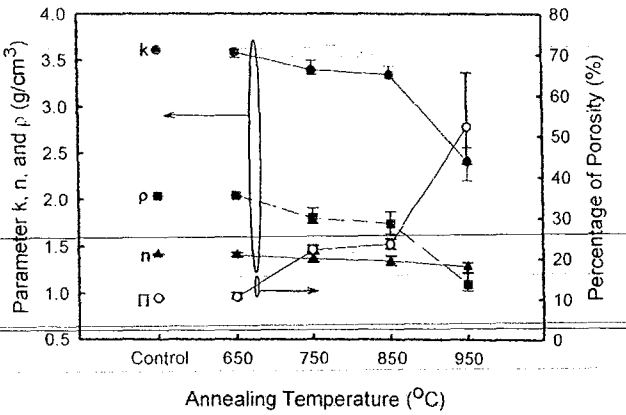

Fig. 4. Effects of vacuum annealing on the refractive index (n), dielectric constant (k), density (ρ), and percentage of porosity (Π) of nitrided thermally grown SiO_2. Unit of Π and ρ are in % and g/cm^3. The error bar represents median and standard deviation of n, k, ρ, and Π.

As the annealing temperature is further increases, the percentage change in the oxide thickness has become significant (Fig. 3).

Fig. 4 shows the refractive index, n, of the samples. Theoretically, the n value of a thermal SiO_2 is 1.46 [12]. However, Fig. 4 shows a slight declining trend with respect to the annealing temperature. This suggested that the surface structure of the SiO_2 film may be changed after being annealed in vacuum. The change of surface structure probably is related to the weakening of Si–O–Si bonding in the bulk oxide. The transformation of surface topography as a function of annealing temperature will be presented in the subsequent paragraph. The density (ρ), porosity (Π), and dielectric constant (k) of the samples can be determined from the measured n value. The ρ value has been calculated using the following relationship [13]:

$$\rho = (n-1)/0.202 \quad (1)$$

From the calculated film density, Π and k values can also be obtained from the following relationships [13]:

$$\Pi = 1 - \rho/\rho_s \quad (2)$$

where Π is the film porosity and ρ_s (thermally grown conventional SiO_2 film)=2.27 g/cm^3 and

$$k = 1 + 1.28\rho \quad (3)$$

The effects of vacuum annealing on the film density and porosity are shown in Fig. 4. The film density and porosity are reduced and increased, respectively, as a function of annealing temperature. The theoretical value of film density for pure SiO_2 is around 2.0–2.3 g/cm^3 [12]. The calculated density values of sample without annealing and annealed at 650 °C are in the theoretical range and the values for other samples are reduced gradually. This reduction is also associated with the increment

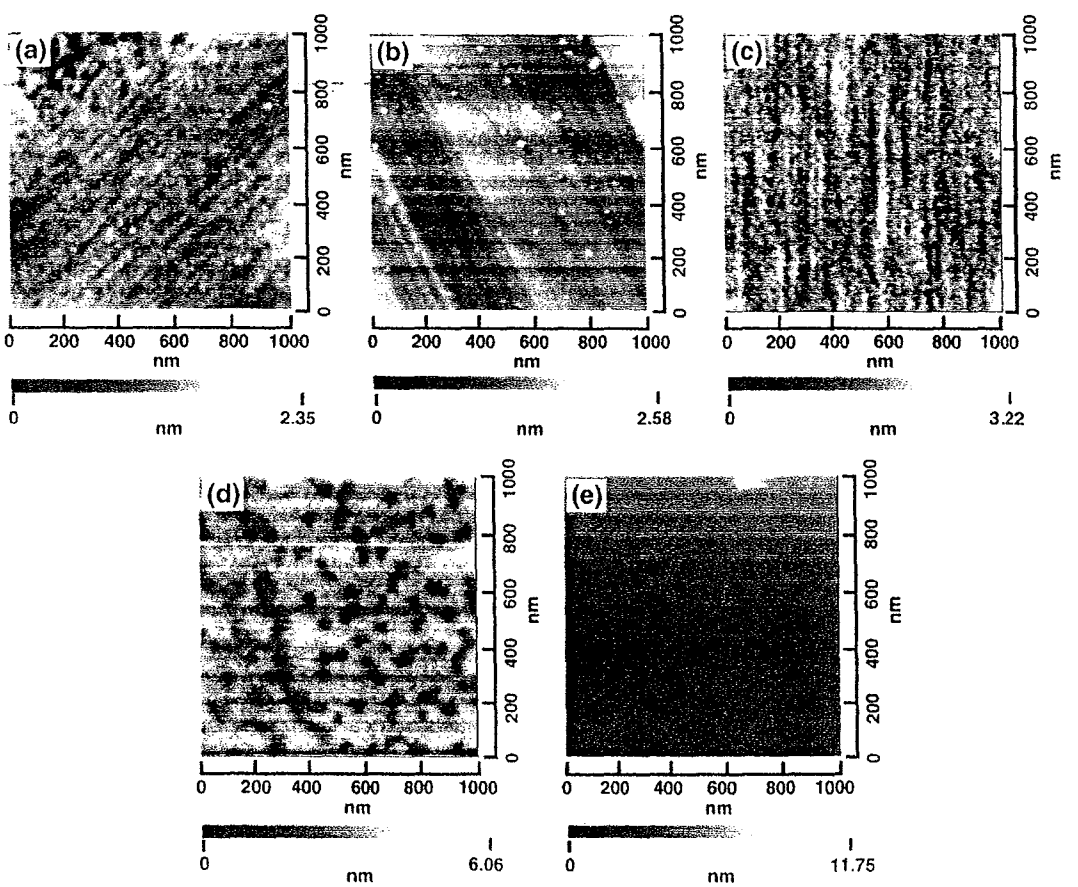

Fig. 5. Two-dimensional surface topography of (a) non-annealed oxide, (b) 650 °C-, (c) 750 °C-, (d) 850 °C-, and (e) 950 °C-annealed oxides.

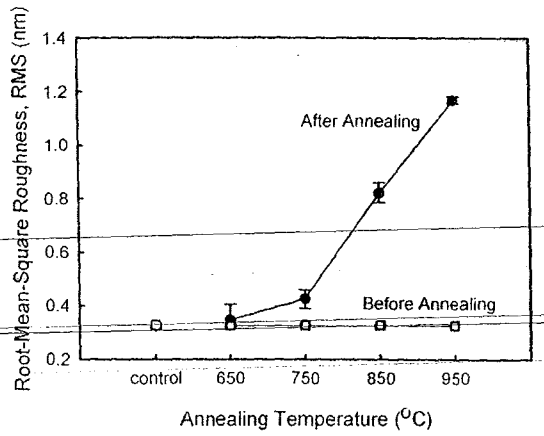

Fig. 6. A comparison of annealed and non-annealed oxide surface root-mean-square (RMS) roughness. The error bar represents median and standard deviation of RMS roughness of the sample surface.

of porosity in the annealed films. The increment of porosity may be attributed to the weakening of Si–O–Si bonding in bulk structure of SiO_2. Fig. 4 also presents the calculated results of k as a function of annealing temperature. Theoretically, the k value of SiO_2 is 3.9 [12]. From the observation, control sample and sample annealed at 650 °C are the two samples that possessed the average k value near to the theoretical value. The k value is reduces as the annealing temperature increases. The physical properties of thermally nitrided oxide formed at 1175 °C have been changed after successive vacuum annealing at lower temperatures. This is similar to those oxides underwent post oxidation or nitridation annealing at lower annealing temperatures in N_2 ambient [14].

AFM has been employed to study the surface topography of the thin films and the changes of surface roughness after annealed at different temperatures. Non-contact mode AFM measurement was used in this analysis in order to avoid sample surfaces from damaging. Typical two dimensional topography of the annealed and non-annealed oxide is shown in Fig. 5. The influence of vacuum annealing on the root-mean-square (RMS) roughness is described. Fig. 6 compares the RMS roughness of oxides before and after vacuum annealing. The initial RMS roughness before annealing was 3.267×10^{-1} nm, which corresponds to a smooth and continuous film surface as shown in Fig. 5a (control sample). As the samples underwent annealing treatment, value of RMS surface roughness has been increased gradually from 650 °C to 750 °C. The surface topography of sample annealed at 650 °C is rather similar to the topography of the control sample, except showing a higher number of protrusions (Fig. 5b). When sample annealed beyond 750 °C, a significant increment in the RMS surface roughness has been observed. This is associated to the increment in number and size of protrusions on the oxide surface as the annealing temperature is increased to 950 °C (Fig. 5(c)–(e)). The increment of RMS roughness as a function of annealing temperature may be attributed to the restructuring of Si–O–Si bonds. This increment is also observed in similar oxide underwent rapid thermal annealing [8].

4. Conclusion

The effects of vacuum annealing at different temperatures (650–950 °C) on the physical properties of thermally grown nitrided-SiO_2 on n-type 4H SiC were investigated. Weakening of Si–O–Si bonding was detected from FTIR analysis as the annealing temperature was increased. The increase in annealing temperature also attributed to the increase of oxide thickness and to the gradually reduction of refractive index. Similarly, a reduction trend had been recorded in the calculated oxide density and dielectric constant as a function of annealing temperature. However, the oxide porosity was increased as the temperature increased. These may be associated with the weakening of Si–O–Si bonding in the bulk oxide and roughening of oxide surface as what had been revealed in surface topography and root-mean-square roughness measurement from AFM.

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Analysis of charge conduction mechanisms in nitrided SiO_2 Film on 4H SiC

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Abstract

Seven different thicknesses (2–20 nm) of nitrided SiO_2 on *n*-type 4H-SiC have been employed to investigate the charge conduction mechanism through these oxides. Several potential mechanisms have been identified. The mechanisms are depending on electric field and oxide thickness. A relationship plot among these three parameters has been established.

Keywords: Fowler–Nordheim tunneling; Poole–Frenkel emission; Electric breakdown field; Space-charge limited

1. Introduction

Silicon carbide (SiC) is a chemically inert, mechanically rugged, electronically superior wide-bandgap semiconductor that enables it to be used as a substrate for high power, frequency, temperature, and non-volatile memory metal-oxide-semiconductor (MOS)-based devices [1,2]. The gate oxide, which is sandwiched in between a gate electrode and the SiC is the dominate factor determining the success of fabricating a functional MOS-based device. This is because the gate oxide, ideally, must be able to block all charges injected either from SiC or gate electrode; so that leakage current through the oxide could be prevented. Up to date, thermally grown nitrided SiO_2 gate has been generally accepted as the best quality gate oxide compared with its counterparts grown by dry or wet oxidation [3–7]. The MOS structure with this type of oxide has demonstrated an ultra low leakage current [8]. The reasons for this and the excellent electronic properties of MOS-based devices with nitrided SiO_2 gate have been widely reported [1–13].

Even though the quality of nitrided SiO_2 is excellent, at high electric field (E), this oxide could break down electrically due to Fowler–Nordheim (FN) tunneling. This is an oxide thickness- and temperature-dependence process and typically this tunneling process is initiated at $E > 6.5$ to 8 MV/cm is SiC-based sample [9]. In additional to this tunneling process, charge-trapping and interface-trap facilitated by FN tunneling may also attribute to oxide breakdown depending on post-nitridation treatment of the oxide and applied electric field [10]. In most literatures, FN-like tunneling has been considered as the only charge conduction mechanism causing the leakage [11–13]. Usually, MOS-based power devices and gas sensors are operated at an electric field not more than 3 MV/cm, this is mainly due to the limitation of the SiC substrate [14,15]. Therefore, the knowledge on leakage current derived from high-electric field (FN-like tunneling) is not suitable to be used to explain the cause of leakages detected in low electric field. Therefore, a systematic investigation must be performed to explore the potential charge-conduction mechanisms occur at low electric field in the nitrided SiO_2 gate. In this Letter, analysis of the mechanisms on *n*-type 4H SiC-based nitrided SiO_2 as a function of nitrided oxide thickness and electric field has been reported.

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2. Experimental procedure

N-type, 8° off (0001) oriented, 4H SiC wafers with 10-μm thick epilayer doped with (1–4) × 10^{16} cm^{-3} of nitrogen were used to fabricate the MOS-capacitor. Seven different oxide thicknesses (t_{ox}) (2.1, 5.0, 6.0, 7.2, 9.6, 16.6, and 20.1 nm) of thermal nitrided SiO_2 were grown on pre-cleaned wafers in a tube furnace under 10%-N_2O ambient at 1175 °C. The oxidation/nitridation time was adjusted to obtain the required t_{ox}. After the oxide growth, the furnace was cooled down to 800 °C in high-purity N_2, a layer of aluminum was then sputtered on the oxides to form gate electrodes. The subsequent MOS-capacitor fabrication process has been described elsewhere [4]. *A Semiconductor Parameter Analyzer* (HP-4156) was used to measure leakage current of the MOS capacitor with an area, A, of 1.30 × 10^{-3} cm^2 at various temperatures (25–140 °C). The gate current (I_G) as a function of forward gate-voltage sweep, V_G (ramping rate = 0.3 V/s) was recorded. The results of MOS characteristics as a function of nitrided SiO_2 thickness have been reported earlier [9].

3. Results and discussion

The results of I_G as a function of V_G for different t_{ox}, measured at room temperature, have been reported in Ref. [9]. Fig. 1(a) shows a typical plot of current density, J, ($J = I_G/A$) as a function of electric field, E, [$E \cong (V_G - V_{FB})/t_{ox}$] for some of the investigated oxides, which have been fitted with Ohm's law [$J_{Ohm} = qn_0\mu E$] and trap-filled limit (TFL) [$J_{TFL} = BE^m$] process. The symbols J_{Ohm}, J_{TFL}, V_{FB}, q, n_0, μ, B, and m are current density governs by Ohm's law, current density governs by TFL process, flatband voltage, electronic charge, density of thermal generated free carriers, electronic mobility in the oxide, a constant, and a trap distribution and temperature related constant [16]. These are the two out of three conduction mechanisms governing a space-charge limited (SCL) process. From the curve fitting results, the third SCL mechanism—Child's law—was not revealed in all of the oxides. The gradient, S, of the J–E plots obtained from the above two mechanisms are presented in Fig. 1(b). The legends "Ohm's (1)", "TFL", and "Ohm's (2)" in the figure refer to the governing conduction mechanism by Ohm's law at initiate electric field, follows by trap-filled limit, and subsequently take over again by Ohm's law. This observation was only limited to oxides with thickness of 5.0 and 9.6 nm. The dominate conduction mechanism of the remaining oxide thicknesses is either by Ohm's law or Ohm's law followed by TFL process. It is clear that the extracted S values from Ohm's law as a function of t_{ox} are closed to its theoretical value of 1. For current conduction obeying Ohm's law, at this extremely low electric field, the density of thermally excited electrons from trap centres located at bulk oxide is much larger than the density of injected electrons from SiC. This is because, at this electric field, electrons from semiconductor are unable to be injected into the oxide, even through its concentration is much higher than concentration of trapped electron. Since, this is happened in an electrically quasineutral state, the empty

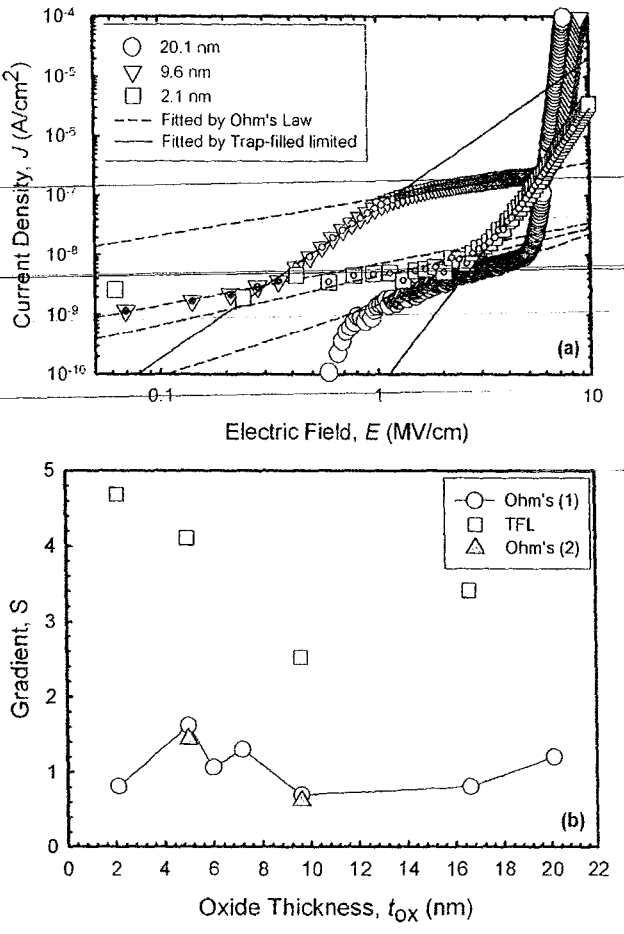


Fig. 1. (a) Plot of current density, J, as a function of electric field, E, measured from MOS capacitor with different nitrided SiO_2 thickness. Solid symbols represent data points for Ohm's law and trap-filled limited process fitting. (b) Gradient, S, of J–E plot in (a) as a function of t_{ox}.

traps are unable to be filled by any weak injected electron from SiC. Therefore, the detected leakage current density from this conduction mode is ultra-low [Fig. 1(a)] [17]. As E is further increased, more electrons are able to be supplied and injected from SiC. The injected electron may be captured in trap centres located at the bulk oxide. When trapping of electron happens, TFL process, which is a charge compensation-free is started to reveal. The electric field that enables the electron-trapping process is refers to E_{on}. As the electric field is further increases, more electrons are being injected into trap centres located deeper below Fermi level. This trapping process is continue until all of the deep traps are completely filled. At a higher electric field, no further electrons are able to be trapped. The extracted S value from the TFL process is between 2 and 5 [Fig. 1(b)]. At E_{on}, transit time of electron (τ_e) is equal to the relaxation time of dielectric and it is estimated by $\tau_e = \varepsilon(E/J)$, where ε is the dielectric constant of oxide and E/J is the inverse gradient of J–E plot for Ohm's law. The τ_e values estimated are in the ranging of (1.8–5.0) × 10^{-7} s, depending on the oxide thickness. By knowing the value of τ_e and E_{on}, the value of μ ($\tau_e = t_{ox}/\mu E_{on}$) could be computed.

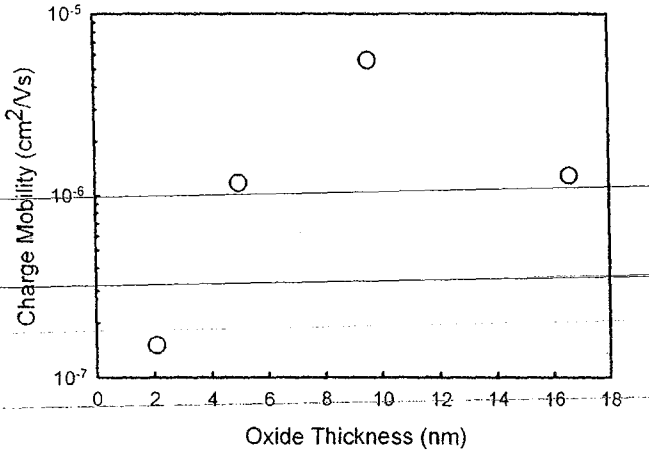
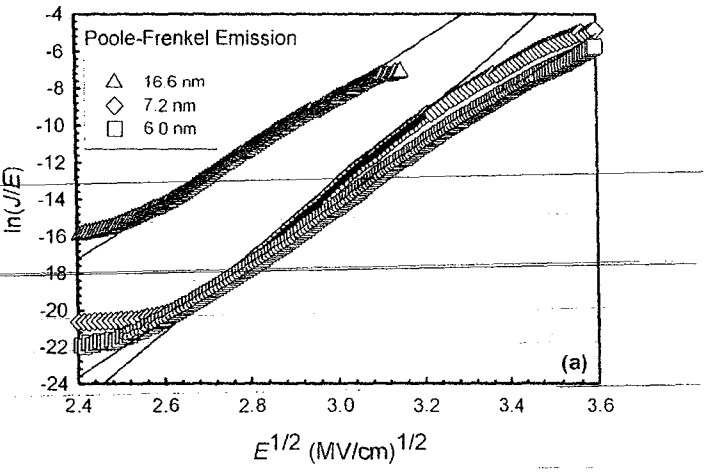


Fig. 2. Calculated charge mobility in bulk oxide as a function of oxide thickness.

Since only samples with $t_{ox} = 2.0, 5.0, 9.6$, and 16.6 nm have revealed the transition electric field from Ohm's law to TFL process (E_{on}), therefore, these are the only oxides with μ values that have been calculated (Fig. 2). The calculated μ value is similar to those obtained from Ohm's law. Even though all of the oxides were grown in same process and condition, the extracted μ and S values are much different in this process.

As the electric field is further increased, charge is conducted through the oxides ($t_{ox} = 6.0, 9.6$, and 16.6 nm) via Poole–Frenkel (PF) emission. This is a process of field-enhanced thermal excitation of trapped electron into conduction band (E_C) of oxide. It has been reported that the traps are in acceptor-like nature [18]. When an electron is emitted from a trap, the trap becomes neutral and the emitted electron is moved to the positively charged electrode and this produces a steady-state current. This current can be mathematically represented by $J_{PF} = (qN_c\mu)E\exp\{[-q(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0})]/[KT]\}$; where N_c, ϕ_t, ε_r, ε_0, and K are the density of states in E_C, trap energy level, dynamic dielectric constant, dielectric constant of vacuum, and Boltzmann's constant, respectively [19]. From the slope of $\ln(J/E) - E^{1/2}$ plot [Fig. 3(a)], ε_r has been extracted and shown in Fig. 3(b). The error bars presented in each data point refer to the ε_r value obtained from different temperatures. The self-consistent ε_r values at different temperatures and close to its theoretical value of 3.9 have ensured that PF emission is the dominate conduction mechanism in this investigated electric field. Besides PF emission, FN tunneling has been the major conduction route through the oxide under high electric field. Unlike PF emission, FN tunnelling is being revealed in $t_{ox} > 2.1$ nm. The detail analysis of this mechanism has been reported [9].

Fig. 4 summarized the potential charge-conduction mechanisms at room temperature of thermally grown nitrided SiO_2 on n-type 4H SiC as a function of t_{ox} and E. Included in the figure are oxide breakdown field (E_B), defined as any electric field that could cause leakage current density higher than 10^{-6} A/cm^2, and oxide hard-breakdown field (E_{HBD}), defined



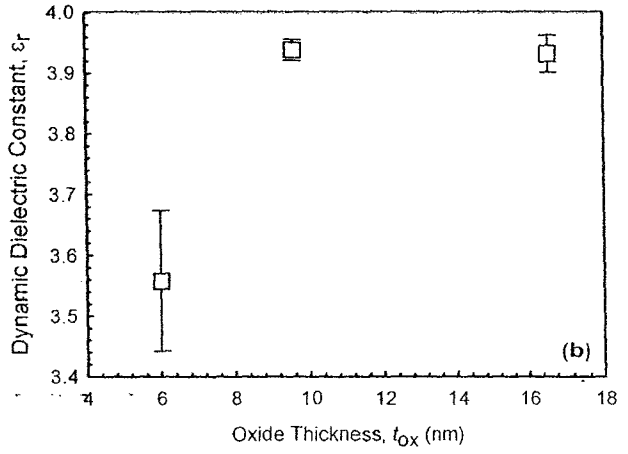


Fig. 3. (a) Poole–Frenkel (PF) [$\ln(J/E) - E^{1/2}$] plot of oxides with different oxide thicknesses. Solid symbols represent data points for PF emission linear fitting. (b) The extracted dynamic dielectric constant, ε_r, as a function of oxide thickness.

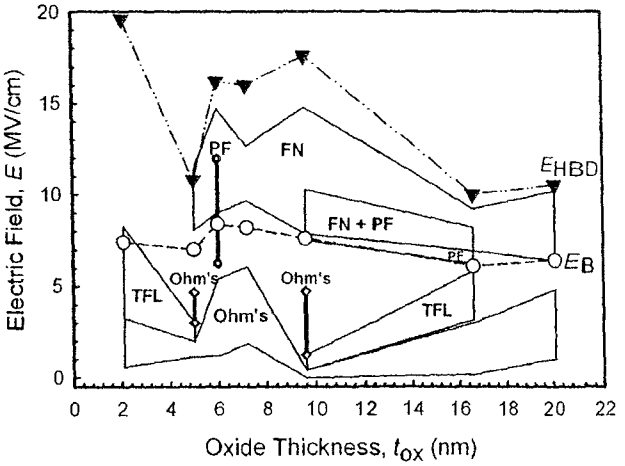


Fig. 4. A relationship plot among electric field, E, oxide thickness, t_{ox}, and potential charge conduction mechanisms for thermally grown nitrided on n-type 4H SiC. Breakdown field (E_B) and hard breakdown field (E_{HBD}) of oxide have been included in the plot.

as any electric field that induces an instantaneous increase of current density. From the figure, one could easily determine the conduction mechanism responsible to current leakages in different t_{ox}. It is also obvious that leakage current in MOS-based devices operate at or below 3 MV/cm is govern by Ohm's law or/and TFL process and not FN tunneling.

4. Conclusions

In this Letter, analysis of charge-conduction mechanism in thermally grown nitrided SiO_2 on n-type 4H SiC has been systematically performed and reported. Ohm's law, trap-filled-limited, Poole–Frenkel emission, and Fowler–Nordheim tunneling have been identified as the potential current leakage paths in the oxides with various thicknesses (2–20 nm). A relationship plot among oxide thickness, electric field, and type of conduction mechanism has been established.

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X-ray Reflectivity Analysis of Nitrided SiO_2 Grown in Different Percentage of N_2O Gas on 4H-SiC Substrate

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ABSTRACT

Thin film nitrided SiO_2 has been grown thermally on n-type 4H-SiC substrate in a diluted N_2O ambient at 1175°C for certain period. Three different percentages of N_2O gas (1%, 10%, and 50%) diluted in N_2 have been investigated. The films have been characterized using X-ray reflectivity to estimate their oxide thickness, film density, and SiC-SiO_2 interface roughness. The effects of percentage N_2O on these parameters have been reported.

Keywords: X-ray reflectivity, nitridation

INTRODUCTION

Thermal nitrided SiO_2 has been widely accepted as the best quality gate oxide used in silicon carbide (SiC) based MOS devices (Cheong, 2003). With this gate oxide, it enables SiC to be used as a substrate of MOS-based devices for high power and high temperature, applications. The oxide is commonly grown on SiC using N_2O gas at high temperature whereby dissociation of N_2O into NO and O_2 may promote oxidation and nitridation (Gupta, 1998). In order to grow a high quality and reliable nitrided oxide, the oxidation and nitridation rates must be in equilibrium or else accumulation of carbon cluster originated from SiC dissociation may deteriorate the performance of the oxide (Cheong, 2003). Therefore, by varying the N_2O percentage the purpose may be achieved. It has been reported that the best performance oxide is achieved by using 10% N_2O. However, the physical characteristics of the oxide (oxide density and roughness) are not well studied. In this paper, x-ray reflectivity (XRR) measurement is used to estimate the oxide density, roughness, and thickness. The effects of N_2O percentage on these parameters are reported.

EXPERIMENTAL METHODS

Thin nitrided SiO_2 was thermally grown on n-type 4H–SiC substrate. Three types of the oxides were grown using three different percentages of N_2O gas (1, 10, and 50% N_2O mixed with 99, 90, and 50% of high purity N_2 gas) at 1175°C. XRR was used to analyze oxide thickness, interface roughness, and electron density, which was related to oxide density. The XRR measurements were performed by a PANalytical X'Pert PRO MRD in a scattering angle range of $0 \leq 2\theta \leq 2°$ after the metal electrode gate has been etched. The X-ray source is a Cu Kα wavelength of $\lambda = 1.54$ Å using tube current of 40 mA and a voltage of 40 kV. The measurement was carried out using a set-up consisted of X-ray multilayer mirror at the incident beam and parallel plate collimator at the scatter beam. The measured results were analyzed using X'Pert Reflectivity version 1.1 software based on Paratt formulae. The fitting of the investigated nitrided SiO_2 film was performed using a three-slab model namely L1, L2 and L3 (Fig. 1), assuming that L1, L2, and L3 are the interfacial layer of SiC-SiO_2, bulk SiO_2, and unpassivated and exposed SiO_2 out most layer, respectively (inset of Fig. 2).

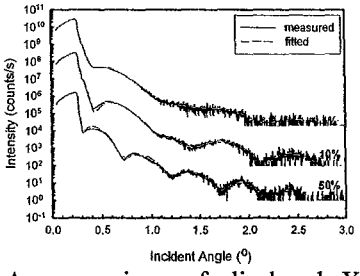

Figure 1: A comparison of displaced XRR profiles (measured and fitted) for the nitrided oxides.

The critical angle of the measurements were 0.221° (or 2θ = 0.442°) and the region less than this angle is suppose to be flatted if the sample size is big enough. The measured XRR data was well fitted with this model (Fig. 1). In additional, oxide total thickness (t_{ox}) was measured by Filmetric and Fourier methods.