FABRICATION OF SUBMICRON HEMT MUSHROOM GATE STRUCTURE USING ELECTRON BEAM LITHOGRAPHY AND ITS CHARACTERIZATION

by

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LIST OF ABBREVIATION

2DEG	Two-dimensional electron gas
AFM	Atomic force microscope
EBL	Electron beam lithography
ECR	Electron cyclotron resonance
FESEM	Field emission scanning electron microscope
FIB	Focus ion beam
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
ICP	Inductively coupled plasma
MBE	Molecular beam epitaxy
MESFET	Metal-semiconductor field effect transistor
MMA	Methyl methacrylate
MOCVD	Metal-organic chemical vapor deposition
MODFET	Modulation doped field effect transistor
NPGS	Nano patterning generator system
PMMA	Polymethyl methacrylate
RIE	Reactive ion etching
SEM	Scanning electron microscope

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LIST OF PUBLICATIONS

1. A. Yusof, A. Dolah, M. R. Yahya, A. F. Awang Mat, A. Abdul Aziz, K. Ibrahim (2005) "Dose Variation Study for 200 nm HEMT Mushroom gate Structure Using Electron Beam Lithography," in *Proc. 14th Scientific Conference for Electron Microscopy Society Malaysia (EMSM 2005)*, Penang.

2. A. Yusof, H. G. Lee, M. R. Yahya, A. F. Awang Mat, A. Abdul Aziz, K. Ibrahim (2005) "pHEMT Double Recess Gate Etch Using Electron Beam Lithography," *J. Solid State Science And Technology Letters, Vol. 12, No. 1 (Suppl.)*: 134.

3. A. Yusof, A. Dolah, M. R. Yahya, A. F. Awang Mat, A. Abdul Aziz, K. Ibrahim (2006) "FIB Analysis of HEMT Mushroom Gate Structure," in *Proc. 15th Scientific Conference for Electron Microscopy Society Malaysia (EMSM 2006)*, Terengganu.

4. A. Yusof, H. Soetedjo, M. N. Osman, A. Dolah, M. R. Yahya, A. F. Awang Mat, A. Abdul Aziz, K. Ibrahim (2007) "Ti/Pt Schottky Contact Measurements For HEMT Gate Metallization Using Current-Voltage Method," *J. Solid State Science And Technology, Vol. 15, No. 2 (2007.)*: 44-49.

FABRIKASI STRUKTUR GET CENDAWAN HEMT BERSAIZ SUBMIKRON MENGGUNAKAN LITOGRAFI ALUR ELEKTRON DAN PENCIRIANNYA

ABSTRAK

Dalam kajian ini, struktur get HEMT dengan *gatelength* bersaiz 200 nm dan berprofil cendawan telah direkabentuk, difabrikasi dan dicirikan. Ini membolehkan HEMT berfungsi pada frekuensi bersesuaian untuk applikasi telekomunikasi gelombang mikro dan millimeter. Corak get yang digunakan adalah rekabentuk yang mempunyai susunatur 10 x 10 set get, yang setiap satunya terdiri daripada 10 corak individu struktur get. Teknik semikonduktor piawai seperti litografi alur elektron, punaran basah, pemendapan logam dan *lift-off* telah digunakan disepanjang proses fabrikasi. Kaedah pengoptimuman dos alur elektron telah digunakan dimana nilai dos pembolehubah dikenakan ke atas sistem tiga lapisan perintang PMMA, berdasarkan corak get. Seterusnya, pencirian menggunakan SEM, AFM dan FIB dilakukan keatas struktur get HEMT. Didapati bahawa pada dos alur tengah bersamaan 192 $\mu C/cm^2$, *gatelength* bersaiz 200 nm telah dicapai. Kesan cendawan juga telah berjaya diperolehi berdasarkan analisa keratan rentas. Selain itu, sentuhan Schottky antara logam get dan lapisan epi HEMT telah diperolehi. Lapisan Cap n+ GaAs HEMT telah dipunar sehingga 40 nm manakala lapisan logam get Ti/Pt/Au telah dimendapkan untuk melengkapkan sentuhan Schottky berkenaan. Jurang ketinggian sentuhan Schottky, ϕ_b, diantara logam get dan lapisan Supply AlGaAs yang didapati melalui pengiraan adalah 0.65 eV.

FABRICATION OF SUBMICRON HEMT MUSHROOM GATE STRUCTURE USING ELECTRON BEAM LITHOGRAPHY AND ITS CHARACTERIZATION

ABSTRACT

In this research study, 200 nm gatelength HEMT gate structures with mushroom-shaped profile have been designed, fabricated and characterized. This allows HEMT to operate in frequencies suitable for microwave and millimeter-wave telecom applications. Gate design consisting of a 10 x 10 array of 10 individual gate strips was used as basis for patterning. Throughout the fabrication step, standard semiconductor processes such as electron beam lithography, wet etching, metal deposition and lift-off process were used. Electron beam dose optimization method was employed, in which variable dose values were exposed on PMMA tri-layer resist system based on the gate design. Subsequently, the HEMT gate structures were characterized using SEM, AFM and FIB. It was found that at central beam dose of 192 $\mu C/cm^2$, gate lengths of 200 nm have been achieved. The mushroom effect has been successfully constructed based on the cross-sectional analysis. Additionally, Schottky contact between gate metal and HEMT epi-layers has been obtained. The HEMT n+ GaAs Cap layer was recessed for 40 nm and Ti/Pt/Au gate metal stack was deposited to create the Schottky contact. The calculated Schottky contact barrier height, ϕ_b, between the gate metal stack and AlGaAs Supply layer, was found to be 0.65 eV.

CHAPTER 1

INTRODUCTION

Since first invented by Dr. Takashi Mimura, High Electron Mobility Transistor (HEMT) has over the years developed as the device of choice for high frequency analog applications especially in communication sectors. Indeed, GaAs-based HEMTs are the building block of many analog circuits which includes power amplifiers found in most cellphones and cellular base stations. A market research report by The Information Network as shown in Table 1.1 indicates that the total GaAs IC market which includes HEMT integrated circuits (IC) has increased to USD 3.13 billion in 2005 and is forecasted to reach USD 4.622 billion in 2009 [1]. Strong demands in communications market have increased its usage and growth, backed by the advancement in the semiconductor equipment and fabrication process techniques for higher frequency HEMTs.

Table 1.1: Worldwide GaAs Market Forecast By Application (USD mill.) [1]

	2003	2004	2005	2006	2007	2008	2009
Wireless Telecom	2,085	2,334	2,316	2,672	3,019	3,374	3,656
Fiber Telecom	372	446	438	500	561	625	684
Consumer	192	186	157	106	74	52	37
Aerospace / Defense	111	80	78	81	90	95	97
Other	148	160	141	162	176	164	148
Total	2,908	3,206	3,130	3,521	3,920	4,309	4,622

Over the years, the development of HEMT has evolved into methods to alter conventional square-shaped cross-sectional gate structures into that of T-shaped or mushroom-shaped cross-sectional gate structures with ultra-short gatelength. This allows HEMT to operate at higher frequencies needed especially in today's high speed telecommunication network for microwave and millimeter-wave applications. The values of gatelengths as reported in various literatures currently ranges from 150 nm down to 50 nm [2-4]. This ultra-short gatelength requirement is also part of Telekom Research & Development (TMR&D) research project specifications for the development of high frequency HEMT devices. From simulation, it is shown that with 200 nm HEMT mushroom gate it is enough to obtain HEMT operating frequency up to 60 GHz which suits telecommunication applications [5].

It is therefore the aim of this work to design, construct and characterize this type of HEMT gate structures. The main goal of this research work is three-fold:

i. to design and construct 200 nm gatelength of the HEMT gate structures with mushroom-shaped profile
ii. to perform beam dose exposure optimization during electron beam lithography process
iii. to characterize the HEMT gate structures through physical inspection and electrical measurements

To achieve these objectives, this research study is largely divided into two parts. The first part is to fabricate the gate structure which includes device fabrication steps such as electron beam lithography, etching, metal deposition and lift-off

process. The second part is to characterize the HEMT gate which includes physical characterization using SEM, AFM and FIB analysis as well as electrical characterization with Schottky contact measurements of the gate.

This thesis begins with an introduction in Chapter 1. Chapter 2 discusses the basic theory of HEMT, metal-semiconductor physics, standard fabrication steps of gate fabrication and electron beam lithography involving multilayer resist development. It also discusses the review of related current results reported by other researchers in the literatures. Chapter 3 presents the methods and materials used for gate fabrication as well as the characterization techniques employed. Chapter 4 reports all the results obtained from the experiments including electron beam dose optimization, physical gate feature investigations and Schottky contact characteristics. Finally, chapter 5 provides the conclusion of the work.

CHAPTER 2

THEORY & REVIEW

2.1 HEMT Device Technology

2.1.1 Introduction

GaAs–based HEMTs have appeared as the primary devices for the implementation of millimeter-wave analog circuits and ultra-high speed digital circuits. The first concept of modulation doping was first introduced by Dingle et. all in 1978 [6]. In this technique, electrons from remote donors in a higher bandgap material transfer to an adjacent lower gap material. The electrostatics of the heterojunction results in the formation of a triangular well at the interface, which confines the electrons in a two-dimensional (2D) electron gas (2DEG). The separation of the 2DEG from the ionized donors significantly reduces ionized impurity scattering resulting in high electron mobility and saturation velocity.

Modulation-doped field effect transistors (MODFETs), or HEMTs, which use the 2DEG as the current conducting channel have proved to be excellent candidates for microwave and millimeter-wave analog applications and high-speed digital applications. This progress has been enabled by advances in crystal growth techniques such as MBE and MOCVD as well as advances in device processing techniques, most notably electron beam lithography, which enabled the fabrication of HEMTs with gate lengths in the region of 500 nm and below. Today, the fabrication and device performance of microwave and millimetre-wave HEMTs having mushroom-shaped or T-shaped gate structure with gatelengths down to 150 nm and even 50 nm have been reported elsewhere [2-4].

2.1.2 Structure & Behavior

2.1.2.1 Metal-Semiconductor Junction

Metal-semiconductor junction is created when metal is deposited onto an n-GaAs region [7]. By varying the type of metal or the type of semiconductor doping level, the junction can be made into a rectifying or a non-rectifying junction. Rectifying junctions favorably permit current to flow in one direction versus the other. For instance, electrons may flow easier from the metal into the semiconductor than the opposite. Therefore, a rectifying junction functions as a gate keeper to stop current from flowing in the reverse direction. The rectifying junction is commonly called a Schottky contact or a Schottky barrier junction. On contrary, the non-rectifying junction or ohmic contact permits current to flow across the junction in both directions with very low resistance.

Figure 2.1 shows a representation of the junction in the form of schematic and cross section with an external bias connected to the metal. The energy band diagram of this junction is shown in Figure 2.2 in a case at which the metal and semiconductor is totally separated from each other, and in the case where the two are put in intimate contact. Figure 2.2 (a), shows a finite number of electron exist in the conduction band of the semiconductor, and the number of these free electrons is dependant on the temperature and doping concentration or purity of the material. Likewise, there are a number of free electrons in the metal, and the number of free electrons is dependent on the metal and temperature. The only new parameter introduced in figure 2.2 (a) is the metal work function, Φ_m, which is the energy required to remove an electron from the Fermi level of the metal to a vacuum potential. Most of metals commonly used in GaAs circuits and devices have work functions between 4 and 5.5 eV.

If the semiconductor Fermi level is greater than the metal Fermi level, $\chi + V_{CF} < \Phi_m$, as is shown in Figure 2.3(a), then when the metal and semiconductor are put in intimate contact, electron will diffuse from the semiconductor to the metal. As electrons are depleted from the semiconductor, a net positive charge is created in the semiconductor at the junction. This positive charge will exert a force on the electrons that opposes the diffusion current. Equilibrium is established when these two forces are equal, as shown in Figure 2.3(b). It is within this region, called the deletion region, that all of the junction's electrical properties are established. The amount of band bending is called the built-in potential, V_{bi}. For an electron to cross from the semiconductor to the metal, it must overcome V_{bi}, whereas an electron moving from the metal to the semiconductor must overcome the barrier potential, Φ_b. To a first approximation, the barrier height is independent of the semiconductor properties, whereas V_{bi} is dependent on the doping level.

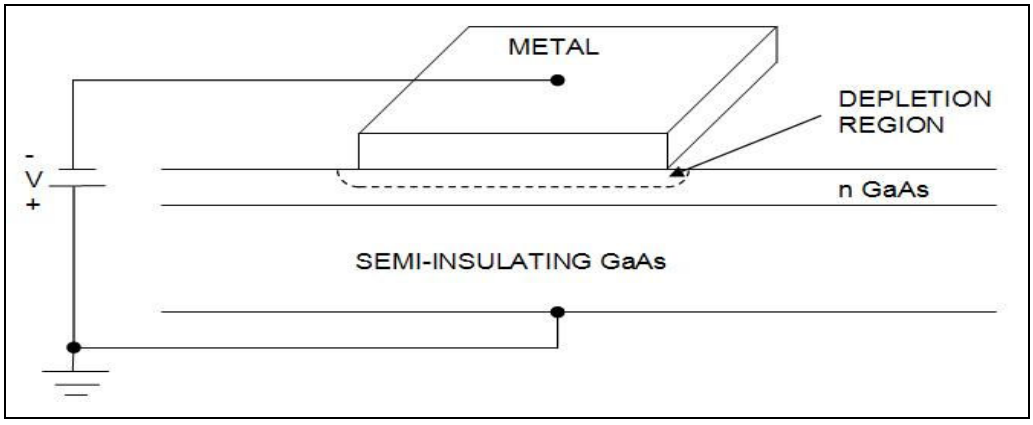
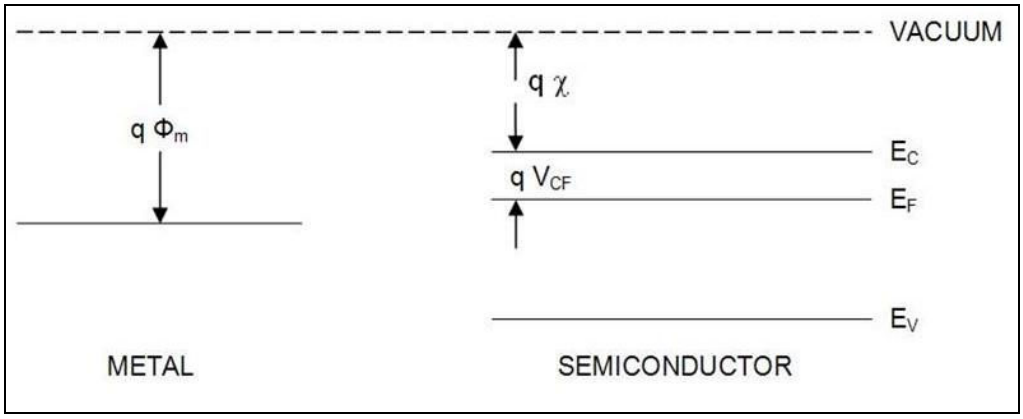
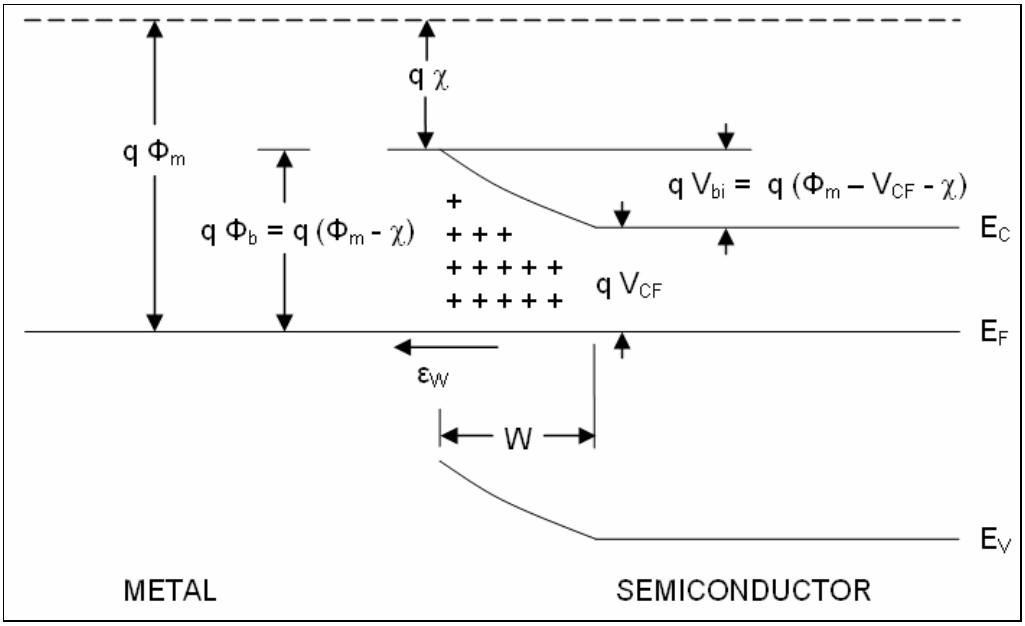


Figure 2.1: Schematic and cross section of metal-GaAs junction

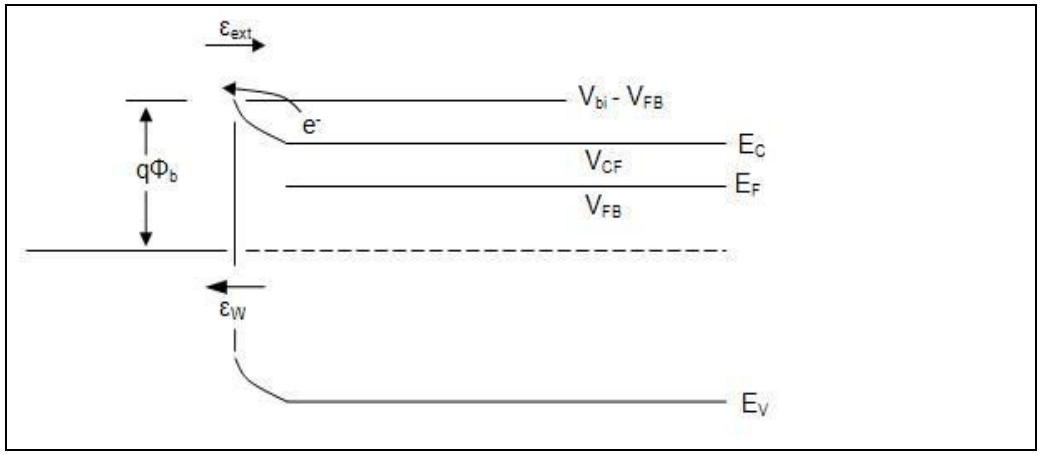


(a)

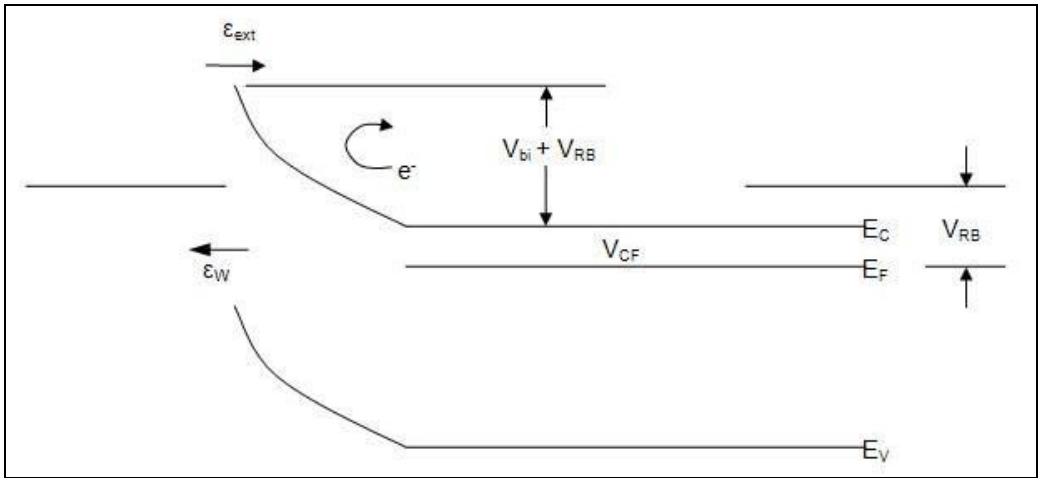


(b)

Figure 2.2: Energy band diagram of metal and semiconductor
(a) separated from each other and (b) in intimate contact



(a)



(b)

Figure 2.3: Energy band diagram of metal-semiconductor junction under (a) forward bias and (b) reverse bias

If an external potential is applied across the junction, the added electric field will disturb the equilibrium conditions. A positive external potential (Figure 2.1) will create an electric field across the junction that is opposite to the electric field caused by the depleted GaAs atoms. The result is that the diffusion current will not be sufficiently opposed, and the current will flow across the junction. This is shown schematically in Figure 2.3 (a). Note that the reduction in the barrier for electrons flowing from the semiconductor to the metal, but not the electrons flowing from the metal to the semiconductor. If a negative voltage is applied to the metal, the external

field will reinforce the electric field caused by the depleted carriers, increase the band bending at the junction, and prevent the diffusion current from flowing (Figure 2.3 b)

In the case of HEMT, the deposition of gate metal onto the n AlGaAs supply layer creates a Schottky contact [8]. The transport of electrons over the potential barrier of this Schottky diode, usually called thermionic emission, is represented in terms of current density, J:

$$J = A^{**}T^2\left[\exp\left(-\frac{q\phi_b}{kT}\right)\right].\left[\exp\left(\frac{qV}{nkT}\right)\right] \qquad \text{(Eq. 2.1)}$$

$$= J_S.\left[\exp\left(\frac{qV}{nkT}\right)\right] \qquad \text{(Eq. 2.2)}$$

where;

$$J_S = A^{**}T^2\left[\exp\left(-\frac{q\phi_b}{kT}\right)\right] \qquad \text{(Eq. 2.3)}$$

In Eq. 2.3, A^{**} is the Richardson constant, T is temperature (in K), n is the ideality factor (=1 for an ideal Schottky barrier diode), q is electric charge, k is Boltzman constant and ϕ_b is Schottky barrier height (eV).

From Eq. 2.3, it is obvious that J is exponentially dependent on the barrier potential, temperature, and the applied voltage. It is this strong dependence on the applied voltage that makes the junction a good rectifier. Furthermore, an ideal diode would have n = 1, but for actual diodes, n > 1. A change in the ideality factor over the life of the diode is an indication that the metal-semiconductor interface is

changing. Table 2.1 shows the typical Schottky barrier heights obtained for a number of different metals on the surface of GaAs [9]

Table 2.1 Selected Schottky barrier height for common metals on GaAs

Metal	Schottky barrier height (eV)
Al	0.76
Au	0.92
Cr	0.81
Ni	0.82
Pt	0.99
Ti	0.83
Pd	0.93
W	0.80

2.1.2.2 Device Physics

The epitaxial structure of a basic HEMT is illustrated in Figure 2.4. The HEMT structure is grown on semi-insulating GaAs substrate using MBE or MOCVD. Table 2.2 contains the common HMET epitaxial structures. The typical thickness values of each epitaxy layers can be found in Appendix A.

The buffer layer, also typically GaAs, is epitaxially grown on substrate in order to isolate defects from the substrate and to create a smooth surface upon which to grow the active layers of the transistor. Many HEMT structures contain a superlattice structure to further inhibit substrate conduction. A superlattice structure is a periodic arrangement of undoped epitaxial layers used to realize a ticker epitaxial layer of a given property.

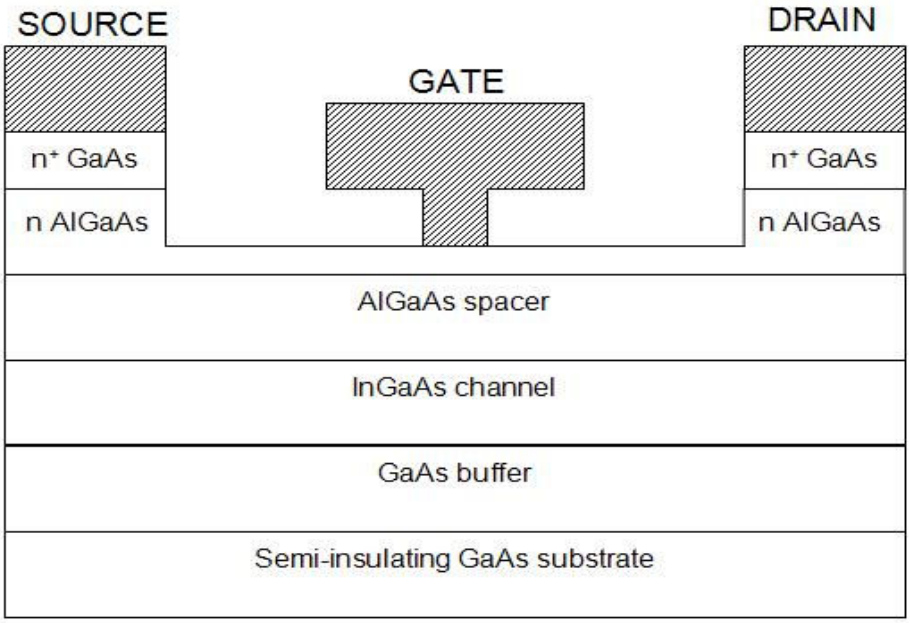


Figure 2.4: Epitaxial structure of a basic AlGaAs/GaAs HEMT

Table 2.2: Epitaxial layer compositions for basic GaAs-based HEMT

Device Layer	HEMT
Ohmic contact	n^+ GaAs
Schottky contact	n AlGaAs
Spacer	Undoped AlGaAs
Channel	Undoped InGaAs
Buffer	GaAs

In conventional HEMT, the channel is where all the electron conduction will take place. The most important point about the channel layer in HEMT devices is the two-dimensional electron gas (2DEG) that results from the band-gap difference between $Al_xGa_{1-x}As$ and GaAs. Illustrated in Figure 2.5 is the band diagram of a

generic HEMT showing the 2DEG formed by the different band gaps. The 2DEG is formed since the higher bandgap of $Al_xGa_{1-x}As$ allows free electrons to diffuse from the $Al_xGa_{1-x}As$ to the lower bandgap GaAs near the interface. A potential barrier then confines the electrons to a thin sheet of charge known as the 2DEG. In HEMT, the 2DEG has significantly less Coulomb scattering, resulting in a very high mobility device structure.

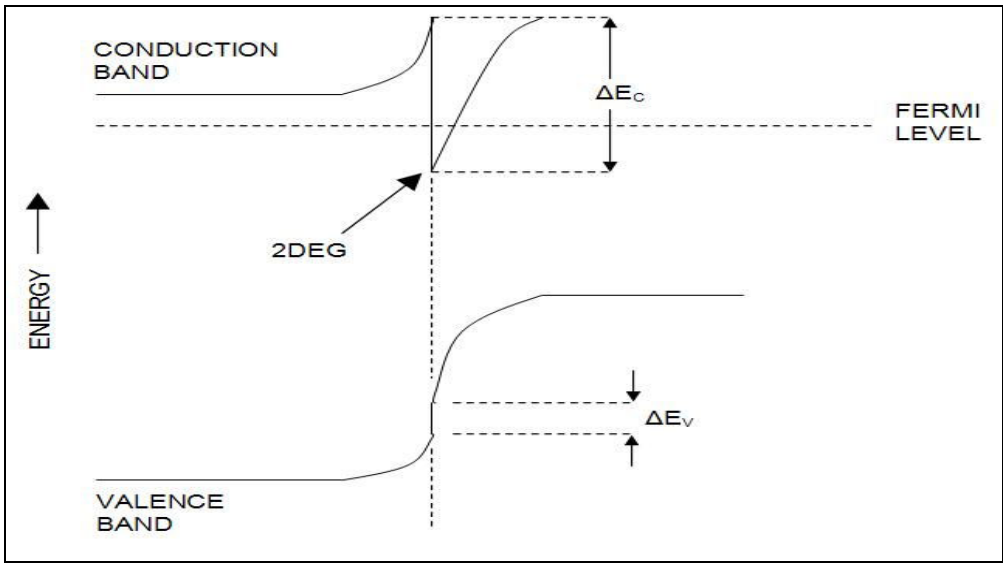


Figure 2.5: Energy band diagram of a generic AlGaAs-GaAs HEMT showing the 2DEG quantum well channel

The remainder of the HEMT structure contains an $Al_xGa_{1-x}As$ spacer layer, a donor layer n+ $Al_xGa_{1-x}As$, an n $Al_xGa_{1-x}As$ Schottky contact layer, and a highly doped n+ GaAs layer. The spacer layer serves to separate the 2DEG from any ionized donors generated by the pulse doping or n+ active layer. The drawback of the spacer layer, however, is that the sheet carrier concentration (total amount of charge) in the channel is reduced as the spacer layer thickness is increased. The donor layer or Schottky layer is an n+ $Al_xGa_{1-x}As$ layer and serves as the source of the electrons. To avoid the possibility of electron conduction in the $Al_xGa_{1-x}As$ (which has low

electron mobility), the thickness of the Schottky must be chosen so that the depletion region of the gate overlaps the depletion at the $Al_xGa_{1-x}As$/2DEG interface for depletion mode devices. The n+ GaAs is present to realize low-resistance ohmic contacts.

The structure described above is a basic HEMT structure. Most of the structures used today are variants of this, having been optimized for performance and applications. For instance, many pHEMTs used for power applications will incorporate two silicon pulses, the second one below the channel, to increase the total charge available.

The fabrication and basic operation of HEMT devices differs from other type of devices (such as MESFET) in terms of the presence of $Al_xGa_{1-x}As$ in the epitaxial structure. As mentioned previously, $Al_xGa_{1-x}As$ has larger bandgap energy than GaAs and the band gap increases with the AlAs mole fraction. HEMTs require ohmic contacts directly to the 2DEG, which is made more difficult with increased AlAs mole fraction. An advantage of the AlGaAs is the higher Schottky barrier height resulting from the deposition of gate metal on the AlGaAs. Unfortunately, the high doping in the donor layer decreases the breakdown voltage. However, power HEMT and p-HEMT structures with higher breakdown voltages (> 10V) have been engineered using either double recess technology or by reducing the doping in the Schottky layer.

When a negative gate bias is applied to the HEMT device, the Schottky layer becomes depleted. As the gate is biased further, the 2DEG becomes depleted. This results in the modulation of the channel (2DEG) by a negatively applied gate bias where gain and amplification occur until the channel is pinched off (i.e. fully depleted). The transconductance is given by

$$g_m = (\varepsilon v_{sat} W_g)/d \qquad \text{(Eq. 2.4)}$$

Where ε is the permittivity of $In_xGa_{1-x}As$, V_{sat} equals saturated velocity of carriers in $In_xGa_{1-x}As$, W_g is the unit gate width of the device, and d equals the distance from the gate to the 2DEG. Since the conduction of electrons from the source to the drain takes place in a channel that is well-confined, g_m will remain very high at low drain currents. At low drain current, the distance d will increase because of the edge of the depletion region enters the tail of the doping profile. This results in a compression of the g_m. The higher mobility of the HEMT results in lower parasitic drain and source resistances. As a result, the current gain cutoff frequency $f_T = g_m/(2\pi C_{gs})$ and the power gain cutoff frequency f_{max} are increased for a given gate length leading to a lower noise figure and higher gain.

2.1.3 Impact of Gate Geometry and Process

2.1.3.1 High Frequency Performance

The HEMT small signal equivalent circuit model is shown in Figure 2.6 [10]. This model can provide insights into the role of various parameters in the high-frequency performance of the device. The two measures of the high performance of a HEMT can be defined in terms of the small signal model of the device. The current gain cutoff frequency f_T can be defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{\upsilon_{sat}}{2\pi L_G}\eta \qquad \text{(Eq. 2.5)}$$

From this equation, f_T can be increased by increasing electron velocity in the channel, v_{sat}, and reducing gate length, L_G. The current gain cutoff frequency is mainly a physical measure of device performance. A more practical measure of high frequency device performance is f_{max}, the power gain cutoff frequency. This is the frequency at which the power gain of the HEMT is unity. It is defined as follows [11]:

$$f_{\max} = \frac{f_T}{\sqrt{4g_{ds}(R_{in} + \frac{R_S + R_g}{1 + g_m R_S}) + \frac{4C_{gd}}{5C_{gs}}(1 + \frac{2.5C_{gd}}{C_{gs}})(1 + g_m R_S)^2}} \qquad \text{(Eq. 2.6)}$$

A simpler form of Eq. 2.6 is:

$$f_{\max} = f_T \sqrt{\frac{R_{ds}}{4P_{in}}} = \frac{f_T}{\sqrt{4g_{ds}R_{in}}} \qquad \text{(Eq. 2.7)}$$

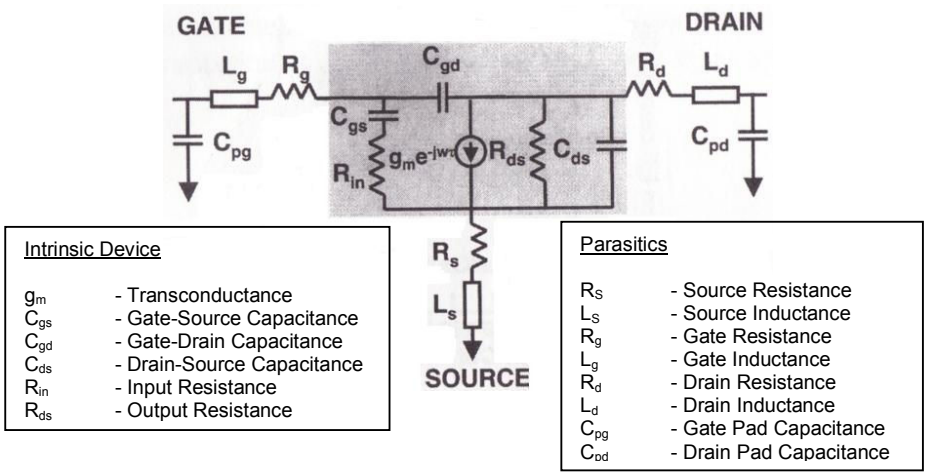


Figure 2.6: Small signal equivalent circuit model

To improve the f_{max} of the device it is necessary to minimize the quantities in the denominator of Eq. 2.6. The crucial parameters here are the output conductance of the device g_{ds}, and the source and gate parasitic resistances R_S and R_g and the gate-

drain feedback capacitance C_{gd} which need to be minimized. In terms of fabrication process technology, f_T and f_{max} can be significantly improved with a T-shaped or mushroom-shaped gate structure. This is possible by constructing shorter gate length, L_G, while maximizing the cross-sectional area of the gate. The typical values of f_t and f_{max} can be found in Appendix A.

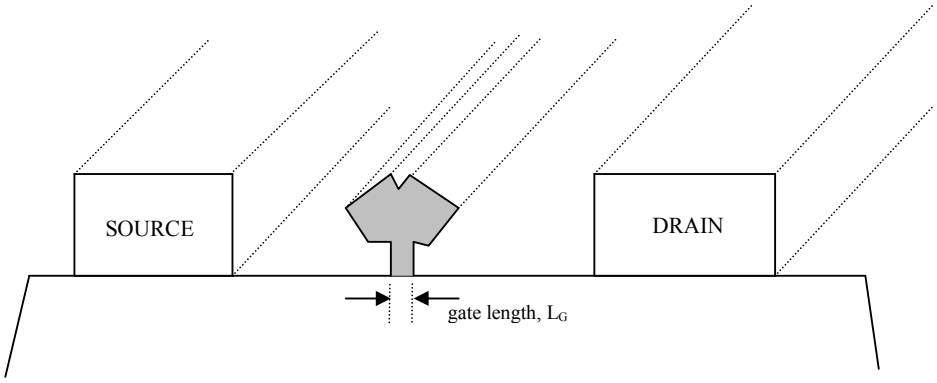


Figure 2.7: The gate length, L_G, of HEMT

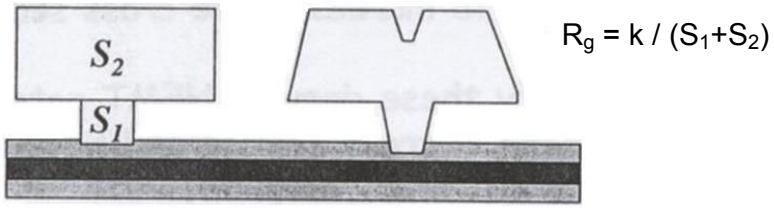


Figure 2.8: Cross-sectional area ($S_1 + S_2$) of HEMT

Equations 2.5 and 2.6, as well as figures 2.7 and 2.8, show that in order to achieve higher frequency, the HEMT gate has to be mushroom-shaped in cross section, and have the smallest possible width of footprint. As the intended feature resolution of the gate is in the nano-meter range, electron beam lithography technique is used instead of optical lithography.

2.1.3.2 Gate Recess Process

Of the etching processes available, most fall into two separate and in many ways complementary categories; wet etching in aqueous chemical solutions and dry etching in plasmas [12].

In wet etching the basic operation of the etchants involves two chemical components, with one component serving as an oxidizer and the other as a reducing or complexing agent for removal of the oxide species. Many chemical systems have been investigated, with the majority of the systems employ hydrogen peroxide as the oxidizing agent and acid serving as the reducing and complexing agent for the surface atom desorption. Table 2.3 lists common wet chemical etchants used for gate recess:

Table 2.3: Wet chemical etchants for gate recess on GaAs [12]

Material	Etchant	Etch rate
GaAs	H_2SO_4:H_2O_2:H2O 1:10:250	30 nm / min @ 23 °C
GaAs	NH_4OH:H_2O_2:H2O 3:1:150	80 nm / min @ 20 °C
GaAs/AlxGa1-xAs	CA:H_2O_2 4:1 CA – 100g solid citric acid in 100ml of DI water	360 nm / min @ 20 °C

In addition to wet etching, a variety of dry-etching techniques exist such as plasma etching, conventional reactive ion etching (RIE), electron cyclotron resonance (ECR) RIE, and inductively coupled plasma (ICP) RIE. Typical etch rate for GaAs using conventional RIE is listed in Table 2.4:

Table 2.4: Typical etch rate for GaAs using RIE

Chemistry	Bias Voltage	Etch rate (nm/min)
Cl_2	300 V	250
Cl_2/Ar	100 V	2000
$SiCl_4$/Ar	100 V	500
CH_4/H_2	600 V	40

An important issue with any dry etching technique is that of damage to the semiconductor material. Due to the ion bombardment that occurs in all varieties of RIE and other ion-assisted etching methods, the semiconductor is damaged by collisions with energetic ions [13]. The damage can be manifested in the form of non-stoichiometric regions, defect aggregates and point defects. For this reasons, most gate recess etching processes are done using wet etching.

2.1.3.3 Choice of Gate Metal [8]

Several requirements of Schottky contact include having high electrical conductivity, good adhesion and effectiveness as diffusion barrier. However, it is not possible to achieve all requirements with a single metal. Gold for instance is a good electrical conductor, but shows poor adhesion to GaAs. Such multiple, conflicting requirements in GaAs processing often lead to multi-level metallization consists of two or more layers of different metals.

In principle, high electrical conductivity can be met by four metals: gold, aluminium, silver and copper. Copper however, is a rapid diffuser and exhibits high chemical reactivity so therefore copper or copper alloys are almost never used on GaAs HEMTs. Similarly, silver is being rarely used due to being highly reactive. Aluminium can be used entirely as gate metal as it has good electrical conductivity and good adhesion to GaAs. However, gold is often chosen over aluminium due to

higher electrical conductivity and chemical inertness. Despite this, gold has poor adhesion to GaAs and is highly susceptible to diffusion. Hence, metals with good adhesion to GaAs such as chromium or titanium are deposited first before gold. However, gold can diffuse through metals such as titanium and chromium and initiate diffusion problems at the metal-GaAs interface. In these case, barrier metal which prevent diffusion are used between the Schottky metal (Ti/Cr) and gold. This barrier metal is usually platinum, but molybdenum and palladium have also been used. It can be concluded that most HEMT gates are either aluminium entirely or composition of metal stacks (the first metal listed is nearest to substrate) such as Ti/Pt/Au, Ti/Mo/Au, Cr/Pd/Au and Mo/Al. For this study, Ti/Pt/Au composition is used exclusively.

2.2 Electron Beam Lithography (EBL)

2.2.1 EBL System

In HEMT process development, EBL is used primarily for the gate structure formation which requires finer resolution unattainable by optical lithography. Unlike optical lithography, EBL is done by using a direct-write method in which electron beam is used to generate patterns directly. IC designs are downloaded direct from a computer and transferred onto wafers using an e-beam exposure mechanism, enabling features in the sub-1μm region. Figure 2.9 shows a typical EBL exposure system.

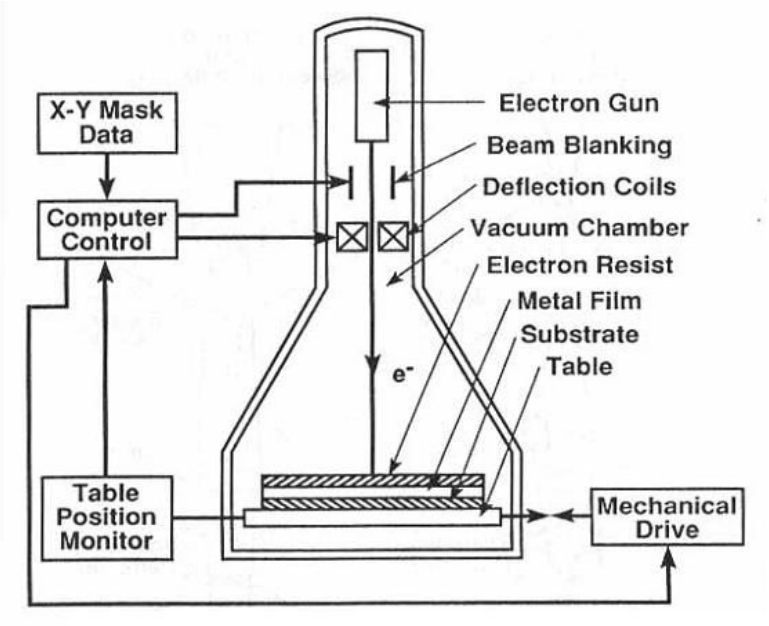


Figure 2.9: A typical EBL exposure system

Direct-write EBL has a big advantage over optical lithography for its superior resolution. With optimized exposure methods and use of high resolution resists such as polymethyl methacrylate (PMMA), resolution of less than 100 nm is not uncommon. This dramatic improvement in resolution compared to optical lithography is a direct consequence of the fundamental difference in operational principles of EBL and optical lithography; rather than exposing the resist with light of a particular wavelength, the sample is exposed to electrons in a desired pattern. Because the de Broglie wavelength of electrons in the energy range generally used for lithography is orders of magnitude smaller than typical optical wavelengths, diffraction effects are negligible and excellent resolution can be achieved.

The first demonstration of using a scanned electron beam for lithography purposes occurred in 1960 when Mullenstadt and Speidel patterned 20 nm features on a thin substrate [14]. Most of the high resolution lithography work has utilized PMMA. In 1978 Broers et. all demonstrated 25 nm linewidths at a period of 50 nm

on a thin Si_3N_4 film using 110 nm of PMMA and a lift-off of 20 nm of AuPd [15]. The thin film substrate was used to minimize the back-scattered electron effects. Features slightly smaller than 10 nm have also been achieved on PMMA resists using electron beam at much higher accelerated voltage up to 100 kV. Patterns with 8 nm wide lines in PMMA on a bulk Si substrate using 80 keV beam[16] and 5-7 nm wide lines on PMMA using a 100 keV beam [17] has been reported.

2.2.2 E-beam Properties

2.2.2.1 Energy Profile

Although EBL tools are capable of forming extremely fine probes, things become more complex when the electrons hit the work-piece. As the electrons penetrate the resist, they experience many small angle scattering events (forward-scattering), which tend to broaden the initial beam diameter. As the electrons penetrate through the resist into the substrate, they occasionally undergo large angle scattering events (back-scattering). The back-scattered electrons cause the proximity effect, where the dose that a pattern feature receives is affected by the electrons scattering from other features nearby. During this process the electrons are continuously slowing down, producing a cascade of low voltage electrons called secondary electrons.

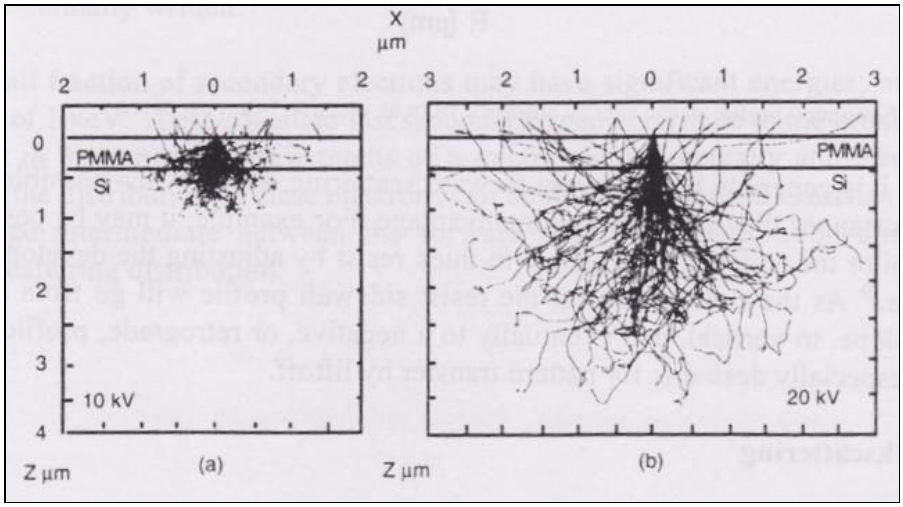


Figure 2.10: Monte Carlo simulation of electron scattering in resist on a silicon substrate at (a) 10 kV and (b) 20 kV [18]

Figure 2.10 shows some computer simulations of electron scattering in typical samples. Such scattered electrons resulted exposure from an incident electron beam which is not spatially limited to the initial beam distribution. The effect of electron beam scattering can be characterized by the double-Gaussian model [19]:

$$\exp osure(r) = \frac{1}{\pi(1+\eta)}\left[\frac{1}{\beta_f^2}\exp\left(\frac{-r^2}{\beta_f^2}\right)+\frac{\eta}{\beta_b^2}\exp\left(\frac{-r^2}{\beta_b^2}\right)\right] \qquad \text{(Eq. 2.8)}$$

where r is the radial distance from the beam position, β_f is the forward-scattered electron range (finite incident beam diameters are also modeled in β_f), η is the ratio of integrated exposure from back-scattered electrons relative to forward-scattered electrons, and β_b is the back-scattered electron range. Parameters for this model depend on the incident beam energy, spot size, and the resist and substrate materials.

2.2.2.2 Electron Scattering [18]

Some fraction of electrons penetrating the resist will undergo small angle scattering events, which can result in a significantly broader beam profile at the bottom of the resist than at the top. Forward-scattering is minimized by using the thinnest possible resist and the highest available accelerating voltage. Although it is generally best to avoid forward-scattering effects when possible, in some instances they may be used to advantage. For example, it may be possible to tailor the resist sidewall angle in thick resist by adjusting the development time. As the time increases, the resist sidewall profile will go from a positive slope, to vertical, and eventually to a negative or retrograde profile, which is especially desirable for pattern transfer by lift-off.

As the electrons continue to penetrate though the resist into the substrate, many of them will experience large angle scattering events. These electrons may return through the resist at a significant distance from the incident beam, causing additional resist exposure. This is called the electron beam proximity effect. The range of electrons (defined here as the distance a typical electron travels in the bulk material before losing all its energy) depends on both the energy of the primary electrons and the types of substrate. The fraction of electrons that are back-scattered, η, is roughly independent of beam energy, although it does depend on the substrate material, with low atomic number materials giving less back-scattering. Typical values of η range from 0.17 for Silicon to 0.50 for tungsten and gold.

Apart form that, as the primary electrons slow down, much of their energy is dissipated in the form of secondary electrons with energies from 2 to 50 eV. They are responsible for the bulk of the actual resist exposure process. Since their range in resist is only a few nanometers, they contribute little to the proximity effect. Instead,

the net result can be considered to be an effective widening of the beam diameter by roughly 10 nm. This largely accounts for the minimum practical resolution of 20 nm observed in the highest resolution electron beam systems and contributes (along with forward-scattering) to the bias that is seen in the positive resist systems, where the exposed features develop larger than the size they were nominally written. A small fraction of secondary electrons may have significant energies, on the order of 1 keV. These so called fast secondaries can contribute to the proximity effect in the range of a few tenths of a micron. Experimentally and theoretically, the distribution of these electrons can be fit well by third Gaussian with a range intermediate between the forward-scattering distribution and the back-scattering distribution.

2.2.2.3 Proximity Effect Avoidance & Corrections

The net result of the electron scattering discussed in previous sections is that the dose delivered from the electron beam tool is not confined to the shapes that the tool writes, resulting in pattern specific linewidth variations known as the proximity effect. If a pattern has fairly uniform density and linewidth, all that may be required is to adjust the overall dose until the patterns come out the proper size. This method typically works well for isolated transistor gate structures. Using higher contrast resists can help minimize the linewidth variations.

Many schemes have been devised to minimize the proximity effect which includes dose modulation technique [20] and computer software manipulation [21]. The proximity effect can also be minimized by working on thin substrates to reduce back-scattered electron contributions and using thin resists to reduce forward-scattering, or by using sparsely spaced patterns which are smaller than the back-scattered electron range. Alternatively, proximity effects can be compensated for by