DEVELOPMENT OF INDUCTIVELY-DEGENERATED LNA FOR W-CDMA APPLICATION UTILIZING 0.18 μm RFCMOS TECHNOLOGY

by

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DECLARATION

I hereby declare that the work in this thesis is my own except for quotations and summaries which have been duly acknowledged.

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Ω	Ohm
γ	Noise parameter, γ = 2/3 for long-channel
δ	Coefficient of gate noise, $\delta = 2\gamma$ = 4/3 for long-channel
α	Noise parameter, $\alpha = g_m / g_{d0}$
Γ	Reflection coefficient
Γ_S	Reflection coefficient looking into the source
Γ_{in}	Reflection coefficient looking into the input
Γ_L	Reflection coefficient looking into the load
Γ_{out}	Reflection coefficient looking into the output
μ_n	Mobility of electron
μ_p	Mobility of hole
ξ	Noise parameter of the uncorrelated portion of the transistor's gate noise
ξ_1	V_{DS} to V_{OV} ratio
κ	Noise parameter of the correlated portion of the transistor's gate noise
χ	Noise parameter that includes both correlated and uncorrelated portions of the transistor's gate noise
ρ	$\rho = V_{OV} / LE_{sat}$
ε_0	Permittivity of free space, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
λ	Wavelength of the frequency of operation
A_d	Area drawn
A_v	Voltage gain
A_{vo}	Open-circuit voltage gain
B_c	Correlation susceptance
B_{opt}	Optimum susceptance
B_S	Source noise susceptance

B_{system}	System bandwidth
c	Correlation coefficient, c = j0.395 for long-channel devices
C_a	Areal capacitance
C_c	Coupling capacitor
C_{db}	Drain-Body capacitance
C_{ex}	Extra capacitor placed across G-S for a PCSNIM LNA
C_f	Feedback capacitor
C_{gd}	Gate-Drain capacitance
C_{gs}	Gate-Source capacitance
C_{gsn}	Gate-Source capacitance of NMOS
C_{gsp}	Gate-Source capacitance of PMOS
C_{gsT}	Total Gate-Source capacitance
c_{light}	Speed of light, $c_{light} = 3 \times 10^8$ m/s
C_{ox}	Oxide capacitance of NMOS
C_{oxn}	Oxide capacitance of PMOS
C_{oxp}	Oxide capacitance
C_p	Capacitance per unit periphery
C_t	Total capacitance
d	Largest dimension of the design
E_b	Average bit energy
$(E_b/N_t)_{eff}$	Average bit energy to noise and interference power spectral density minimum ratio
E_C	Average energy per PN chip
$\overline{e_n}$	External voltage noise generator
E_{sat}	Field strength at which the carrier velocity has dropped to one half the value extrapolated at low-field mobility
f	Frequency
F	Noise factor

f_{block}	Frequency of the block signal
fcw	Spurious response frequencies
f_{IF}	Frequency of the IF Signal
f_{LO}	Frequency of the LO Signal
F_{min}	Minimum noise factor
F_{min}^{o}	Minimum noise factor for the classical noise matching input stage of the LNA
F_{min,P_D}	Minimum noise factor for the PCNO LNA
f_{RF}	Frequency of the RF signal
f_T	Transition frequency
F_{UW}	Frequency of unwanted signal
F_{UW1} (CW)	Frequency of the first unwanted signal of the CW nature
F_{UW2} (Modulated)	Frequency of the second unwanted signal of the modulated nature
f_{wanted}	Frequency of the wanted signal
G_c	Correlation conductance
g_{d0}	Drain-Source conductance at 0 V_{DS}
G_f	Conductance of C_f
g_g	Real, noiseless conductance in the gate circuit
g_m	Transconductance of the transistor
G_m	Transconductance of the circuit
g_{mb}	Body-effect transconductance of the MOSFET
G_m-C	Transconductance-Capacitor
G_{m_eff}	Effective transconductance of the circuit
g_{mT}	Total transconductance
G_n	Conductance contributing to thermal noise due to $\overline{i_n^2}$
G_{opt}	Optimum conductance

G_S	Conductance contributing to thermal noise due to $\overline{i_S^2}$ or source conductance
$I_{blocking}$ (CW)	Blocking signal (CW) band power spectral density
I_c	Noise current correlated with e_n
I_D	DC drain current
$\overline{i_d^2}$	Channel thermal noise source
i_g^2	Shunt noise current to g_g
$\overline{i_{g,c}^2}$	Gate noise current source correlated with the drain noise
$\overline{i_{g,u}^2}$	Gate noise current source uncorrelated with the drain noise
$\overline{i_n}$	External current noise generator
I_{or}	The total transmit power spectral density of the forward link at the base station antenna connector.
$\hat{I}_{or}$	The received power spectral density of the forward link as measured at the UE antenna connector.
I_{ouw}	Unwanted signal specified by the W-CDMA standard for linearity tests
i_S	Noise source
i_u	Noise current uncorrelated with e_n
k	Boltzmann constant, $k = 1.38 \times 10^{-23}$ J/°K
K	Stability factor
K_{ox}	Relative permittivity of silicon dioxide
k Ω	kilo-ohm
L	MOSFET's channel length
L_d	Length drawn
L_g	Gate inductor
L_s	Source inductor
N_o	Noise spectral density
N_t	Noise and interference power spectral density

$P_{2ndorder(blocker}$	Power of the second-order products of the blocker signal
$P_{allowed}$	Noise power allowed
P_{AVN}	Power available from the network
P_{AVS}	Power available from the source
P_{BLeak}	Power of the blocker leakage
$P_{BLOCKER\ (in\text{-}band)}$	Power of the in-band blocker
$P_{CW(interferer)}$	Power of the CW interferer signal
P_D	Power dissipated by the LNA
P_d	Perimeter
$P_{DPCH(Rx)}$	Power of the dedicated physical channel at the receiver
P_I(acceptable)	Maximum allowable interference level
P_{INT}	Power of the interfering signal
$P_{intermodulation}$	Power of an intermodulation signal
$P_{modulated(interferer)}$	Power of the modulated interferer signal
P_N	Noise power
P_{N+I}	Power of noise + interference
$P_{N(actual)}$	Actual noise power
$P_{N(max)}$	Maximum allowable noise power
$P_{N(osc)}$	Noise power of the oscillator
P_o	A constant which is dependent on the process parameters v_{sat} and E_{sat}
P_{TxLeak}	Power of the Tx leakage signal
q	Electronic charge, q = 1.6×10^{-19} C
Q_{in}	Quality factor of the input stage
Q_{in,opt,P_D}	Optimum quality factor of the input stage
Q_{ind}	Quality factor of the inductor
Q_{opt}	Optimum quality factor
$Q_{parallel}$	Quality factor of the parallel output impedance

Q_S	Quality factor in the form of the actual source (input) conductance
Q_{series}	Quality factor of the series output impedance
$Q_{S,opt}$	Optimum Q_S
$R_{\square}$	Sheet resistance
RF_{in}	RF signal at the input
RF_{out}	RF signal at the output
R_g	Gate resistance
R_{Lg}	Series resistance of L_g
R_n	Resistance contributing to thermal noise due to $\overline{e_n^2}$
R_n^o	Noise resistance of the classical noise matching of the input stage of the LNA
r_o	Output resistance of the MOSFET
R_{opt}	Optimum resistance
$R_{parallel}$	Resistance of the parallel impedance
R_S	Source (Input) resistor
R_{series}	Resistance of the series impedance
S_{11}	Input reflection coefficient
S_{12}	Reverse transmission coefficient
S_{21}	Forward transmission coefficient
S_{22}	Output reflection coefficient
T	Temperature
T_e	Electron temperature
T_0	Standard noise temperature, T_0 =300°K
t_{ox}	Oxide-thickness
t_{oxn}	Oxide-thickness for the NMOS
t_{oxp}	Oxide-thickness for the PMOS
Tx	Transmitter

V_{DD}	Supply voltage
V_{DS}	Drain-Source voltage
V_{dsat}	Drain-Source voltage at saturation
v_{gs}	Gate-Source voltage
v_{in}	Input voltage
V_{OV}	Overdrive voltage
ν_{sat}	Carrier velocity at saturation
V_{th}	Threshold voltage
W	MOSFET's width
W_d	Width drawn
ω_{IF}	IF angular frequency
ω_{IM}	Image angular frequency
ω_{LO}	LO angular frequency
Rx	Receiver
ω_{IF}	IF angular frequency
ω_{IM}	Image angular frequency
ω_{LO}	LO angular frequency
ω_{O}	Operating angular frequency
ω_{RF}	RF angular frequency
ω_{T}	Transition angular frequency
$X_{parallel}$	Reactance of the parallel impedance
X_{series}	Reactance of the series impedance
Y	Admittance
Y_c	Correlation admittance constant
Y_{opt}^{o}	Optimum noise admittance for cascade
Y_S	Noise Admittance
Z	Impedance

Z_{in}	Input impedance
Z_L	Load impedance
Z_{opt}	Optimum noise impedance
Z_{out}	Output impedance

LIST OF ABBREVIATIONS

2G	Second-Generation
3G	Third-Generation
AC	Alternating-Current
ACS	Adjacent-Channel Selectivity
ADC	Analog-to-Digital Converter
ADE	Analog Design Environment
BER	Bit-Error-Rate
BPF	Band-Pass Filter
BS	Base Station
BW	Bandwidth
C+CC	Capacitors and coupling capacitors
CDMA	Code Division Multiple Access
CG	Common-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
CNM	Classical Noise Matching
CR	Current-Reuse
CS	Common-Source
CW	Continuous Wave
dB	Decibel
DC	Direct-Current
DCR	Direct-Conversion Receiver
DPCH	Dedicated Physical Channel
$DPCH\_E_C$	Desired Signal Power
$\frac{DPCH\_E_C}{I_{or}}$	The ratio of the received energy per PN chip of the DPCH to the total transmit power spectral density at the BS antenna connector.

DRC	Design Rule Check
D-S	Drain-Source
DS-CDMA	Direct Sequence-Code Division Multiple Access
DUT	Device Under Test
FC	Folded-Cascode
FDD	Frequency Division Duplexing
GHz	Gigahertz
G-S	Gate-Source
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HD	Harmonic Distortion
I	In-Phase
IC	Integrated Circuit
IDC	Inductively-degenerated cascode
IF	Intermediate-Frequency
IIP_2 (Tx)	Input-referred second-order intermodulation point for the Tx band
IIP_3	Input-Referred Third-Order Intermodulation Point
IM	Inter-Modulation
IP_{1dB}	Input 1-dB Compression Point
IP_2	Second-Order Intercept Point
IRR	Image Rejection Ratio
I-V	Current-voltage
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
LVS	Layout versus Schematic
Mbps	Megabit Per Second

MCMC	Malaysia Communications and Multimedia Commission
Mcps	Megachip Per Second
MHz	Megahertz
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NF	Noise Figure
NF_{max}	Maximum Noise Figure
NMOS	N-Metal Oxide Semiconductor
OIP_3	Output-Referred Third-Order Intermodulation Point
OP_{1dB}	Output 1-dB Compression Point
OQPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PCCPCH	Primary Common Control Physical Channel
$\frac{PCCPCH\_E_C}{I_{or}}$	The ratio of the average transmit energy per PN chip for the PCCPCH to the total transmit power spectral density.
PCNO	Power-Constrained Noise Optimization
PCSNIM	Power-Constrained Simultaneously Noise and Input Matching
PEX	Parasitic Extraction
PMOS	P-Metal Oxide Semiconductor
PN	Pseudo Noise
Q	Quadrature
Q-factor	Quality Factor
QPSK	Quadrature Phase Shift Keying
R	Parasitic resistors only
R+C	Parasitic resistors and capacitors
R-C	Resistor-capacitor
R+C+CC	Parasitic resistors, capacitors and coupling capacitors
RF	Radio-Frequency

RLC	Resistor-inductor-capacitor
Rx	Receiver
SAW	Surface Acoustic Wave
SNIM	Simultaneous Noise and Input Matching
SNR	Signal-to-Noise Ratio
SNSP	Strong-N Strong-P
SNWP	Strong-N Weak-P
SOC	System-on-Chip
S-parameters	Scattering Parameters
TDMA	Time Division Multiple Access
TM	Telekom Malaysia
UE	User Equipment
UMTS	Universal Mobile Telecommunications System
VGA	Variable Gain Amplifier
W-CDMA	Wideband-Code Division Multiple Access
WNSP	Weak-N Strong-P
WNWP	Weak-N Weak-P

LIST OF APPENDICES

LIST OF PUBLICATIONS & SEMINARS

1. Mohd. Noh, N. and Zulkifli, T.Z.A. (2006). A 1.4 dB Noise Figure RF Integrated CMOS LNA for W-CDMA Application. RFM2006 International RF and Microwave Conference, Putra Jaya, Malaysia. 12-14 September 2006.

2. Mohd. Noh, N. and Zulkifli, T.Z.A. (2007). Study and Analysis of a 0.18 um Single-ended Inductively Degenerated CS Cascode LNA Under Post-layout Corner Conditions. ICIAS2007 International Conference on Intelligent & Advanced Systems, Kuala Lumpur, Malaysia. 25-28 November 2007.

3. Zulkifli, T.Z.A., Mohd. Noh, N., Ibrahim, S.S., and Kordesh, A. V. (2007). Inductive Degeneration 0.13 um CMOS Low Noise Amplifier Utilizing On-Chip Inductors at 2.4 GHz. ROVISP2007 International Conference on Robotics, Vision, Information, and Signal Processing, Penang, Malaysia. 28-30 November 2007.

4. Mohd. Noh, N. and Zulkifli, T.Z.A. (2007). Comparative Study of the Folded-cascode, Current-reuse and the PCSNIM LNA Topologies for W-CDMA Direct-conversion Receiver. ROVISP2007 International Conference on Robotics, Vision, Information, and Signal Processing, Penang, Malaysia. 28-30 November 2007.

5. Mohd. Noh, N. and Zulkifli, T.Z.A. (2007). Design, Simulation and Measurement Analysis on the S-parameters of an Inductively-degenerated Common-source Open-drain Cascode Low Noise Amplifier. RFIT2007 IEEE International Workshop on Radio-Frequency Integration Technology, Singapore. 9-11 December 2007.

6. Mohd. Noh, N. and Zulkifli, T.Z.A. (2008). Systematic Width Determination for the Design of Power-Constrained Noise Optimization Inductively-Degenerated Low Noise Amplifier. Submitted for review to the Microelectronics International, 16 September 2008.

7. Mohd. Noh, N. and Zulkifli, T.Z.A. (2009). S-Parameter Close-Form Derivations for the Power-Constrained Noise Optimization Inductively-Degenerated Cascode Low Noise Amplifiers. Submitted for review to Elsevier Editorial System Microelectronics Journal, 2 January 2009.

PERKEMBANGAN LNA INDUKTIF-TERNYAHJANA BAGI APLIKASI W-CDMA MENGGUNAKAN TEKNOLOGI 0.18 μm RFCMOS

ABSTRAK

Satu metodologi terperinci dan bersistematik untuk merekabentuk penguat hingar rendah (LNA) induktif ternyahjana kaskod, juga dikenali sebagai topologi Padanan Masukan dan Hingar Serentak (SNIM), bagi aplikasi penerima penukaran terus (DCR) Jalur Lebar – Kod Pembahagian Berbilang Capaian (W-CDMA) diberikan dalam tesis ini. Frekuensi operasi adalah 2.14 GHz dengan voltan bekalan 1.8 V dan menggunakan proses 0.18-μm 6-logam 1-poli RFCMOS. Ini diikuti dengan analisa litar dan metodologi rekabentuk yang terperinci serta perbandingan perlakuan bagi beberapa LNA terbitan SNIM. Topologi yang terpilih ialah SNIM dengan Kekangan Kuasa (PCSNIM), Guna-semula Arus (CR) dan Kaskod Terlipat (FC). Keputusan menunjukkan bahawa bagi aplikasi voltan rendah, FC memberikan kelelurusan yang baik pada nilai angka hingar (NF) yang berpatutan. Namun, gandaan kuasanya adalah yang terendah. Prestasi SNIM LC-terpadan dan CR adalah setara, tetapi SNIM LC-terpadan bersaiz besar. Dalam keadaan simulasi yang serupa, PCSNIM menambahbaikkan angka hingar sebanyak 37% daripada yang dipamerkan oleh SNIM. Ini membuktikan keberkesanan penambahan satu kapasitor merintangi transistor masukan litar. Satu rekabentuk PCSNIM dengan keluaran berpenimbal telah dihasilkan untuk mengekalkan merit NF PCSNIM terpadan yang konvensional ke atas SNIM terpadan, tetapi dengan kelebihan ruang bentangan yang jauh lebih kecil. Gandaan kuasa SNIM dan PCSNIM LC-terpadan, serta PCSNIM dengan keluaran berpenimbal adalah agak setara tetapi kedua-dua PCSNIM kalah dari segi kelelurusan. Namun, PCSNIM dengan penimbal keluaran adalah lebih baik bagi integrasi litar kerana saiznya yang lebih kecil. S_{12} lebih baik daripada -30 dB dihasilkan oleh semua topologi membuktikan keupayaan litar kaskod untuk memencilkan keluaran daripada

masukan. Terbitan yang terperinci bagi gandaan voltan, S-parameter dan hingar bagi SNIM diberikan dalam tesis ini. Terbitan dilaksanakan menggunakan Matlab dan disahkan melalui perbandingan dengan hasil simulasi Cadence SpectreRF. Lebar transistor penguat bagi semua topologi (kecuali CR) adalah 290 μm, ditentukan melalui kaedah Pengoptimuman Hingar dengan Kekangan Kuasa (PCNO). Analisa yang komprehensif tentang kesan keadaan ekstrim terhadap prestasi LNA diberikan dalam tesis ini. Dua jenis simulasi pasca-bentangan telah dilaksanakan, mereka adalah rintangan teragih – kapasitor parasitik – kapasitor gandingan dan parasitik terkumpul. Perbandingan dan analisa dilakukan ke atas keputusan daripada simulasi pra- dan pasca-bentangan dengan keputusan daripada pengukuran. Simulasi pasca-bentangan menghasilkan keputusan yang menghampiri pengukuran dalam kebanyakan kes.

DEVELOPMENT OF INDUCTIVELY-DEGENERATED LNA FOR W-CDMA APPLICATION UTILIZING 0.18 μm RFCMOS TECHNOLOGY

ABSTRACT

A detailed and systematic methodology on the design of the inductively-degenerated cascode LNA, also known as the Simultaneously Noise and Input Matching (SNIM) LNA, for Wideband-Code Division Multiple Access (W-CDMA) Direct-Conversion Receiver (DCR) is presented in this thesis. The operating frequency was 2.14 GHz with a supply voltage of 1.8 V and implemented on Silterra's 0.18-μm 6-metal 1-poly RF CMOS process. This is followed by comprehensive circuit analysis, design methodology and performance comparisons of the modified SNIM, namely the Power-Constrained SNIM (PCSNIM), Current-Reuse (CR) and Folded-Cascode (FC) LNAs. Results show that for applications with low voltage requirement, the FC offers good linearity at a comparable NF. However, the trade-off is the gain. CR and matched SNIM are comparable in all of the performance metrics, but matched SNIM posed a disadvantage in term of space. Under similar simulation conditions, the PCSNIM was able to reduce the NF of the SNIM by 37%, proving the effectiveness of adding a capacitor at the transistor's input. A new modified PCSNIM with output buffer was designed to maintain the matched conventional PCSNIM noise figure (NF) merit over the SNIM, but with much less layout space consumed than by the latter. The power gain of the LC-matched SNIM, LC-matched PCSNIM and the new modified PCSNIM with output buffer are comparable but both PCSNIM lost in term of linearity. However, the new modified PCSNIM with output buffer will be better for circuit integration as it requires less space. S_{12} of better than -30 dB was recorded for every LNA topology in this work and this shows that the cascode configuration is able to to provide good reverse isolation. Detailed voltage gain, S-parameters and noise derivations for the SNIM LNA are provided in this thesis. The derivations for the voltage gain and S-parameters were implemented using Matlab, verified with the simulation results

generated by Cadence SpectreRF. The transistor's width for all the topologies except CR was determined at 290 μm using the power-constrained noise optimization (PCNO) method. Comprehensive analysis on the extreme or corner condition effects on the SNIM LNA performance is provided in this thesis. Two types of post-layout simulations were performed, they were the distributed resistance-parasitic capacitors-coupling capacitors and lump parasitic. Comparisons and analysis were made on the pre- and post-layout simulations and measurement results, and the post-layout results were found to better resembling the results obtained from the measurement in most cases.

CHAPTER 1
INTRODUCTION

1.0 Motivation for the thesis

Low noise amplifier (LNA) is the first block of any receiver system. Due to this fact, the LNA is considered as one of the most important stage to be designed. Thus, it is very important for the LNA to be performing well in order to provide the following stages with good signals to process. However, there is a difficulty in finding literatures which describe detailed methodology on designing the LNA. There is no write-up, to the best of the author's knowledge, that provides comprehensive description on designing this circuit starting from the application specifications, to determining the transistor's size, followed by the calculations on the associated passives involved, to the determination of the input and output matching on-chip circuitries, physical layout design and finally the measurement procedures and test-setup.

During the design of the LNA, difficulties were met in understanding the noise analysis given in many textbook. Discussions on noise are extensive in books by Lee (2001, 2004) and Razavi (1998), but no detailed derivations were given to easily understand the equations.

Because of its importance, many LNA topologies are available. Unfortunately, no literature is available on detailed comparison of these topologies starting with comprehensive design analysis, to simulation and characterization results comparison. This comparison is important as it can serve as a platform for further design improvements. It is observed that the basic circuitry of many of the topologies is the inductively-degenerated cascode. The conventional inductively-degenerated cascode LNA provides simultaneous noise and input matching and the topology is also known as SNIM (Nguyen & Lee, 2006). Studies on SNIM LNA and three modified inductively-

degenerated cascode topologies were made. The modified designs chosen were the power-constrained simultaneously noise and input matching (PCSNIM) from Nguyen & Lee (2006), the current-reuse (CR) from Karanicolas (1996) and the folded-cascode (FC) from Nguyen *et al.*(2004). Finally, a new LNA circuit was designed that combines the PCSNIM with an output buffer circuit resulting in better noise performance and superior on-chip matching.

1.1 Problem statements

Detailed methodology in designing LNAs from the initial stage of understanding the application specifications to determining the transistors' sizes, associated passives involved, on-chip matching circuitries, physical layout design, and finally the test set-up for the characterization of the fabricated designs are unavailable to the best of the author's knowledge. The chosen LNA topology to be designed is the inductively-degenerated cascode LNA, which is also known as SNIM. This topology was chosen as it is the basis for many of the LNA designs presently available due to its ability to provide simultaneous noise and input matching.

Detailed analysis on the noise and gain calculation of the inductively-degenerated cascode LNA is unavailable to the best of the author's knowledge. Presently available literature analysis on these two very important performance metrics of the LNA are not very detailed. Hence, a comprehensive description of this analysis is paramount.

There are not many literatures on comprehensive comparison between presently available LNAs in terms of the design analysis and simulation results. The chosen topologies are the SNIM, PCSNIM, CR and FC. PCSNIM, CR and FC were chosen as they are evolutions from the conventional state-of-the-art inductively-degenerated cascode LNA (SNIM).

1.2 Objectives

Concurrent to the problems that had been stated in (1.1), the following objectives were set to tackle these problems:

1. To design an LNA with good noise and gain performances following the specifications set by the W-CDMA standard.

2. To study a suitable topology for the LNA in a W-CDMA DCR such as the the inductively-degenerated cascode. Subsequently, detailed noise, gain and S-parameter analysis of the chosen topology will be performed from the small-signal model incorporating the capacitances for high frequency analysis.

3. To study and analyze the modified circuits of the inductively-degenerated cascode LNA such as the PCSNIM, CR and FC LNAs and make comparison on the merits of each one with reference to their noise figure and gain performances.

1.3 Contributions

The following are the contributions from the accomplishments of this project :

1. A modified inductively-degenerated cascode LNA design with PCSNIM merits and output buffer for on-chip matching enhancement was designed.

2. A systematic and detailed methodology on designing the inductively-degenerated cascode LNA was presented. The methodology starts from the determination of the standard specifications, followed by derivations for the noise, gain and S-parameters from the small signal analysis of the schematic,

the calculations for the passive components, implementation of on-chip matching circuitry, and finally the chip characterization.

3. Detailed noise, gain and S-parameters analysis with extensive derivations from the small-signal model of the inductively-degenerated cascode LNA were given.

4. Comparative study of the designs and simulated performances of the PCSNIM, CR and FC LNA topologies with reference to the inductively-degenerated cascade (SNIM) LNA were detailed out in this thesis.

1.4 Organization of the thesis

The thesis starts with the Introduction in Chapter 1. In this chapter, the thesis motivation, problem statements, project objectives, contributions and organization of thesis are given.

An overview of the wireless standard for the application of the LNA's in this work and the receiver topology where the LNA is to reside are given in Chapter 2. Specifications of the standard and characteristics of the receiver are given in this chapter as they are important to be known prior to designing the LNA. Specifications of the wireless standard become the bench mark for the LNA's performance. In this work, the LNA is for the W-CDMA application and the intended receiver is the direct-conversion type as it is the best architecture for this wireless standard due to the high integration level that it is capable of. High level of integration in a transceiver architecture is very important especially in wireless and portable systems.

Chapter 3 is on the introduction to the amplifier topologies and LNA performance metrics. This chapter states the functions of the LNA with its design

goals, and describes the different amplifier topologies available namely the common-source amplifier with shunt-input resistor, common-gate amplifier, shunt-series amplifier, inductively-degenerated common-source amplifier, inductively-degenerated cascode amplifier and lastly, the differential inductively-degenerated cascode amplifier. As for the LNA performance metrics, the S-parameters, gain, linearity and noise definitions and descriptions are given.

Chapter 4 covers the analysis of five LNA topologies, which includes the conventional inductively-degenerated cascode amplifier (also known as SNIM) and its modifications. The modified SNIM LNA topologies studied are the PCSNIM, CR and FC. Merits and weakness of each design are included in the analysis. Finally, a desription of the modified PCSNIM LNA designed in this work is given here.

The LNAs design methodologies are given in Chapter 5. This chapter starts with the methodology in designing the SNIM LNA. An explanation on the power-constrained noise figure optimization technique to determine the LNA transistor's width that can provide the optimum noise performance is given here. This is followed by the methodology in calculating the passive components constructing the LNA. Subsequently, the determination of the current mirror components values were elaborated. The conventional basic current mirror became the standard biasing circuit in every LNA design in this work. The determination of the input and output matching circuitries were given in the next section followed by the layout design issues in the final section. The methodologies in designing the PCSNIM, CR, FC and the new PCSNIM with output buffer LNAs are thoroughly discussed in this chapter.

The LNA design analysed in this work were simulated and the SNIM and PCSNIM LNA topologies were characterized. The results of the simulation and measurement are given in Chapter 6. Pre- and post-layout simulations were performed

and comparisons between the two were made and differences explained. Finally, the simulated performances of the LNAs are compared with the specifications imposed by the W-CDMA standard. In order to characterize the fabricated design, test setup has to be constructed. Chapter 6 gives the test-bench setup for the measurement of the single-input LNA. The set-ups are for measuring the DC, S-parameters, P_{1dB} and noise. Naturally, the subsequent section will be on the measurement results on the various experiments performed on the inductively-degenerated cascode LNA.

Chapter 7 concludes the findings of the work in this project. It also includes future work that can be performed to further develop the research on the LNA.

Additional to the seven chapters described, important theories and derivations are included in the appendices. These materials may help in enhancing the understanding of certain calculations utilized in the designing of the LNAs. Appendix A1 is on the derivations to show the relationship between the reflection coefficients.and the S-parameters. Appendix A2 consists of the derivations of the harmonic and inter-modulation products using the Taylor's series expansion. Appendix A3 contains derivations for determining the current in saturation for short channel devices. Appendix A4 shows the derivations involved in generating the power dissipation, P_D, versus ρ noise contour plots. Appendix A5 is on the derivations for obtaining P_D versus Q factor noise contour plots. Appendix A6 is on the Matlab codes and solutions for determining S_{11}, S_{21} and S_{22}. Appendix A7 has the derivations for determining inductances of the CR LNA. Appendix A8 displays the microphotographs of the SNIM and PCSNIM LNAs fabricated. Their layouts are also given as comparisons. Besides these, the layout diagrams of the CR, FC and the newly designed PCSNIM with output buffer are also shown. Finally, Appendix A9 shows the values of Q of the inductors characterized by Silterra at 2.45 GHz.

CHAPTER 2
OVERVIEW OF THE RECEIVER ARCHITECTURES AND W-CDMA REQUIREMENTS

2.0 Introduction

It is very important to choose and understand the receiver architecture where the LNA will reside. This is so that the merits and problems of the architecture are considered during the design stage of the LNA. Equally important (if not more) is the wireless standard that will be applied to the LNA. The specifications imposed by the standard will be the benchmark to the performance required from the LNA.

In the past few decades, the wireless communication has become very popular that it has shaped the trend in transceiver designs. Modern receiver designs are focused on increasing the integration level between RF and mixed-mode circuitries. The move is towards producing “single-chip radios”. There are a number of receiver architectures which had been and still are very popular in radio designs such as the superheterodyne receiver. Besides this, there is the direct-conversion receiver (known also as DCR or DICON) and its spin-off such as the Low-IF. Another architecture that is worth mentioning is the Wideband-IF Receiver.

The DCR is the receiver architecture that seems to be the most appropriate choice for achieving full circuit integration on chip. Full circuit integration is of utmost importance in the present portable and wireless technology transceiver design as this is how multiple radio standards can be accommodated in one radio. Besides this, full integration will result in smaller radio size and consequently, better portability. DCR’s architecture is less complex and smaller in size since there is less number of blocks due to the elimination of multiple IF stages and image reject and RF filters. Due to this simple architecture, the DCR is capable of lowering the power consumption and fabrication cost when compared to superheterodyne.

Another advantage of DCR is that it uses only LPFs after down-conversion. For the wireless standard like the Wideband-Code Division Multiple Access (W-CDMA), the channel bandwidth is adjustable at 5 MHz, 10 MHz and 20 MHz to support the signal bandwidth of 3.84 Mcps, 8.192 Mcps and 16.384 Mcps respectively. This requirement makes the DCR to be the best architecture for this application as the different bandwidth of the receiver can be obtained by altering the cut-off frequency of the integrated LPF (Pretl *et al.*, 2000b; Lie *et al.*, 2002). Adjusting the cut-off frequency of a LPF is much simpler than changing the bandwidth of a BPF at high frequency.

The LNA designed in this project is for the W-CDMA application. Due to the capabilities of the DCR, this LNA has to reside in a DCR environment. All issues related to a DCR will have to be taken into consideration during the design period. However, what is more important is understanding the requirement set by the W-CDMA standard as this will form the design goals of the LNA.

The W-CDMA system is for the third-generation (3G) cellular communication. W-CDMA uses the Direct Sequence Code Division Multiple Access (DS-CDMA) signaling method to gain higher speed and to support more users as compared to the previous second-generation wireless telephone standard (2G) Global System for Mobile Communications (GSM) which employs Time Division Multiple Access (TDMA) signaling method (Pärssinen, 2001).

W-CDMA is also commonly known as Universal Mobile Telecommunications System (UMTS). UMTS is the 3G standard in Europe whereas W-CDMA is the standard for 3G in Japan. Irrespective of what it is known as, W-CDMA (or UMTS) is a mobile communications technology that can cater data transmission speeds up to 2 megabits per second (Mbps). Actual speeds are lower at first due to the capacity limit on the network. The present 3G systems are commonly using 384 kbps of data rate.

W-CDMA or UMTS has a transmitting frequency band in the range of 1920-1980 GHz. The received frequency band is in the range of 2110-2170 GHz.

2.1 Receiver types

2.1.1 Superheterodyne receiver

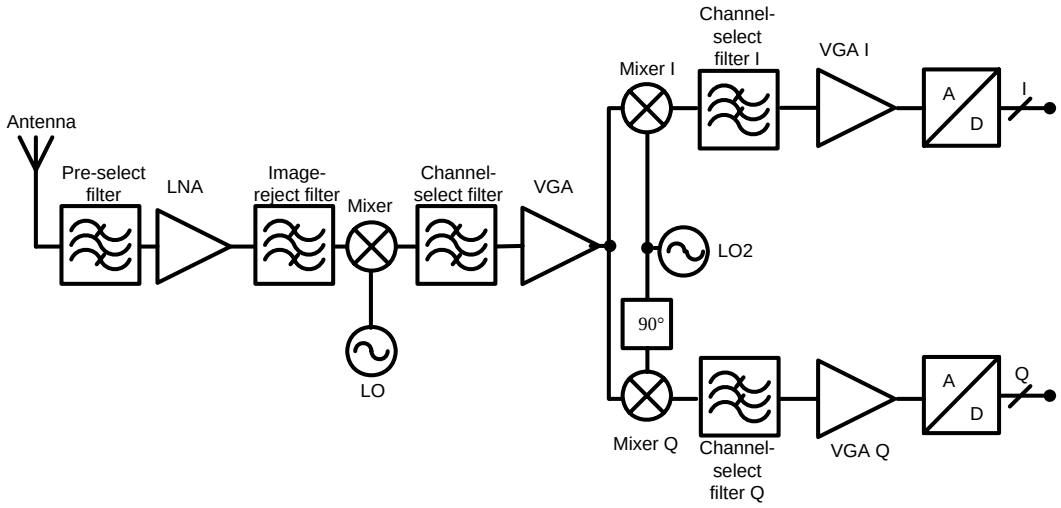

Figure 2.1: A typical superheterodyne receiver with a quadrature demodulator (Zou *et al.*, 2004; Ryynanen, 2004).

The present domination in receiver architecture is by the superheterodyne receiver. The receiver's architecture is shown in Figure 2.1. Heterodyne means two signals of different frequencies combined to produce the sum and difference of the original frequencies. The RF signal that reaches the antenna is first fed into a filter which is of the band-pass type (this filter is also called pre-select filter, selecting the frequency bandwidth of interest). The function of this filter is to remove the out-of-band signals. The signal is then amplified by a low noise amplifier (LNA). This amplifier is not only to amplify the small magnitude RF signals, but more importantly it amplifies with the least addition of noise to the system. The LNA has a very strict noise performance requirement. The LNA output is then filtered by an image-reject filter. This filter is to remove the image, which is a side effect of the mixing process. The image signal has an offset of twice the intermediate frequency from the desired channel signal

frequency. Subsequent to the filter, the signal is down-converted to the intermediate-frequency (IF) by the mixer. An IF signal is obtained when the signal at the desired frequency and another signal generated by a local oscillator (LO) are mixed. In a receiver, down-mixing is performed, i.e. the IF signal's frequency is the difference between the RF and the LO frequencies. In a transmitter, the opposite is performed, i.e. up-mixing to produce an IF signal which frequency is a summation of the RF signal with the LO. Down-mixing is performed in a receiver to ease amplification and rejection of the unwanted signals prior to the baseband circuitries. The conversion to the baseband may require several IF stages.

Figure 2.1 shows a receiver which has two of such stages. The output of the mixer is then fed to a channel-select filter that performs channel selection at the IF, and a variable gain amplifier (VGA) will further amplify the filter's output. Subsequently, demodulation or detection is carried out to retrieve the desired information.

Main disadvantages of the superheterodyne receiver architecture are its cost, large power consumption and size. Significant contributors to the cost are the RF, image and IF filters (Razavi, 1997). The large power consumption is also due to the losses in these external filters (especially ceramic band pass or SAW filters), which have to be compensated by having amplifying sections. These filters are the components that limit the level of miniaturization, the minimum cost, and the minimum power dissipation that can be achieved. Nevertheless, since 2002, the Bulk Acoustic Wave (BAW) filters have started to gain popularity due to their compatibility with VLSI and CMOS processes and high frequency capability (up to 8 GHz) with good rejection of 40 dB and small size (1.5 x 2 x 0.6 mm) (Aigner, 2003; Leti, 2006). However, due to the many filters required by the superheterodyne, the size of the integrated transceiver will still be huge.

Having the possibility of requiring multiple IF stages means a possibility of increasing fabrication cost and power consumption too. Due to the large number of blocks, a superheterodyne receiver might not be the right choice to fulfill the need for full transceiver integration required by the present portable and wireless technology although it is still considered as the most sensitive and selective architecture.

Extensive research had taken place to achieve good performance with any other possible receiver architectures more suitable for integration. The direct-conversion receiver was deemed most appropriate for highest level of integration.

2.1.2 Direct-conversion receiver (DCR)

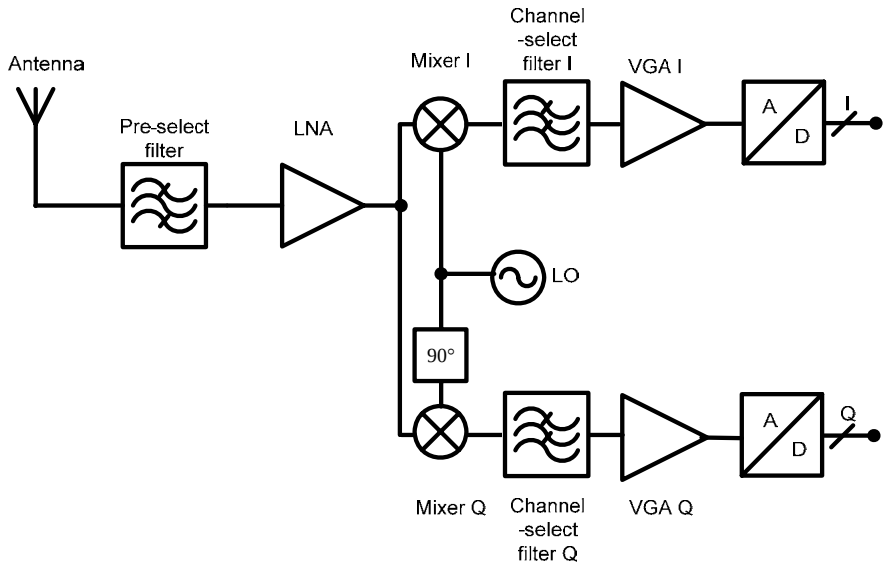

Figure 2.2: A direct-conversion receiver (Springer *et al.*, 2002; Zou *et al.*, 2004; and Ryynanen, 2004).

A DCR block diagram is shown in Figure 2.2. A DCR is not new, it was in fact invented many decades ago. It was invented in the same era as superheterodyne. DCR was an option to the superheterodyne, but it was not as popular as it has many drawbacks. However, DCR has made a comeback recently and this is due to the improvement in IC technologies. DCR's past failures were from effects that could not

be removed in discrete implementations, but may be controlled and suppressed in integrated circuits. DCR drawbacks can be overcome by using more transistors and this is possible as the IC technology has advanced tremendously.

Also called zero-IF or homodyne conversion, DCR is an efficient approach to downconvert a signal from RF straight to baseband in one step. This is achieved by mixing the RF with an oscillator signal of the same frequency. Since the DCR converts the carrier of the desired channel to zero frequency immediately in the first mixers, there is no longer a necessity for extra down conversion circuitries for final downconversion. This also means that multiple local oscillator circuitries can be eliminated. Hence, due to the less number of blocks, the architecture becomes less complex and consumes less power. As the RF signal being directly converted to baseband, the DCR employs low pass filters (LPF) for filtering out unwanted interferers. LPF (which is by design less complex than BPF) and baseband amplifiers can be implemented on chip, making the goal of producing a fully integrated receiver possible. The cost of producing this type of receiver is also reduced due to the absence of the expensive filters at RF (for image rejection) and at IF (for channel selection).

Since DCR directly converts RF to baseband, no image rejection filter is required. This is an advantage as an image reject filter is a high-selectivity high frequency BPF, and therefore this filter is only possible to be implemented off-chip. Hence, there will exist problems in matching the LNA with this off-chip image reject filter as what is faced by a superheterodyne receiver. Since a DCR's LNA need not drive the 50 Ω load as there is no image reject filter, the DCR suffers much less from mismatch-induced effects as compared to the superheterodyne receiver which has this image-reject block. If the BAW filters are to be implemented in the superheterodyne, the DCR will still be having an advantage as it consumes less space due to the absence of the image reject and IF filters.

To summarize, the DCR enables higher level of integration as it is simpler, smaller in size and less costly compared to the superheterodyne. This architecture has a potential to accommodate multiple radio standards with different channel bandwidths (i.e. wide frequency band) on one chip. However, there are some drawbacks with DCR including dc offsets, LO self-mixing, flicker (1/f) noise, and even-order nonlinearities, which post a great challenge to designers (Namgoong & Meng, 2001; Manku, 2003). DC offsets from various sources lie directly in the signal band of interest, and in the worst case they can saturate the back-end of the analogue receiver at high gain values. One way to overcome this problem is to use a variable gain LNA to cater for very small to large amplitude signals. The drawbacks of the DCR are elaborated and discussed further in Section 2.2.

The DCR is not free from drawbacks and there are a few receiver architectures designed to overcome these problems. These architectures are the Low-IF and the Wideband receivers.

2.1.3 Low-IF receiver

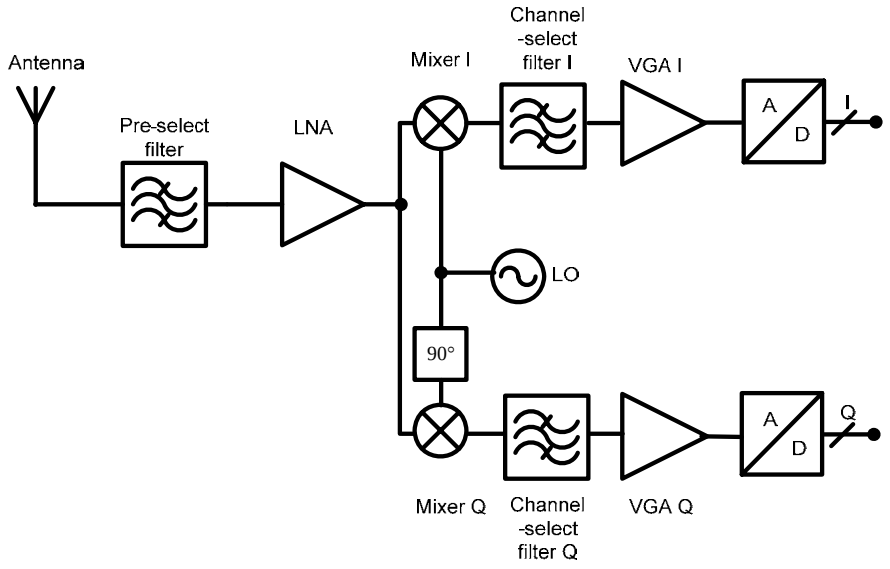

Figure 2.3: Block diagram of low-IF receiver (Pärssinen, 2001).

Figure 2.3 illustrates the block diagram of a low-IF receiver. The low-IF receiver differs from DCR in that the first IF is placed above dc (does not convert the signal directly to baseband) but its frequency is lower than half of the system reception bandwidth, i.e. $0 < f_{IF} < B_{system}/2$. This receiver architecture was originally proposed to reduce the drawbacks of a DCR.

How "low" is the IF of a Low-IF receiver? If the lowest IF (next to dc) is chosen, flicker noise, self-mixing and envelope distortion should be considered (just like in a DCR) but the image rejection requirement is relaxed. If the higher IF is chosen, the problems above can be avoided because there is no signal information at around dc. Thus, dc offsets can be filtered without signal information being removed. The drawbacks, however, are that the 2^{nd} order nonlinearity still exists and now a strict image reject requirement is imposed.

From the block diagram in Figure 2.3, the signal is divided into quadrature branches in the first downconversion. This is to separate the unwanted image from the desired channel (Pärssinen, 2001). However, matching between the I and Q branches is critical if sufficient image rejection is to be achieved.

The channel selection is performed with a BPF. Because of the low frequency operation, this filter can be integrated as it now becomes possible to design a high order filter using low frequency IC filtering techniques such as Gm-C or switched capacitor filters. A LPF, in fact, should be sufficient to perform this function, but a BPF has the capability to remove static offsets.

Low-IF has a limitation of only 30 to 55 dB of image suppression achieved with on-chip matching, whereas in an application like W-CDMA, strict image reject

requirement of at least 40 dB is required to pass the adjacent channel selectivity test (Pretl *et al.*, 2000b).

2.1.4 Wideband-IF receiver

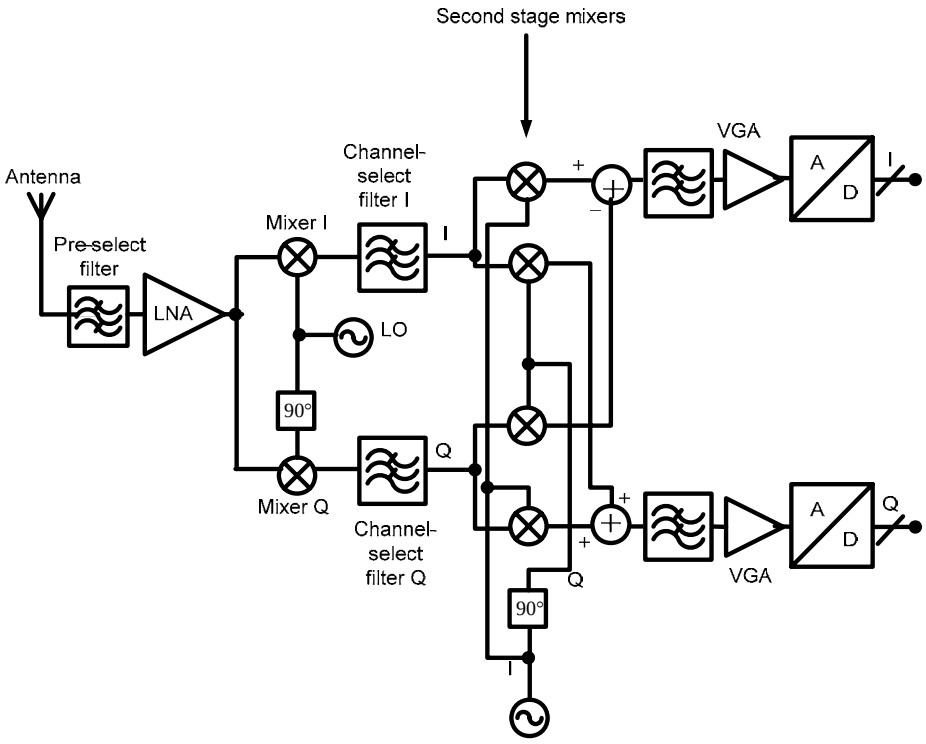

Figure 2.4: Block diagram of the wide-band IF receiver (Pärssinen, 2001).

With the objectives to not only mitigate the problems created by image frequency rejection strict requirement in order to have a fully integrated transceiver, but also to reduce the drawbacks of a DCR, designers have come out with an architecture that can accomplish both desires. An image rejection receiver as shown in Figure 2.4 is suitable for integration. This receiver has two downconversion stages but performs the channel selection completely after the second downconversion. However, the architecture becomes more complex than the DCR due to the existence of the second stage mixers.

In general, the LNA is always the first block to receive the RF signal from the pre-select filter. The receiver architectures maybe different, but the performance requirements for the LNA are very similar. The main differences between the different architectures, however, are the output load, reverse isolation, and the different spurious signals on-chip. The LNA load can be an external filter or an on-chip device. If the load is not an external filter, the interface between the LNA and mixer can be altered to optimize receiver performance. If the load is an external filter having an input impedance of 50 Ω, then the design becomes tougher as an output driver maybe required. As consequences, the gain and power consumption are not optimized. In term of reverse isolation, this parameter becomes important if the LO frequency is in the reception band of the receiver. The LNA may need high reverse isolation in order to prevent self mixing.

2.2 Issues in receiver topologies

2.2.1 Superheterodyne receiver

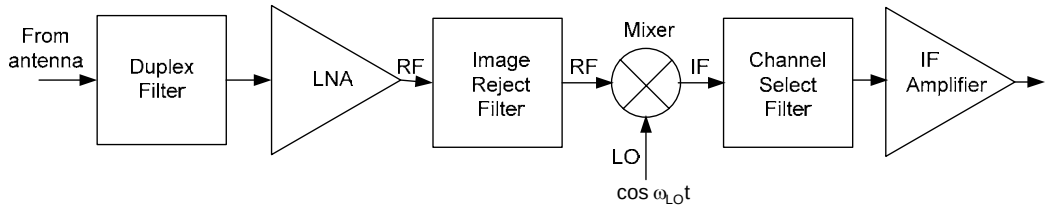

Figure 2.5: Simplified block diagram of a superheterodyne receiver (Larson, 1998).

Figure 2.5 shows the simplified block diagram of the superheterodyne receiver. The mixer performs two types of mixing, one is the up-conversion mixing and the other is down-conversion mixing. For the up-conversion mixing:

$$\omega_{LO} + \omega_{RF} = \omega_{IF} \tag{2.1}$$

For the down-conversion mixing:

$$\omega_{LO} - \omega_{RF} = \omega_{IF} \tag{2.2}$$

Up-conversion mixing is used in transmitters whereas down-conversion mixing is employed in receivers to ease the baseband processing.

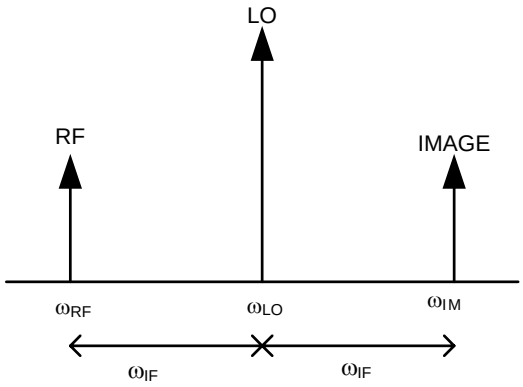

Figure 2.6: RF, LO and Image relationship.

Another by-product of the mixing is the image signal. This signal can be represented by the following Equation 2.3 (Razavi, 1998) and is shown in Figure 2.6.

$$\omega_{IM} = \omega_{LO} + \omega_{IF} = \omega_{RF} + 2\omega_{IF} \tag{2.3}$$

Here, ω_{IM} is the image angular frequency. If the image is not properly attenuated, it will be fed to the mixer and subsequently will be mixed with the LO. Mixing will produce components at $\omega_{IM} \pm \omega_{LO}$ (Razavi, 1998).

$$\omega_{IM} + \omega_{LO} = 2\omega_{LO} + \omega_{IF} \tag{2.4}$$

$$\omega_{IF} = \omega_{IM} - \omega_{LO} \tag{2.5}$$

The frequency ω_{IF} in Equation (2.1) can be easily filtered out by the channel select filter, but components at the frequency of Equation (2.2) really fall on the desired

signal frequency. An image reject filter is therefore very necessary to be placed before the mixer to filter out the image signal.

(a) Trade-off between image rejection and interferers' suppression

In real situation, the wanted signal will not be the only signal captured by the receiver, but with it comes interferers as well. The interferers that are of great concern are the ones that are very close to the frequency of interest. Besides the interferers, there will also exist the image signal whose method of generation had been discussed previously.

Referring to Equation (2.3), the image signal frequency, ω_{im}, is located two times the intermediate signal frequency, $2\omega_{IF}$, away from the frequency of the signal of interest, ω_{RF} (Razavi, 1998). If the IF is high, the image will be located far from the frequency of the signal of interest. Hence, the image reject filter will be able to greatly attenuate this image signal. Unfortunately, it is very difficult to obtain a highly selective filter to operate in the GHz range. So, the image reject filter will not be able to attenuate the nearby interferer signals much, and subsequently, this interferer signals will also be mixed with LO. As a result, unwanted signals near to IF will be produced. If the IF is high, then selectivity of the IF filter is also not that good and therefore the nearby interferers will still remain at significant levels at the output of the IF filter. On the other hand, if the IF is low, the image signal will be too close to the signal of interest, the image reject filter will not be able to attenuate the image signal much and this image signal (together with the interferer signal) will still be mixed with LO. Since the IF is low, an IF filter with high selectivity is obtainable and due to its high selectivity, the filter can filter out the interferers easily. However, the image signal that was not suppressed appropriately by the image reject filter will fall exactly on the wanted signal after mixing and this will corrupt the downconverted signal (Abidi, 1995b, Razavi, 1997). Figure 2.7

shows this image rejection and interferers' suppression trade-off phenomena.

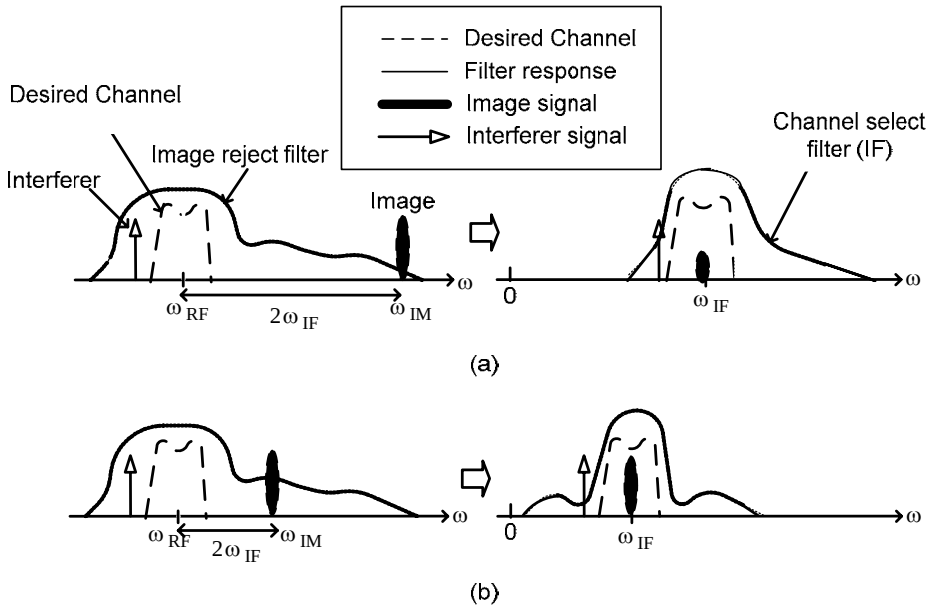

Figure 2.7: Image rejection versus interferer's suppression (Razavi, 1998) for (a) High-IF and (b) Low-IF.

To overcome this trade-off, both the image reject filter and the IF filter require highly selective transfer functions that are actually impractical to implement on-chip. Therefore, the solution has always been to employ external, bulky filters such as surface acoustic wave (SAW) devices (Jensen *et al*., 2000, Reynolds *et al*., 2003a). In addition, most systems will utilize two IF filters from two stages of mixing to compromise between the two rejections. This results in more oscillator circuits, a more complex and large circuitry. A fully integrated circuit is quite impossible to be achieved from this type of receiver. However, with the recent development in the BAW filters, there seems to a light at the end of the tunnel for fully integrated superheterodyne transceivers. Unfortunately, the limitation is on the size of the integrated superheterodyne as it requires many filters and more complex circuitries compared to the DCR.

(b) 50 Ω impedance requirement

Filter typically has a 50 Ω input and output impedance. Due to the existence of the off-chip duplex and image reject filter, the LNA has to be input and output matched to 50 Ω. This off-chip implementation adds another set of trade offs among noise, linearity, gain, and power dissipation of the LNA (Pärssinen *et al.*, 1999).

2.2.2 DCR

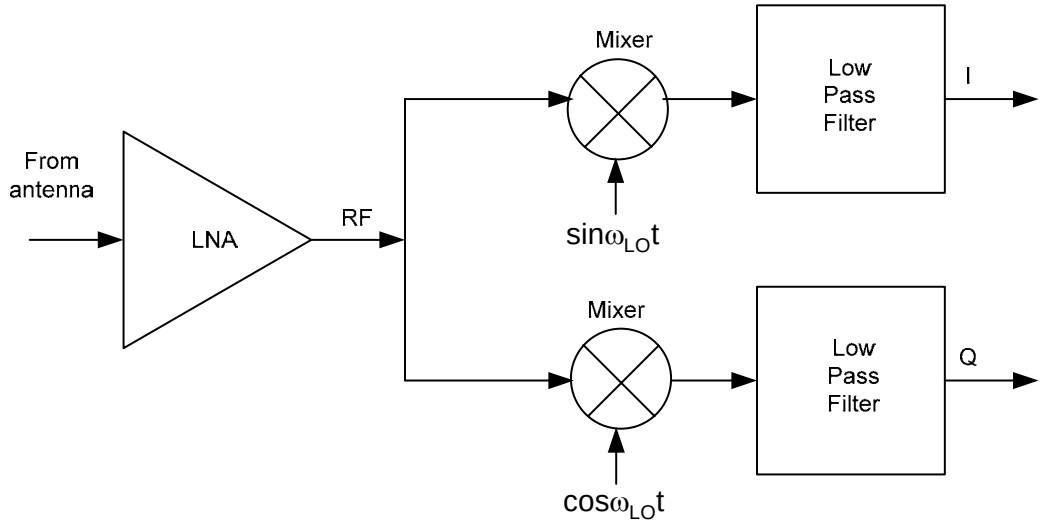

Figure 2.8: Simplified DCR block diagram.

Although DCR is known for its potential in fully implementing integrated blocks of the transceiver, there are a few design issues existing in DCR (Gharpurey *et al.*, 2003). As it is known, the RF and LO in a DCR are both at the same frequency and this contributes to an IF of 0. The mixer in a DCR will produce components at $2\omega_{RF}$ and 0, that is

$$\omega_{LO} + \omega_{RF} = 2\omega_{RF} \tag{2.6}$$

and

$$\omega_{LO} - \omega_{RF} = 0 \qquad (2.7)$$

The components with the $2\omega_{RF}$ can be easily filtered by the low pass filter. The desired signal band in a DCR has a carrier at baseband as shown by Equation 2.7. Hence, most of the problems in a DCR arise from both static and dynamic low-frequency distortion terms that fall in this baseband. These distortion terms are generated from the coupling between the LO and RF signals and also from 2^{nd}-order intermodulation products (explained in greater detail in Sub-section 3.3.2) that are produced by the quadrature mixers and the subsequent baseband amplifiers and filters. These blocks can translate any signal with amplitude variations to the baseband frequency where the desired signal lies.

Since DCR frequency band of interest lies at 0 carrier frequency, the issues mentioned are most severe in DCR compared to superheterodyne (whose carrier is at IF). The issues associated with low-frequency distortion terms that fall in the baseband can be divided into four categories and are explained below.

(a) DC offsets

Downconverted band in DCR is at zero frequency. Thus, any dc offset voltages can corrupt the signal. The most critical case is when these dc voltages are large enough to affect the biasing of the transistors in the circuits of the following stages (this condition can disrupt the amplification of the desired signal) (Khalil *et al.*, 2003, Ryynanen, 2004). The causes of the dc offsets can be better explained by the following diagrams.

Capacitive and substrate coupling will cause a feedthrough (also called LO leakage) to occur when there is an imperfect isolation between the LO port and the

inputs of the LNA and the mixer. This phenomena is shown in Figure 2.9. If the LO is provided externally, the offset will arise from bond wire coupling.

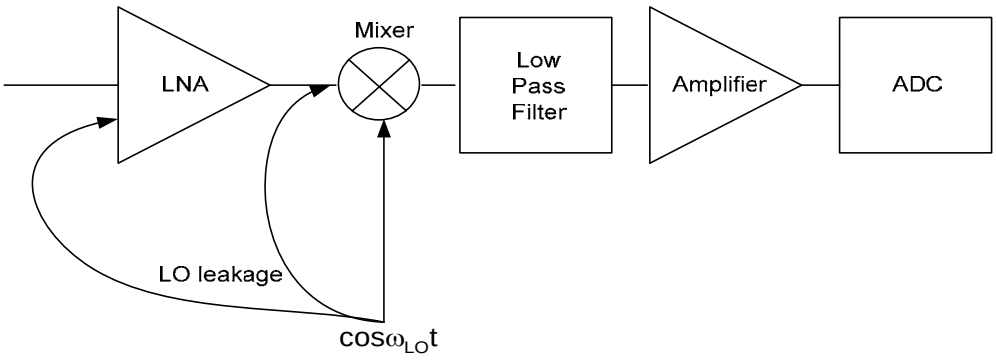

Figure 2.9: LO leakage due to imperfect isolation between the LO port and the inputs of the LNA and mixer (Razavi, 1998).

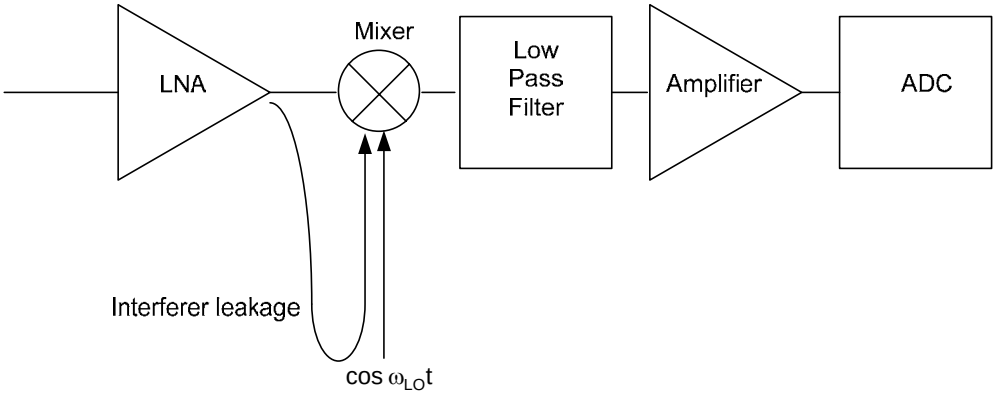

Figure 2.10: Interferer leakage due to large interferer that leaks from the mixer input to the LO port (Razavi, 1998).

When feedthrough occurs, leakage signal will reach the mixer and subsequently mixed with the LO signal, creating what is known as “self-mixing”. Self-mixing can generate dc components which can saturate the following stages. LO signal can also leak to the antenna through the mixer and LNA as these blocks have finite reverse isolation. This leaked signal is radiated and will become an in-band interferer to nearby receivers that are tuned to the same frequency band (Abidi, 1995b). The leakage signal can also be reflected from moving objects back to the receiver. This leakage is an

important issue especially in DCR as the LO frequency is the same as the RF frequency, and hence the leakage signal falls in the frequency band of interest. Similar effect occurs if large interferer leaks from mixer input to LO port. This condition is called interferer leakage. This phenomena is shown in Figure 2.10.

(b) Flicker noise

The downconverted signal at the output of the mixer is usually very small, in tens of microvolts. The input noise of the subsequent stages, like the amplifiers and filters, is therefore still critical. The signal of interest at this stage is located around zero frequency and thereby is susceptible to the flicker noise (1/f noise). Flicker noise is a severe problem in MOS circuitries (Abidi, 1995a, Razavi, 1997, Ryynanen, 2004). Due to this problem, a relatively high gain in the RF range is desirable. High gain can be achieved through the use of active mixers rather than passive mixers.

Flicker noise arises from random trapping of charge at the oxide-silicon interface of MOSFETs. Represented as a voltage source in series with the gate, the noise density is given by (Razavi, 1999, 2001)

$$\overline{v_n^2} = \frac{K}{WLC_{ox}^2}\frac{1}{f}\Delta f \qquad (2.8)$$

where $\overline{v_n^2}$ is the mean square noise voltage in V^2, K is a process-dependent constant in C^2/m^2 , W and L are the width and length of the transistor, respectively, in m, f is the operating frequency in Hz, Δf is the noise bandwidth in Hz over which the measurement is made, and finally, C_{ox} is the oxide capacitance in F/m^2.

While the effect of flicker noise may seem negligible at high frequencies, this effect is an issue in DCR as the carrier is directly converted to baseband. From

Equation (2.8), it can be seen that the effect of flicker noise is reduced by incorporating very large devices.

(c) Even-order distortion

Typical superheterodyne RF receiver are affected by only odd-order intermodulation effects as the IF is at quite a high enough frequency. In a DCR where the RF is directly converted to baseband, even-order distortion also becomes a problem as this distortion occurs at baseband. Second order nonlinearity can be characterized using the second-order intercept point, IP_2. To address the problem of even-order distortion, there are design techniques available that makes achieving high second order linearity possible. Examples are by utilizing capacitive degeneration and ac coupling in the mixer circuit. Differential mixer topology will also be less susceptible to this second-order distortion. Trying to mitigate the problem of even-order distortion at the LNA stage is quite difficult as the antenna and duplex filter are typically single-ended due to the requirement of the power amplifier in the transmit path of the transceiver. Converting the single output from these blocks to differential signals (if differential LNA is to be used) requires an extra element like the balun. Unfortunately, transformers generate losses at high frequencies which will increase the overall noise figure (Razavi, 1997).

(d) LO leakage

As has been mentioned previously, this leakage results in dc offsets (Ryynanen, 2004). Besides this, if the LO signal leaks to the antenna and gets radiated, this signal creates interference in the band of other receivers using the same wireless standard. In superheterodyne receivers, this issue is less severe because the LO frequency in these receivers are typically out of the reception band.

With the advancement of IC technology, the problem of LO leakage becomes